Wafer Fused Vertical Cavity Lasers

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# Chapter 1
# **Introduction**

## 1.1 Overview

The advancement of technology to more sophisticated and useful inventions has rested on scientists' and engineers' abilities to combine different building blocks in more sophisticated and complex manners. Development of the building blocks, whether they be pre-assembled components or raw materials, has occurred at the same time as the advancement of the state of the art in technology. For example, as calculating machines advanced, so that a computer which once filled a room the size of a small house shrank to the size of today's more powerful hand-held calculator, the workhorse component in these machines advanced from vacuum tubes to discrete transistors to integrated circuits.

Equally important as the development of more sophisticated basic components has been the development of more advanced ways to combine those basic components. The basic components of the transistor are materials with different majority carrier conduction types. Since the initial demonstration of the

transistor[1,2], more sophisticated methods in the form of epitaxial growth techniques have been developed for semiconductors. These growth techniques ease the combination of materials of different conduction types and of different energy gaps. This has allowed the creation of heterostructure semiconductor lasers, where the optical mode and injected carriers are confined by materials of different energy gap. The ability to combine different materials has not been without its limits, however. In general, the possible material combinations have been limited to those which have the same lattice constants. In order to grow high quality crystals without a high concentration of defects, it has been necessary to use materials of the same lattice constant.

With the recent advent of wafer fusing and other bonding techniques, however, this last restraint to the ability to combine materials has been removed. In particular, the combination of GaAs- and InP-based materials using wafer fusion has led to the creation of the long-wavelength vertical-cavity surface-emitting lasers (VCSELs) which I will discuss in this thesis. In this chapter I will discuss the need for vertical cavity lasers. Then I will review briefly the background of the long wavelength VCSEL field and show the advances that have been made possible by using high reflectivity GaAs/AlAs mirrors in long wavelength VCSELs. Finally I will give an overview of the dissertation.

## 1.2 Advantages of VCSELs

As fiber optic networks begin their second quarter century of existence, it is clear that they are no longer a laboratory curiosity but are a vital and growing tool for information transmission. The large bandwidth and high speed available with

optical fiber technology make it attractive for applications from short-distance computer data-links to long-haul, intercontinental telephone transmission. A key component of these fiber optic networks are lasers which operate at 1.3 and/or 1.55 µm wavelength. These wavelengths are important in that the zero in pulse dispersion and minima in optical loss in silica fibers occur at these wavelengths.

VCSELs due to their unique geometry offer a number of practical advantages for sources in optical fiber networks. Unlike an in-plane laser, light is emitted out of the top of the chip through a lithographically defined emission window. The resulting circular beam output and narrow beam divergence make the light much easier to couple into optical fibers than it is from an in-plane laser. A major cost and an area in which the ultimate performance of finished semiconductor lasers often degrades is in packaging. A large part of the packaging cost is incurred in aligning the light output with an optical fiber. The ease of fiber coupling from VCSELs should substantially reduce the cost of packaged semiconductor lasers.

In addition to the shape of the optical mode, VCSELs present other advantages for high volume, low cost manufacturing. Because the light is emitted out of the top of the chip, facets do not need to be cleaved prior to testing the devices. This should reduce the failure rate due to cleaving. Perhaps more importantly, however, this aspect of the VCSEL's geometry allows on-wafer testing using high speed, automated techniques that are impossible to use with in-plane lasers. During the testing, bad devices can be marked on the wafer and discarded before further money is spent dicing and packaging them.

Another advantage of the VCSEL is that it is ideal for use in applications which require one- or two-dimensional arrays. VCSELs for implementation in a parallel

fiber data link which uses fiber ribbon cables are easily designed so that the spacing between devices exactly coincides with the fiber-to-fiber spacing in the fiber ribbon cable. Although this can also be done with in-plane lasers, the VCSEL has the advantage that light from a VCSEL can be more readily coupled into the fiber. The VCSEL has a particular advantage in applications requiring a two dimensional array of devices. Instead of stacking individuals laser bars on top of each other as would be the case for in-plane lasers, all of the VCSELs required for the application could be placed on the same die. The emitters from each VCSEL could be placed as closely together as desired without the constraint of the substrate thickness imposed on the two-dimensional array of in-plane lasers. Because the lasers are close together on the die, growth uniformity and the resulting uniformity in output characteristics is inherently better in the VCSEL two-dimensional array than in the in-plane laser array. Growth non-uniformity can be intentionally added to the process, allowing the creation of two-dimensional arrays with different wavelengths at each source [3]. This is an ideal source for WDM systems[4,5], either for long haul telecommunications purposes where sources at 1.3-1.55 µm are necessary due to fiber loss (Fig. 1.1) or for shorter haul, metropolitan- and local-area networks.
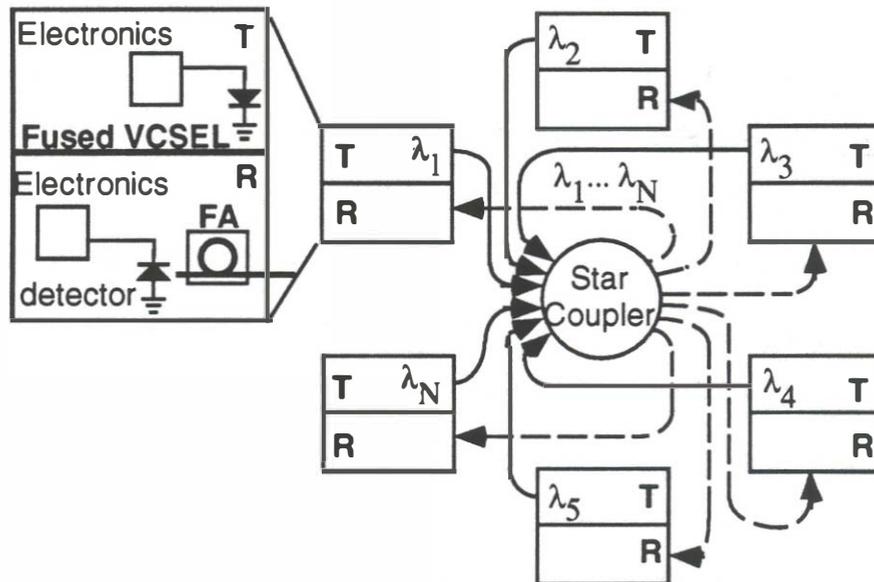
**Fig. 1.1** One possible application for the wafer fused VCSELs is in wavelength division multiplexed (WDM) networks such as the one illustrated here. Both the transmitter (T) and the receiver (R) can be made using similar processes which utilize wafer fused GaAs/AlAs mirrors. A tunable filter at each receiver allows reconfiguration of the network and a fiber amplifier (FA) boosts the signal.

In addition to the technological applications, the geometry of VCSELs leads to several exciting fundamental scientific reasons for studying VCSELs. The VCSEL is an almost ideal semiconductor medium for studying cavity quantum electrodynamics. Because of the reduced cavity size from a typical in-plane laser, VCSELs have fewer cavity modes. Thus, the fraction of spontaneously emitted photons which go into the lasing mode increases. This has led to the prediction of several interesting effects in microcavity lasers, including "thresholdless" lasing or lasing without inversion, reduced intensity noise, and narrower linewidths[6,7,8,9]. Thus, the VCSEL is the forerunner of microcavity lasers that have potentially exciting effects.

## 1.3 Long Wavelength VCSELs

Although the first room temperature, CW operation of a GaAs-based VCSEL occurred more than five years ago [10], at this time room temperature CW operation has not occurred in the long wavelength InGaAsP material system. The long wavelength system faces challenges not seen in GaAs, including increased Auger recombination, lower material gain for a given carrier density, and lack of a mature, readily accessible epitaxial mirror growth technology. Despite these difficulties, progress has been made in long wavelength VCSEL research. To see how the progress was accomplished and to place the results of this dissertation into the proper context, this section describes the evolution of long wavelength VCSELs.

*Early work by Iga's group*

Fifteen years ago, Keniichi Iga and co-workers at the Tokyo Institute of Technology first discussed their idea for a semiconductor laser which emitted light perpendicular to the surface of the substrate. In that paper[11], the authors described the first long wavelength VCSEL which was composed of an InGaAsP double heterostructure grown by LPE, had a 90 $\mu$m long cavity and used two metal reflectors. It lased under pulsed conditions at 77 K with a threshold current of 0.9 A. This is 2-3 orders of magnitude higher than the current room temperature, CW thresholds of GaAs VCSELs! No work on long wavelength VCSELs was reported by groups outside of the Tokyo Institute of Technology for the next decade. This may have been a measure of the severity of the problem in the long wavelength system, as several groups were working on GaAs VCSELs during that

period. During that time period, Iga's group made several improvements on their initial structure, including the use of a shorter cavity to decrease free carrier and diffraction losses[12], the introduction of multilayer dielectric[13] and epitaxial mirrors[14] for higher reflectivity, and the implementation of a buried heterostructure for better current confinement[15]. One interesting note from this work is that the total growth time of the first InP/InGaAsP mirror[14] grown at Tokyo Institute of Technology was only 90 seconds[16]!
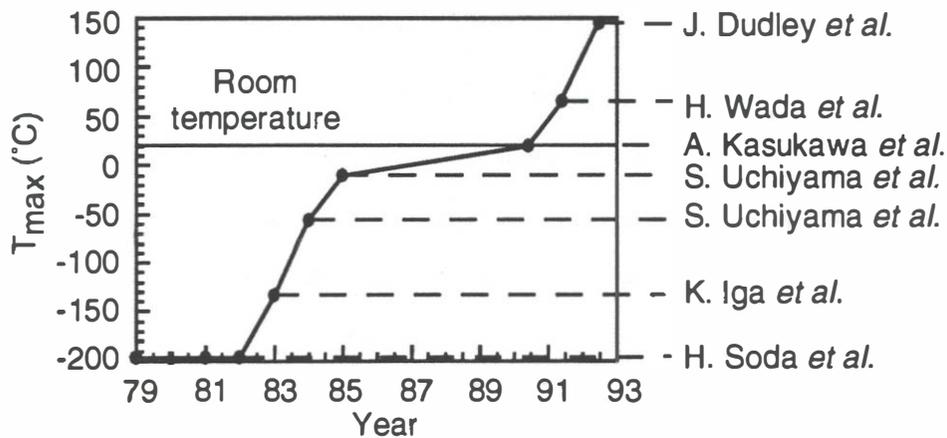


**Fig. 1.2** Maximum operation temperature, $T_{max}$, achieved in a 1.3 or 1.55 μm wavelength VCSEL.

*Room temperature operation*

Figure 1.2 shows the increase in maximum operation temperature of long wavelength VCSELs as the device technology has matured. The first room temperature, pulsed operation of a long wavelength VCSEL was reported by Kasukawa *et al.* at the 1990 Device Research Conference in Santa Barbara[17]. This

device used an MOCVD grown InP/InGaAsP mirror along with a Si/SiO2 mirror. Although our group at UCSB had achieved some success with an optically pumped device[18], we had not been able to achieve similar results with an electrically injected laser.

At the 1991 DRC, we reported the highest temperature operation to date (Fig. 1.2) of a VCSEL with a maximum operation temperature of 66 °C [19]. This etched well device employed two dielectric mirrors and utilized a hole etched in the substrate to form the short cavity[12,19]. Because of the improvement in the current confinement over that of Kasukawa's laser, the threshold current decreased from 225 mA to 50 mA, and the threshold current density decreased from 124 kA/cm$^2$ to 78 kA/cm$^2$. With the use of two dielectric mirrors, the device by necessity had two ring contacts as the electrodes. Further studies showed that the devices suffered from serious problems with non-uniform current injection[20] which could not be easily solved. We felt that to improve on these results would require a dramatic change in the research direction.

The year after we presented our results at the DRC, Tadokoro and co-workers from NTT presented their room temperature pulsed results using an InP/InGaAsP multilayer reflector and a Si/SiO$_2$ reflector enhanced with gold[21]. This device achieved the lowest threshold current density (21 kA/cm$^2$) reported to date (Fig. 1.3), but still had a very high threshold current of 260 mA. Around the same time, Kubota and colleagues at Tokyo Institute of Technology reported the first room temperature, pulsed operation from their group with an etched well structure [22].
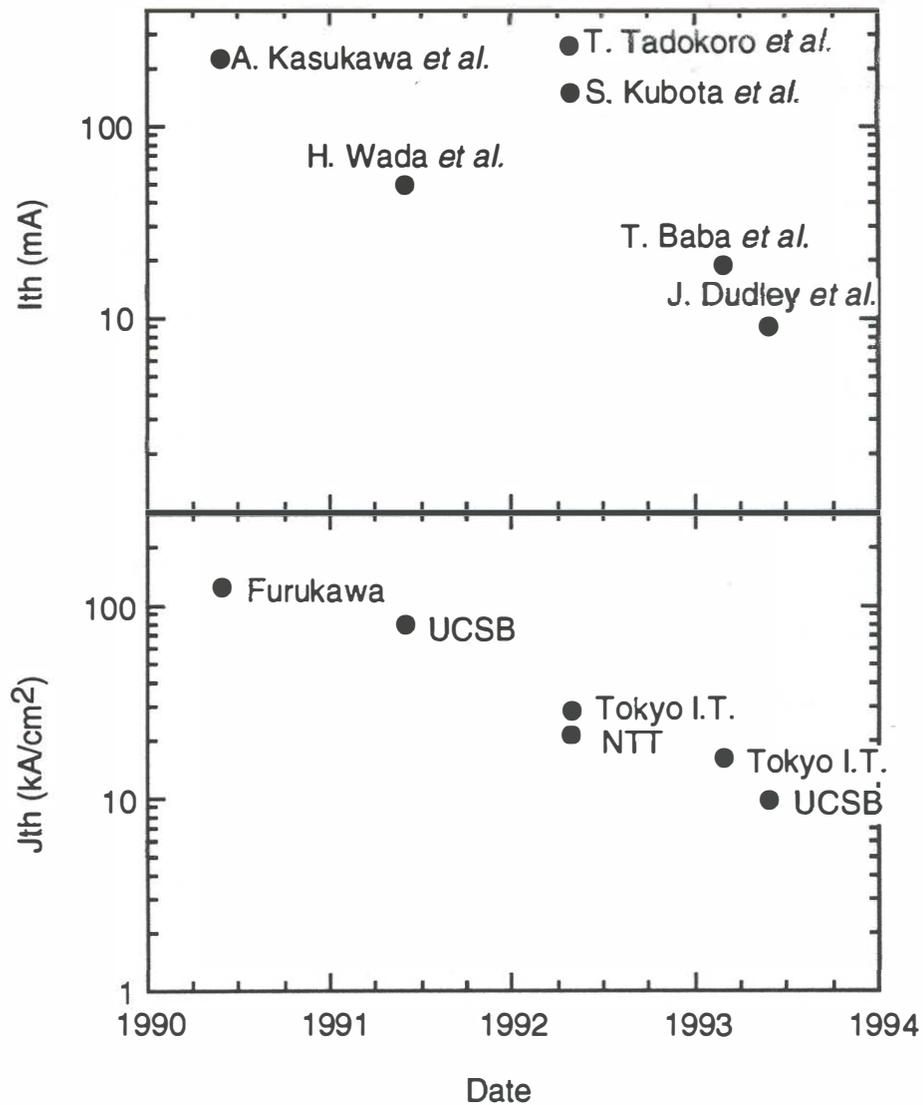
**Fig. 1.3** Minimum room temperature, pulsed threshold currents and threshold current densities achieved in 1.3-1.55 μm wavelength VCSELs.

In the fall of 1992, we reported the first results of our new research direction, namely combining *non-lattice matched* GaAs/AlAs mirrors with InP/InGaAsP laser structures[23]. This represented a dramatic change in the design and fabrication

of long wavelength VCSELs. The high reflectivity GaAs/AlAs mirrors allowed optically pumped, wafer fused VCSELs to operate at temperatures as high as 144 °C, which is the highest operation temperature of a long wavelength VCSEL at the date of this writing. The following spring, Baba and co-workers at Tokyo Institute of Technology reported record high temperature CW operation at 14 °C (57 °F) in an electrically injected, etched well device[24]. The etched well device used an optimized one-step LPE regrowth process in order to achieve low thermal resistance and more uniform current injection.

The same year at the DRC in Santa Barbara, I reported our first electrically injected, wafer fused VCSEL results. These lasers had a room temperature threshold current of 9 mA and threshold current density of 9 kA/cm$^2$ under pulsed operation[25]. These record low thresholds established the credibility of using wafer fusing to make long wavelength VCSELs.

## 1.4  Summary

This thesis looks at the critical problems in the development of practical, room temperature long wavelength VCSELs and demonstrates an effective solution to these problems. The increased Auger recombination, lower material gain, and lack of a mature epitaxial mirror growth technology have made the development of long wavelength VCSELs more difficult than that of (In)GaAs VCSELs. The lack of high reflectivity epitaxial mirrors at 1.3 and 1.55 μm wavelengths presents particularly onerous obstacles to the realization of these devices, as the choice of mirror affects the fundamental device design. Development of a readily achievable epitaxial mirror would address several basic issues, including those of current

crowding, active region heating, and optical loss. This dissertation studies these problems and presents a practical solution to them through the use of wafer fused GaAs/AlAs mirrors.

In particular, Chapter 2 discusses the design of quarter wavelength mirrors (QWMs) used in VCSELs. It addresses the issues of peak reflectivity, diffraction and absorption losses, and thermal resistance. The bandwidth and the peak reflectivity of a QWM can be related with a simple analytic expression which allows us to characterize various mirrors with a single parameter. This is applied to long wavelength VCSELs, where it is shown that GaAs/AlAs mirrors have wider bandwidths and higher reflectivities than the more common InP/InGaAsP mirrors. It is also shown that the thermal resistance of structures employing GaAs/AlAs mirrors are less than half of those using InP/InGaAsP mirrors or two dielectric mirrors, even when the structures are mounted epitaxial side down onto a heat sink.

Chapter 3 discusses the wafer fusing process in detail. It compares wafer fusing with other semiconductor bonding techniques. The chapter includes detailed characterization of the fused interface, including measurements of the optical, mechanical, and electrical properties of the interface. These measurements lead to a better understanding of the mechanisms involved in fusing and give important design rules for use when making fused devices. A model is proposed for the interactions occurring during fusing, which predicts the necessary conditions to achieve good fusing using other materials.

Chapter 4 summarizes the proof of concept experiment for the wafer fused VCSELs. The design of the optically pumped laser as well as the test set up are described. The results of the experiment, including room temperature

measurements, spectral and threshold measurements at high temperatures, and high speed measurements are detailed.

Chapter 5 describes the electrically injected, wafer fused VCSEL results. The design of the lasers is discussed, with particular emphasis on the effects on the device performance of heating in the active region and of detuning of the mirrors. The fabrication procedure including diagnostic testing is outlined. Next, the room temperature characteristics of the devices are studied, including the light-current-voltage characteristics, the polarization, the near field patterns, and the far field patterns. Finally, the temperature dependence of threshold current and the effects of non-uniform current injection are studied.

Chapter 6 summarizes the dissertation. Suggestions for further improvements in long wavelength VCSEL design are presented, and other opportunities for using and studying wafer fusing are suggested.

# References

[1]   Bardeen, J. and Brattain, W.H., *Physical Review*, vol. 74, 230, 1948.

[2]   Shockley, W., *Bell Systems Technical Journal*, vol. 28, 435, 1949.

[3]   Chang-Hasnain, C.J., Harbison, J.P., Zah, C.E., Maeda, M.W., Florez, L.T., Stoffel, N.G., and Lee, T.P., "Multiple Wavelength Tunable Surface-Emitting Laser Arrays," *IEEE Journal Of Quantum Electronics*, vol. 27, no. 6, 1368-1376, Jun 1991.

[4]   Willner, A.E., Chang-Hasnain, C.J., and Leight, J.E., "2-D WDM Optical Interconnections Using Multiple-Wavelength VCSELs For Simultaneous And Reconfigurable Communication Among Many Planes," *IEEE Photonics Technology Letters*, vol. 5, no. 7, 838-841, Jul 1993.

[5]   Maeda, M.W., Chang-Hasnain, C.J., Lin, C., Patel, J.S., Johnson, H.A., and Walker, J.A., "Use Of A Multiwavelength Surface-Emitting Laser Array In A 4-Channel Wavelength-Division-Multiplexed System Experiment," *IEEE Photonics Technology Letters*, vol. 3, no. 3, 268-269, Mar 1991.

[6]   Baba, T., Hamano, T., Koyama, F., and Iga, K., "Spontaneous Emission Factor Of A Microcavity DBR Surface Emitting Laser 2. Effects Of Electron Quantum Confinements," *IEEE Journal Of Quantum Electronics*, vol. 28, no. 5, 1310-1319, May 1992.

[7]   Yamamoto, Y., Bjork, G., Karlsson, A., Heitmann, H., and Matinaga, F.M., "Quantum State Control In Semiconductor pn-Junctions. II. Controlled Spontaneous Emission In Quantum Well Microcavity Lasers," *International Journal Of Modern Physics B*, vol. 7, no. 8, 1653-95, 1 April 1993.

[8]   Yamamoto, Y. and Slusher, R.E., "Optical Processes In Microcavities," *Physics Today*, vol. 46, no. 6, 66-73, Jun 1993.

[9]   Yamamoto, Y., "Lasers Without Inversion In Microcavities," *Japanese Journal Of Applied Physics, Part 2 (Letters)*, vol. 30, no. 12A, L2039-41, 1 Dec. 1991.

[10]  Koyama, F., Kinoshita, S., and Iga, K., "Room Temperature CW Operation Of GaAs Vertical Cavity Surface Emitting Laser," *Transactions Of The Institute Of Electronics, Information And Communication*, vol. E71, no. 11, 1089-90, Nov. 1988.

[11]  Soda, H., Iga, K., Kitahara, C., and Suematsu, Y., "GaInAsP/InP Surface Emitting Injection Lasers," *Japanese Journal Of Applied Physics*, vol. 18, no. 12, 2329-30, Dec. 1979.

[12] Motegi, Y., Soda, H., and Iga, K., "Surface-Emitting GaInAsP/InP Injection Laser With Short Cavity Length," *Electronics Letters*, vol. 18, no. 11, 461-3, 27 May 1982.

[13] Iga, K. and Uchiyama, S., "GaInAsP/InP Surface-Emitting Laser Diode," *Optical And Quantum Electronics*, vol. 18, no. 6, 403-22, Nov. 1986.

[14] Chailertvanitkul, A., Iga, K., and Moriki, K., "GaInAsP/InP Surface Emitting Laser (Lambda =1.4 µm, 77 K) With Heteromultilayer Bragg Reflector," *Electronics Letters*, vol. 21, no. 7, 303-4, 28 March 1985.

[15] Okuda, H., Soda, H., Moriki, K., Motegi, Y., and Iga, K., "GaInAsP/InP Surface Emitting Injection Laser With Buried Heterostructures," *Japanese Journal Of Applied Physics*, vol. 20, no. 8, L563-6, Aug. 1981.

[16] This LPE grown mirror incoporated 25 periods of InP/InGaAsP for a mirror centered at 1.4 µm. Growth time for the InGaAsP layers was 1.1 sec each, while growth time for the InP layers increased from 0.8 to 2.2 sec during the mirror growth. The measured peak reflectivity was 82 %.

[17] Imajo, Y., Kasukawa, A., Kashiwa, S., and Okamoto, H., "GaInAsP/InP Semiconductor Multilayer Reflector Grown By Metalorganic Chemical Vapor Deposition And Its Application To Surface Emitting Laser Diode," *Japanese Journal Of Applied Physics, Part 2 (Letters)*, vol. 29, no. 7, 1130-2, July 1990.

[18] Dudley, J.J., Melcer, L., Bowers, J.E., Hu, E., and Storz, F., "Surface Emitting GaInAsP/InP Lasers," *LEOS Annual Meeting Proceedings*, OE11.3, 1989.

[19] Wada, H., Babić, D.I., Crawford, D.L., Reynolds, T.E., Dudley, J.J., Bowers, J.E., Hu, E.L., Merz, J.L., Miller, B.I., Koren, U., and Young, M.G., "Low-Threshold, High-Temperature Pulsed Operation Of InGaAsP/InP Vertical Cavity Surface Emitting Lasers," *IEEE Photonics Technology Letters*, vol. 3, no. 11, 977-9, Nov. 1991.

[20] Wada, H., Babic, D.I., Ishikawa, M., and Bowers, J.E., "Effects Of Nonuniform Current Injection In GaInAsP/InP Vertical-Cavity Lasers," *Applied Physics Letters*, vol. 60, no. 24, 2974-2976, Jun 15 1992.

[21] Tadokoro, T., Okamoto, H., Kohama, Y., Kawakami, T., and Kurokawa, T., "Room Temperature Pulsed Operation Of 1.5 µm GaInAsP/InP Vertical-Cavity Surface-Emitting Laser," *IEEE Photonics Technology Letters*, vol. 4, no. 5, 409-11, May 1992.

[22] Kubota, S., Koyama, F., and Iga, K., "Low-Threshold GaInAsP/InP Transmission-Type Surface Emitting Laser," *Japanese Journal Of Applied Physics, Part 2 (Letters)*, vol. 31, no. 2B, L175-6, 15 Feb. 1992.

[23] Dudley, J.J., Ishikawa, M., Babić, D.I., Miller, B.I., Mirin, R., Jiang, W.B., Bowers, J.E., and Hu, E.L., "144 °C Operation Of 1.3 μm InGaAsP Vertical Cavity Lasers On GaAs Substrates," *Applied Physics Letters*, vol. 61, no. 26, 3095-7, 28 Dec. 1992.

[24] Baba, T., Yogo, Y., Suzuki, K., Koyama, F., and Iga, K., "Near Room Temperature Continuous Wave Lasing Characteristics Of GaInAsP/InP Surface Emitting Laser," *Electronics Letters*, vol. 29, no. 10, 913-14, 13 May 1993.

[25] Dudley, J.J., Babić, D.I., Mirin, R., Yang, L., Miller, B.I., Ram, R.J., Reynolds, T., Hu, E.L., and Bowers, J.E., "Low Threshold, Wafer Fused Long Wavelength Vertical Cavity Lasers," *Applied Physics Letters*, vol. 64, no. 12, 1463-5, 21 March 1994.

# Chapter 2
# **Mirror Design**

## 2.1 Choice of Mirrors

One of the most important choices to make in designing a VCSEL is that of what materials to use in the mirror. The device structure will be designed with this choice in mind, influencing such device properties as current injection efficiency and thermal resistance. The threshold current and resilience of the cavity mode to variations in growth thicknesses are also greatly influenced by the choice of mirror materials. In this chapter we discuss several different material combinations which have been used or proposed for long wavelength VCSEL mirrors. We discuss which of the material combinations is best under the criteria of reflectivity, bandwidth, and thermal resistance. To incorporate the mirror into a device design, we must take into account all of these criteria. We discuss trade-offs to achieve the best device design, concluding that the GaAs/AlAs combination is the best possible mirror for long wavelength VCSELs.
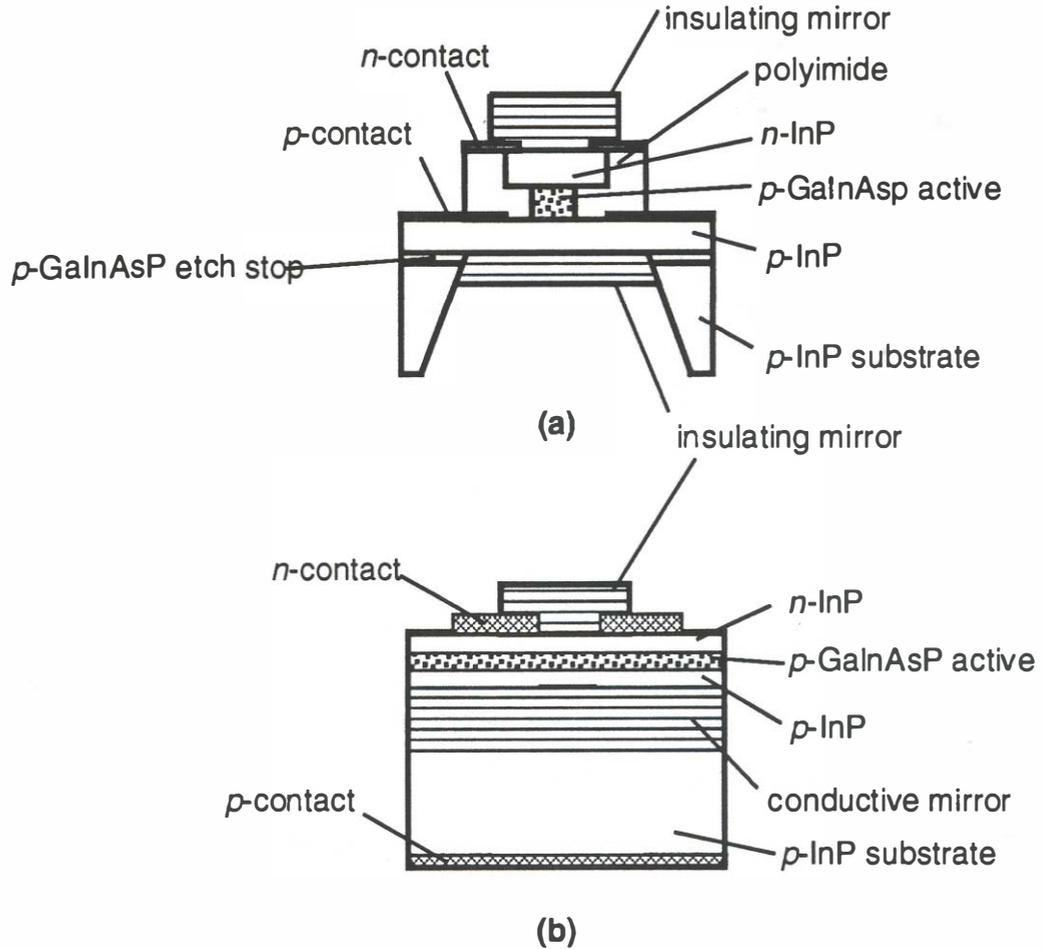
**Fig. 2.1** Common device structures for long wavelength VCSELs prior to the work done in this dissertation. Figure 2.1 (a) shows an etched well device which uses two insulating mirrors, and Fig. 2.1 (b) shows an epitaxial mirror device which utilizes one InP/InGaAsP mirror and one insulating mirror.

*Influence on Device Design*

The different materials which have been used in long wavelength VCSEL mirrors fall into two broad categories: those which are epitaxially grown and are electrically conductive[1], and those which are deposited (e.g. with e-beam

evaporation or reactive sputtering) and are electrically insulating[2]. I will refer to these two classes of mirrors as *conductive* and *insulating* mirrors. Using at least one conductive mirror in the device simplifies the device design and fabrication, as can be seen in Fig. 2.1. The top structure utilizes two insulating mirrors[3,4], and has historically been the most common structure. In order to form the short cavity in the structure, a hole is etched through the substrate down to an etch stop layer. This hole is typically 500 μm in diameter, while the cavity thickness is 3-5 μm. Thus, the devices are mechanically fragile and difficult to handle.

Current flow in structures using two insulating mirrors is also different from that of structures using at least one conductive mirror. Because current cannot be injected through the insulating mirrors, current must flow through thin distributed resistive layers into the active region. This causes problems with non-uniform carrier distributions which leads to poor overlap between the optical mode and the injected carriers and to spatial hole burning[5]. With the use of at least one conductive mirror, however, one can reduce the non-uniform carrier injection problem. In this case, current is injected directly through the mirror instead of through thin distributed layers, leading to more uniform current injection. This could also lower the resistance of the device. However, the mirror design and growth must be optimized in order to achieve this.

*Reflectivity*

The reflectivity of a quarter wavelength stack is a function of the complex dielectric constants of the materials used in the mirror. The common materials used for mirrors in 1.3 and 1.55 μm VCSELs include $\alpha$-Si, $SiO_2$, $Ti_2O_3$, InP, and

InGaAsP. Table 2.1 divides several possible materials into two groups: those used

in insulating mirrors (above the dotted line) and those used in conductive mirrors.

The loss in the low refractive index $SiN_x$, $SiO_2$, and MgO are assumed to be zero.

While there will always be some level of scattering loss in the films, the assumption

of no loss is reasonable because these films are usually combined with $\alpha$-Si layers

in insulating mirrors to achieve a small refractive index ratio. The loss in those

mirrors is dominated by the loss in the $\alpha$-Si layers. The loss in $Ti_2O_3$ was

extrapolated from measurements of a $Ti_2O_3/SiO_2$ mirror in which all of the loss was

assumed to be in the high index $Ti_2O_3$ layers.

| material | wavelength (μm) | refractive index | loss (cm$^{-1}$) | reference |
|---|---|---|---|---|
| $\alpha$-Si | 1.3 | 3.3 | 800 | 6,6 |
| $SiN_x$ | 1.3 | 2.0 | 0 | 7 |
| $SiO_2$ | 1.3 | 1.45 | 0 | 7 |
| $Ti_2O_3$ | 1.3 | 2.47 | 20 | 8,6 |
| MgO | 1.3 | 1.72 | 0 | 8 |
| GaAs | 1.3 | 3.41 | 10 | 9,10 |
| | 1.55 | 3.38 | | |
| AlAs | 1.3 | 2.91 | 10 | 9,10 |
| | 1.55 | 2.90 | | |
| InP | 1.3 | 3.20 | 10 | 11,10 |
| | 1.55 | 3.16 | | |
| InGaAsP ($\lambda_{gap}$ = 1.20 μm) | 1.3 | 3.42 | 10 | 11,10 |
| InGaAsP ($\lambda_{gap}$ = 1.42 μm) | 1.55 | 3.48 | 10 | 11,10 |

**Table 2.1** A listing of the optical properties of important materials used in making quarter wavelength stacks in long wavelength VCSELs.

One can calculate the peak reflectivity of a mirror with several different

methods, including scattering matrices and coupled wave theory. Corzine and

Yan[12] derived an analytic technique for calculating the peak reflectivity called the

hyperbolic tangent substitution method. They showed that for a stack of quarter- and half-wavelength thick materials, the amplitude reflectivity is given by

$$|\Gamma_N| = \frac{1-b}{1+b}, \text{ where } b \equiv \prod_{i=0}^{N}\left[\frac{n_{L_i}}{n_{H_i}}\right] \tag{2-1}$$

where $b$ is the product of the low-to-high index ratios at all of the interfaces in the DBR. The power reflectivity is given by $|\Gamma_N|^2$. For a quarter wavelength stack, $b$ can be expressed as

$$b = \left[\frac{n_{top}}{n_H}\right]\left[\frac{n_L}{n_H}\right]^{N-1}\left[\frac{n_L}{n_{bot}}\right] = \left[\frac{n_{top}}{n_{bot}}\right]\left[\frac{n_L}{n_H}\right]^{N} \tag{2-2}$$

In Equation (2-2), $n_{top}$ is the refractive index of the top surface (adjacent to the mirror stack); $n_{bot}$ is the refractive index of the bottom surface; and $n_L$ and $n_H$ are the high and low refractive indices of the materials in the mirror.
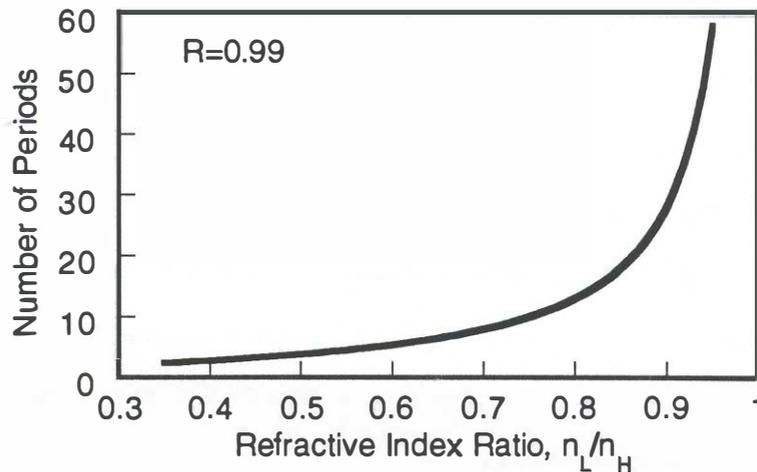


**Fig. 2.2** Number of periods required to achieve 99 % power reflectivity as a function of the ratio of refractive indices in the mirror. The incident medium is InP, and the bottom material is air. The mirror is assumed to have zero loss.

Using Eq. (2-2), one can compare different material combinations for mirrors. Figure 2.2 shows the number of periods needed to achieve 99 % reflectivity as a function of the ratio of low-to-high refractive indices. All of the insulating mirrors have a fairly small refractive index ratio ($n_L/n_H \leq 0.45$) which leads to 99 % reflectivity with fewer than 10 periods in all combinations. The insulating mirrors have the advantage that only a few periods are required to achieve the desired reflectivity. However, stress in the as-deposited films makes the practical realization of these mirrors a challenge. Stress causes problems with adhesion to the substrate and/or other previously deposited thin films (e.g. gold or polyimide). In extreme cases, the thin film stress may cause the membrane to break in the devices which utilize an etched hole. This places a lower limit on the practical thickness of etched hole devices. The electrically conductive mirrors (GaAs/AlAs and InP/InGaAsP) all have refractive index ratios close to 1.0. In all cases more than 15 periods are required to achieve 99 % reflectivity. Without including loss, we can already see that the InP/InGaAsP mirrors will not be practical at 1.3 µm. To achieve 99 % reflectivity, 40 periods or 7.9 µm of material are required. At a growth rate of 1 µm per hour, this corresponds to almost 8 hours of growth for a single mirror without active or cladding regions.

To get a better idea of actual reflectivities, we now include loss in the calculations. It is possible to find the loss in quarter wavelength mirrors without resorting to the use of numerical methods. For mirrors with little loss, we can express the reflectivity as

$$R = R_0(1 - A) \qquad\qquad (2\text{-}3)$$

where $R_0$ is the lossless reflectivity and $A$ is the absorptance. To find the absorptance, we use the known expressions[13,14] for mirrors with little loss. For the situation in which the first layer in the quarter wavelength mirror is the low index material we have

$$A_L = \frac{2\pi}{n_I}\left(\frac{k_L + \left(\frac{n_L}{n_H}\right)^2 k_H}{1 - \left(\frac{n_L}{n_H}\right)^2}\right) \tag{2-4}$$

where $k$ is the imaginary part of the refractive index of the material ($k = \frac{\alpha\lambda}{4\pi}$). For the situation in which the first layer in the mirror is the high index material, we have

$$A_H = \frac{2\pi n_I}{n_H^2}\left(\frac{k_L + k_H}{1 - \left(\frac{n_L}{n_H}\right)^2}\right) \tag{2-5}$$

For the insulating mirrors, the greatest reflectivity is achieved when the layer next to the cladding layer in a VCSEL is the low index layer. Thus, the absorptance is given by Eq. (2-4). For the conducting mirrors the greatest reflectivity is achieved when the layer next to the cladding layer is the high index layer. In this case, the absorptance is given by (2-5).

The error in using Eqs. (2-4) and (2-5) to find the absorptance can be estimated in this way. Because the threshold gain depends on $\ln(R) \approx 1-R$, it is most important to find the error in $1-R$. For the insulating mirrors with $n_L/n_H = 0.44$,

the error was less than 0.3 % for values of $k_i$ ranging from $10^{-4}$ to $10^{-2}$ (i.e. loss

from 10 to 1000 cm$^{-1}$ at 1.3 μm). For conductive mirrors, the maximum error

found from using Eq. (2-5) was less than 0.4 %. When the reflectivity of the

mirror is greater than or equal to 99 %, Eqs. (2-4) and (2-5) agree to within 1 % of

the exact analytic formula derived by Babić and Corzine[15]. Thus we see that there

is little loss in accuracy when using Eqs. (2-4) and (2-5) to find the absorptance.
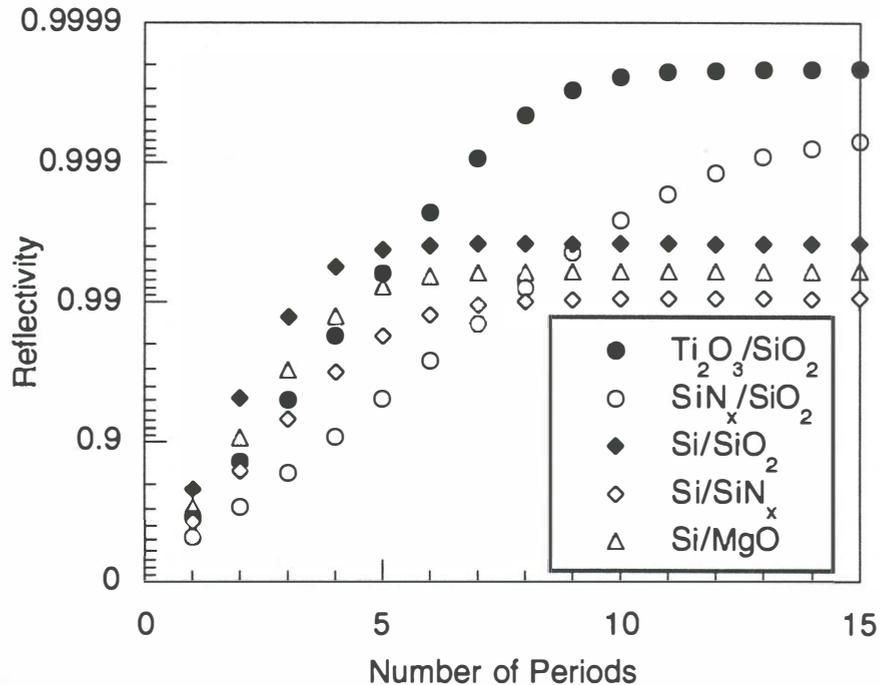


**Fig. 2.3** Achievable reflectivity for various insulating mirrors. Refractive index
and loss data come from Table 2.1. The incident medium is InP, and the bottom
material is air.

The reflectivity as a function of the number of periods for various insulating

mirrors is shown in Fig. 2.3. Because of the large refractive index of Si and the

small refractive index ratio in the Si/SiO$_2$ and Si/MgO mirrors, the reflectivity of these mirrors exceeds 99 % after only 5 periods. However, the large loss in Si (800 cm$^{-1}$ at 1.3 $\mu$m[6]) causes the reflectivity to saturate at its maximum value ($R_{max}$ = 99.5 % and 99.2 % for Si/SiO$_2$ and Si/MgO, respectively) on the sixth period. The Si/SiN$_x$ mirror suffers the most from the large loss in Si because of the relatively large refractive index ratio ($n_L/n_H$ = 0.6) and has a maximum achievable reflectivity of 99 %. The SiN$_x$/SiO$_2$ insulating mirror has small absorption loss but a large refractive index ratio ($n_L/n_H$ = 0.73). Because of the large ratio, these mirrors require 8 periods to achieve 99 % reflectivity and are theoretically expected to exceed reflectivities of 99.9 % when the number of periods exceeds 13. Practical realization of these mirrors is difficult, however, because of the stress in the layers. As the thickness of the film increases after the deposition of 6 or 7 layers, stress leads to the formation of cracks in the mirror, leading to increased scattering loss.

From Fig. 2.3, the best combination of insulating materials to use would be Ti$_2$O$_3$/SiO$_2$. These materials combine low loss with an $n_L/n_H$ < 0.6. Other groups have reported success in using this combination to form mirrors in long wavelength VCSELs[16]. However, the refractive indices used in the calculation[7,8] assume that the correct stoichiometry is achieved in the deposition of the layers. In practice this is difficult to achieve with Ti$_2$O$_3$. Measurements and analysis of Ti$_2$O$_3$/SiO$_2$ mirrors deposited at Hewlett-Packard Laboratories showed that the actual refractive index of Ti$_2$O$_3$ in the mirrors was 2.15 [6], compared to the value reported in the literature of 2.47 [8]. With the measured value of refractive index, the reflectivity achievable for an 8-period Ti$_2$O$_3$/SiO$_2$ mirror is only 99.7 %, compared to a comparable value of 99.6 % for a 5-period Si/SiO$_2$ mirror. Reflectivity is not the

only important parameter in choosing a mirror. As will be discussed later, the Si/SiO$_2$ mirror has twice the thermal conductivity of the Ti$_2$O$_3$/SiO$_2$ mirror. The clear improvement in thermal properties and ease of deposition of the Si/SiO$_2$ mirror outweigh the potential advantage in reflectivity of the Ti$_2$O$_3$/SiO$_2$ mirror.
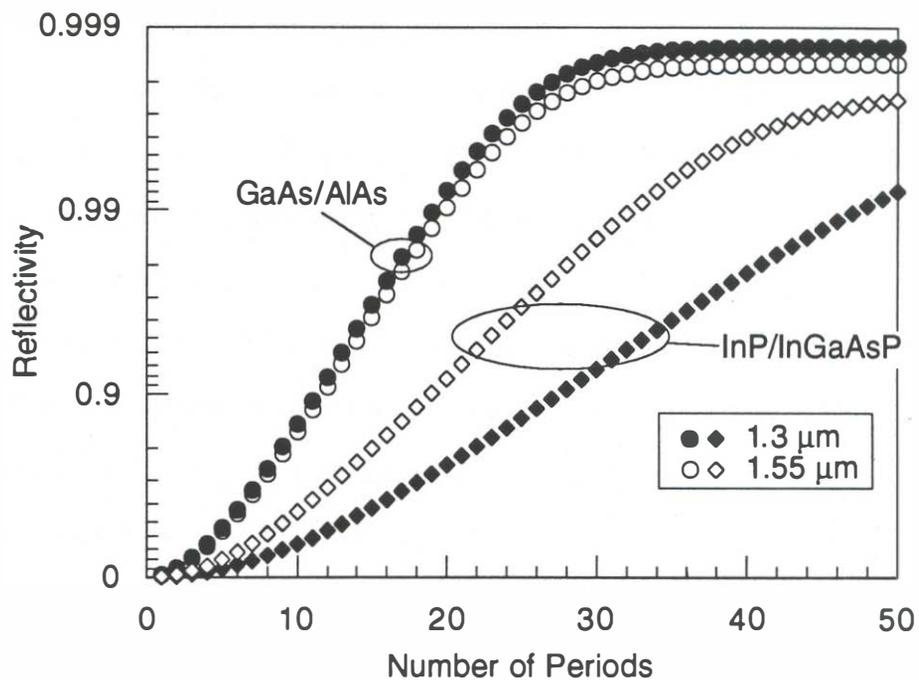


**Fig. 2.4** Achievable reflectivity for GaAs/AlAs and InP/InGaAsP mirrors at 1.3 and 1.55 μm wavelengths. The incident medium is InP, and the bottom material is the lattice matched substrate (GaAs or InP).

The reflectivity of conducting mirrors is plotted in Fig. 2.4. We see now that even at 1.55 μm, the refractive index ratio of InP and InGaAsP is so small that 33 periods are required to achieve 99 % reflectivity. This translates into approximately 8 μm of material. At typical growth rate of ≈ 1 μm/hour, this translates into an 8-

hour growth, a length of time which is not practical for most commercial applications. Aside from the length of the growth, the problems with maintaining lattice matching, maintaining quaternary alloy composition, and achieving a smooth surface morphology for this long of a growth are challenging at best.

If we want to make a device at 1.55 µm without arduous efforts at mirror growth, or if we want to make a device at 1.3 µm using a conducting mirror, we must look outside of the lattice matched InP/InGaAsP material system. Figure 2.4 shows that GaAs/AlAs mirrors achieve over 99 % reflectivity with 20 periods ($\approx 4$ µm) of material. Because of the refractive index dispersion, the reflectivity is slightly lower at 1.55 µm than it is at 1.3 µm in GaAs/AlAs mirrors for the same number of periods.

The first advantage of the GaAs/AlAs mirror combination over other semiconductor mirrors is the ability to achieve high reflectivity with half the thickness of material necessary to achieve the same reflectivity in the InGaAsP material system. Combined with the well-established MBE growth capability for GaAs/AlAs mirrors, this alone is reason to try making a long wavelength VCSEL with this system. However, there are more advantages to the GaAs/AlAs system as will be seen in the next sections.

*Coupling/Diffraction Loss*

The previous subsection has looked at the reflectivity of plane waves incident on the mirrors. A complete discussion of the reflectivity must include the effects of the mode shape on the observed reflectivity of the mirror. In the simplest case, the top mirror, cladding, and active layers are etched to provide a waveguide for the mode

in the VCSEL. The bottom layer is left unetched to provide improved thermal performance. However, this comes at the expense of no guiding and hence lowered modal reflectivity in the bottom mirror. The cavity mode which was guided in the active layer will diffract as it travels through the bottom mirror before returning back to the mirror/waveguide interface. Because the reflected mode has increased in size from the incident mode, the overlap between the incident and reflected mode will not be perfect, resulting in loss. The effects of this coupling or diffraction loss have been quantified by Dubravko Babić[17].

In Babić's paper, he compares the difference in diffraction loss between GaAs/AlAs mirrors at 1.3 μm wavelength and InP/InGaAsP mirrors at 1.55 μm wavelength. To find the reflectivity that the optical mode sees when traveling from a waveguide into the unguided mirror region, the plane wave reflectivity is decreased by the amount of diffraction loss

$$R_{modal} = R_0 (1 - \delta) \qquad\qquad (2\text{-}6)$$

In Eq. (2-6), $R_{modal}$ is the modal reflectivity, $R_0$ is the plane wave reflectivity, and $\delta$ is the fraction of the reflected beam which does not couple into the optical mode. The coupling loss is dependent on the exact mode shape.

The modal reflectivity for the q-TEM$_{00}$ mode from an InP waveguide reflecting off a GaAs/AlAs and an InP/InGaAsP mirror are shown in Fig. 2.5. For comparison, the plane wave reflectivities for both mirrors are also shown. To isolate the effects of diffraction loss, the absorption and scattering losses are neglected. Note that diffraction loss limits the use of unguided InP-based mirrors to diameters of 10 μm or larger. At a diameter of 5 μm, the highest reflectivity that

can be achieved is only 99 %, *without* taking into account the effects of absorption or scattering loss. Because of the low thermal conductance of the quaternary alloy, it is preferable to use the InP/InGaAsP mirror without forming a waveguide to allow heat spreading in the mirror layers. Thus, devices using InP-based mirrors must have diameters of 10 μm or greater.
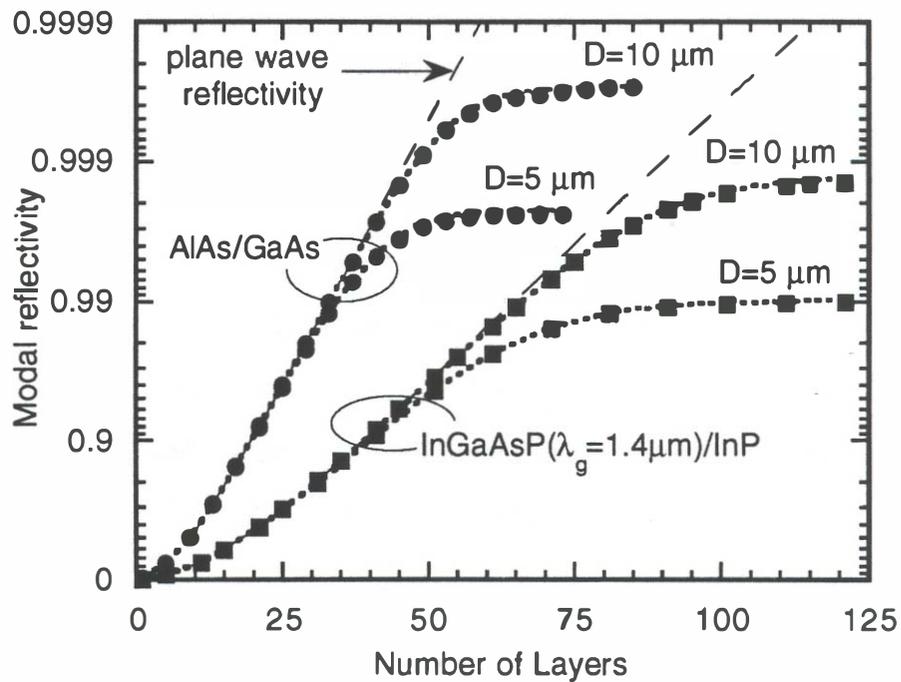


**Fig. 2.5** Modal reflectivity for GaAs/AlAs mirrors at 1.3 μm and for InP/InGaAsP mirrors at 1.55 μm.

For the GaAs/AlAs mirror, diffraction loss is not as large of a problem. For a device with a 5 μm diameter, 99.7 % reflectivity can still be achieved. As the device dimensions shrink from 5 μm, surface recombination and scattering loss due

to imperfect fabrication of sidewalls will probably present greater difficulties than coupling loss.

### Bandwidth

Another important property of quarter wavelength mirrors used in VCSELs is the optical bandwidth. In general, one would like a mirror with as large a bandwidth as possible. Wider bandwidth mirrors allow greater thickness variations in the mirror while still achieving the desired reflectivity at the center frequency of the Fabry-Perot cavity. This relaxes the growth requirements for thickness control in the mirrors. Wider bandwidth mirrors tend to have shorter penetration depths into the mirror, which decreases the effects of loss in the mirror on the achievable reflectivity. The shorter penetration depth also makes it easier to achieve single longitudinal mode operation. Finally, it is easier to tune the center frequency of the Fabry-Perot cavity when mirrors with large bandwidths are used.

The center frequency of the Fabry-Perot cavity can be found from

$$2\beta_m(L+2L_\tau) - 2\omega_0\tau = 2m\pi \tag{2-7}$$

where $\beta_m$ is the propagation constant for the mode, $L$ is the cavity length, $L_\tau$ is the penetration depth into the mirror, $\omega_0\tau$ is the phase change on reflection at a mirror, and $m$ is the mode index. For this discussion, I assume that the phase change is the same at both mirrors. The center wavelength can then be shown to be

$$\lambda_m = 2\pi n \frac{L + c\tau/n}{\pi m + \omega_0\tau} \tag{2-8}$$

where n is the refractive index in the cavity. Differentiation with respect to the cavity length gives

$$\frac{\partial \lambda_m}{\partial L} = \frac{2\pi n}{\pi m + \omega_0 \tau}$$

(2-9)

From Eq. (2-9) we see that to obtain the most sensitivity in the center wavelength, we want a small phase change on reflection. This happens with mirrors with the largest optical bandwidth.
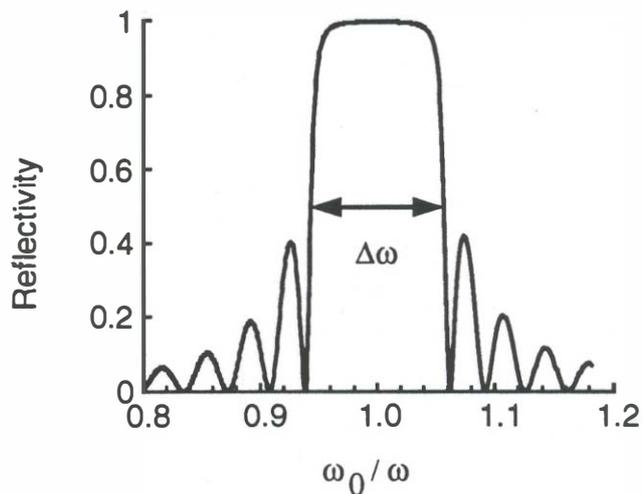


**Figure 2.6** Definition of fractional optical bandwidth, $\Delta\omega/\omega_0$.

It can be shown[13] that the bandwidth of a mirror is related to the refractive indices in the mirror by

$$\frac{\Delta\omega}{\omega_0} = \frac{4}{\pi} \sin^{-1}\left( \frac{1 - \frac{n_L}{n_H}}{1 + \frac{n_L}{n_H}} \right)$$

(2-10)

Figure 2.6 shows the definition of $\Delta\omega$. This is the frequency difference between the halfway points on either side of the mirror stop band. In VCSELs, however, only a portion of that stop band is usable. Because the mirror loss goes like $\ln(R) \cong$ 1-$R$, small changes in $R$ lead to large changes in threshold gain.

Notice that Eq. (2-10) expresses the bandwidth solely as a function of the ratio of refractive indices in the mirror. Comparing this with the relationship for the reflectivity of a lossless mirror, Eq. (2-1), we see that we can characterize both the bandwidth and the reflectivity of a mirror with a single characteristic of the mirror, mainly the refractive index ratio. We can find the number of periods necessary to achieve a given reflectivity, $N$ as a function of the bandwidth of the mirror

$$N = \frac{1}{2}\left( \frac{\log\left(\dfrac{1-R^{\frac{1}{2}}}{1+R^{\frac{1}{2}}}\right)}{\log\left(\dfrac{1-\sin\left(\dfrac{\pi}{4}\dfrac{\Delta\omega}{\omega_0}\right)}{1+\sin\left(\dfrac{\pi}{4}\dfrac{\Delta\omega}{\omega_0}\right)}\right)} - 1 \right) \tag{2-11}$$

Figure 2.7 shows this relationship for the mirrors discussed in this section with reflectivities of 99 and 99.9 %. For reference, the refractive index ratio is shown on the top axis. From this graph one can compare the maximum achievable reflectivity and the fractional bandwidth for a given set of materials (assuming the materials are lossless). Note that the insulating mirrors, all with refractive index ratios less than 0.75, tend to have fractional bandwidths from 20 to 50 %.

However, conductive mirrors where $n_L/n_H$ ranges from 0.85 to 0.95 have maximum bandwidths of just over 10 %. In particular, by using GaAs/AlAs mirrors instead of InP/InGaAsP mirrors, the bandwidth increases from 6 % to 10 %, allowing for more variation in growth thickness.
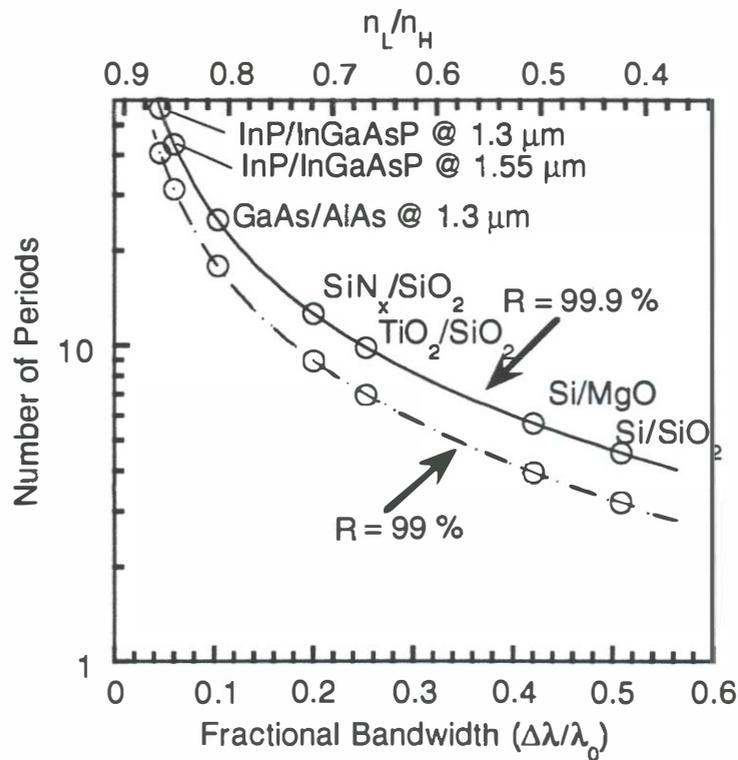


**Figure 2.7** Number of periods required to achieve 99 and 99.9 % reflectivity and the corresponding optical bandwidth for mirrors used in long wavelength VCSELs.

We can also include the effects of loss on the number of periods necessary to achieve a given reflectivity. Equations (2-4) and (2-5) give expressions for loss in a quarter wavelength stack [15]. To simplify the calculation, I have assumed that

the loss is distributed evenly throughout the mirror, i.e. $k_L = k_H = k*$. For the situation in which the first layer in the quarter wavelength mirror is the low index material we have

$$A_L = \frac{2\pi k^*}{n_I} \left| \frac{1 + \left(\frac{n_L}{n_H}\right)^2}{1 - \left(\frac{n_L}{n_H}\right)^2} \right| \qquad (2\text{-}12)$$

For the situation in which the first layer in the mirror is the high index material, we have

$$A_H = \frac{4\pi k^* n_I}{n_H^2} \left| \frac{1}{1 - \left(\frac{n_L}{n_H}\right)^2} \right| \qquad (2\text{-}13)$$

For bandwidths greater than 20 % (i.e. $p < 0.8$) the absorptance is given by Eq. (2-12). The absorptance is given by (2-13) for bandwidths less than 20 %.

Loss can be taken into account to relate the number of periods required to achieve a given reflectivity with the bandwidth of the mirror. To do this, we substitute $R'$ for $R$ in Eq. (2-11), where $R'$ is the transformed reflectivity given by

$$R' = \frac{R}{1 - A} \qquad (2\text{-}14)$$

The desired reflectivity is given by $R$, and the absorptance for a given loss, $k$, is found from Eqs. (2-12) and (2-13). This is shown in Fig. 2.8 for $R = 0.99$ and $R = 0.996$. For these plots I take the incident medium to be InP ($n_I = 3.2$). For

the conducting mirrors I assume that $n_H = 3.4$ in Eq. (2-13). This is a valid assumption for the cases of interest, as $n_H$ is close to the actual refractive indices of both InGaAsP (n = 3.42-3.48 ) and GaAs (n = 3.41).

Note that as the loss increases in the mirror layers, it is no longer possible to have a given bandwidth and reflectivity. These curves give a slight under estimate of the achievable reflectivity when the loss in one of the mirror layers is much greater than in the other, for example with mirrors which include Si. This is caused by the assumption that the loss in both layers of the mirror is the same. For most cases of interest, however, they serve as a useful method to compare different mirror designs.
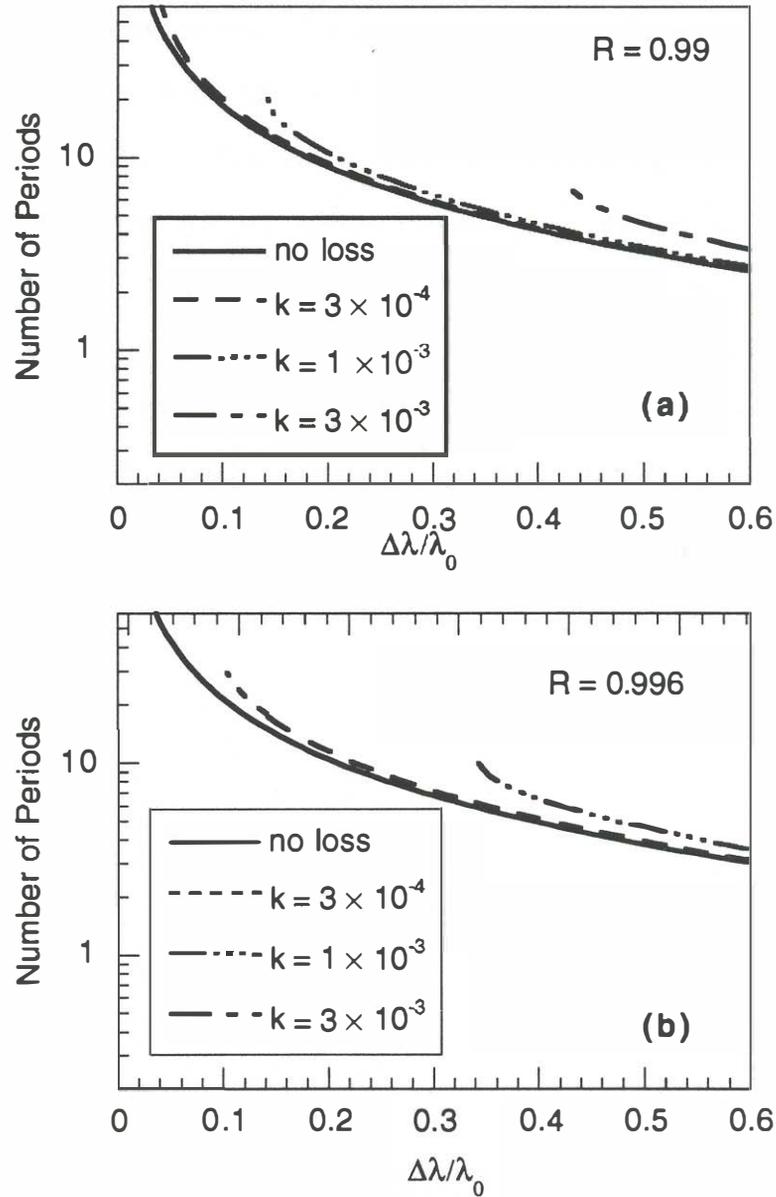
**Fig. 2.8** Number of periods required to achieve (a) 99 and (b) 99.6 % reflectivity and the corresponding optical bandwidth. The curves end abruptly when the loss becomes too high to achieve the given reflectivity and fractional bandwidth.

One can then plot the maximum achievable reflectivity as a function of the bandwidth for various amounts of loss as shown in Fig. 2.9. For small losses, the reflectivity is given by

$$R \equiv R_0(1-A) \tag{2-3}$$

As more periods are added to the mirror stack, $R_0$ approaches unity. Thus the maximum reflectivity is limited by the absorptance, or

$$R_{max} = 1 - A \tag{2-15}$$
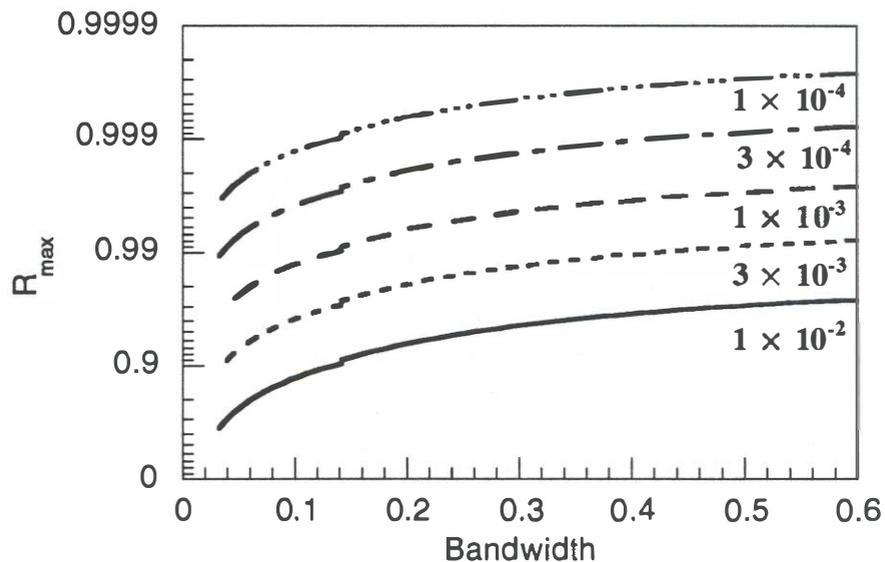


**Fig. 2.9** Maximum achievable reflectivity for a given refractive index ratio and corresponding bandwidth. The extinction coefficient ($k$) in the mirror layers varies from $1 \times 10^{-4}$ to $1 \times 10^{-2}$.

Figure 2.9 shows that in general reflectivities of greater 99 % can be achieved if the material loss is less than 30 cm$^{-1}$ at 1.3 μm. For insulating mirrors with

fractional bandwidths of greater than 40 %, losses up to 300 cm$^{-1}$ can be tolerated. However, large losses decrease the transmission efficiency through the mirror.

## 2.2 Thermal Properties

### Mirrors

The active layers in VCSELs can reach temperatures as high as 50 °C above the heat sink temperature18. In cooling off the active layer, most of the heat flow occurs either through or around the DBR mirror. Thus, it is important to employ a mirror which has the highest possible thermal conductance. In direct analogy to looking at a multilayer electrical system, we can find the thermal conductances both parallel (in the radial direction for cylindrical symmetry) and perpendicular (in the longitudinal direction) to the material interfaces in a multilayer mirror stack. For any system containing a periodic combination of two different materials with thicknesses $d_1$ and $d_2$, the radial and longitudinal thermal conductances are given by

$$\kappa_r = \frac{\kappa_1 d_1 + \kappa_2 d_2}{d_1 + d_2} \qquad\qquad (2\text{-}16)$$

$$\kappa_z = \frac{\kappa_1 \kappa_2}{d_1 \kappa_2 + d_2 \kappa_1}(d_1 + d_2) \qquad\qquad (2\text{-}17)$$

The thermal conductance of each material is given by $\kappa_i$ and the thickness of each material is given by the $d_i$. By definition, the thickness of each layer in a quarter wave mirror is given by $di = \lambda/4n_i$. By substituting this in for the thicknesses in the equations above, one can find the thermal conductance of the quarter wave

mirror knowing only the refractive indices and the thermal conductances of the constituent layers.

$$\kappa_z = \frac{\kappa_1 \kappa_2}{\kappa_1 n_1 + \kappa_2 n_2}(n_1 + n_2)$$

(2-18)

$$\kappa_r = \frac{\kappa_1 n_2 + \kappa_2 n_1}{n_1 + n_2}$$

(2-19)

The average thermal conductivity can be found by taking the geometric mean of the radial and longitudinal thermal conductivities.

$$\overline{\kappa}_{mirror} = \sqrt{\kappa_r \kappa_z} = \sqrt{\left(\frac{\kappa_1 n_2 + \kappa_2 n_1}{\kappa_1 n_1 + \kappa_2 n_2}\right)(\kappa_1 \kappa_2)}$$

(2-20)

Equations (2-18)-(2-20) are useful approximations which permit us to compare the thermal properties of different mirrors quickly and easily. In comparison with an exact result calculated using a two-dimensional thermal modeling program, the error in Eq. (2-20) was found to be as high as 20 %. However, these relationships are useful in that they allow us to compare the thermal conductances of different quarter wavelength mirrors using properties of the materials in the mirrors alone, without needing to know the extrinsic parameters such as the layer thicknesses or the exact device structure. They allow us to predict whether the mirror will act as a heat spreader ($\kappa_r \gg \kappa_z$) or if the mirror will allow heat to transfer through it.

From these relationships, we can compare the thermal properties of several different mirrors. Table 2.2 shows the radial, longitudinal, and geometric mean of the thermal conductances for several mirrors used in long wavelength VCSELs.

The thermal conductances of the individual layers are given in Table 2.3 and the refractive indices are given in Table 2.1. Tanobe *et al.*[8] first suggested using combinations of MgO and Si to form a DBR that would be thermally conductive. (Note, however, that the thermal conductivity of Si[19] quoted in Ref. 8 is two order of magnitude higher than the values used in these calculations[20,21], because the authors used the values for crystalline Si rather than $\alpha$-Si, as is used in the mirrors.) The thermal conductivity of the Si/MgO combination is about twice that of Si/Si$_3$N$_4$ and an order of magnitude higher than that of Si/SiO$_2$.

In comparison with the conductive mirrors, Si/MgO has about the same thermal conductivity as the InP/InGaAsP combination. However, the GaAs/AlAs combination has a higher thermal conductivity than both Si/MgO and InP/InGaAsP. Alloy scattering in the InGaAsP layers leads to a thermal conductance more than one order of magnitude lower than for any of the binaries. This leads to a thermal conductivity of the GaAs/AlAs mirror being more than three times greater than that of the InP/InGaAsP mirror. This has important implications in the thermal properties of devices using these mirrors, as will be discussed in the next section.

| Units of W/cm/K | $\kappa_z$ | $\kappa_r$ | $\kappa_{mirror}$ |
|---|---|---|---|
| Si/Si$_3$N$_4$ | 0.055 | 0.11 | 0.078 |
| Si/SiO$_2$ | 0.016 | 0.018 | 0.017 |
| Si/MgO | 0.070 | 0.40 | 0.17 |
| Si$_3$N$_4$/SiO$_2$ | 0.020 | 0.074 | 0.038 |
| TiO$_2$/SiO$_2$ | 0.008 | 0.009 | 0.009 |
| GaAs/AlAs | 0.61 | 0.69 | 0.65 |
| InP/InGaAsP | 0.09 | 0.38 | 0.18 |

**Table 2.2** Thermal conductivities (axial, radial, and geometric mean) for typical mirrors used in long wavelength VCSELs.

### Thermal Resistance of Devices

There are several important issues one must take into consideration when determining which device design to implement. In this section, we will discuss one of these issues, mainly the thermal resistance of the device. Complex models have been published[22] giving self-consistent solutions for the temperature and carrier profiles in VCSELs. However, none of them have addressed the issue of a fused VCSEL. In this section, I will concentrate solely on the thermal resistance of a given device structure and compare that structure with several other possible candidates. The thermal model will be used also to suggest improvements to the fused VCSEL design.

In this section, I will compare various device structures: a wafer fused VCSEL with a top Si/SiN$_x$ mirror; an etched well structure with two Si/SiN$_x$ mirrors; and a device using one InP/InGaAsP mirror and one Si/SiN$_x$ mirror. The calculations are done with a two-dimensional Poisson equation solver originally written by Mitsuaki Shimizu[18]. This program solves the equation:

$$\frac{1}{r}\frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial r^2} + \frac{\partial^2 T}{\partial z^2} = \frac{\rho}{\kappa} \qquad (2\text{-}21)$$

where $\kappa$ is the thermal conductivity of the medium in W/(cm K), $T$ is the temperature in Kelvin, and $\rho$ is the amount of heat generated in the area in W/cm$^3$. The program solves the Poisson equation in cylindrical coordinates for arbitrary geometries, assuming that there is no angular dependence of heat flow. It employs a uniform mesh for placing the thermal conductivities and heat sources and calculating the local temperature. In these calculations, I assume that all of the heat is generated in the active region. This ignores the contributions of resistive heating in the mirror and cladding layers, yet still gives a reasonable comparison between devices.

Once the temperature distribution is known, we can find the thermal resistance $\Theta_{jc}$ through the relationship:

$$\Theta_{jc} = \frac{T_{max} - T_{hs}}{P} \qquad (2\text{-}22)$$

where $T_{max}$ is the maximum temperature in the device, $T_{hs}$ is the temperature of the heat sink, and P is the power dissipated in the device.

A schematic diagram of the device structure modeled using the thermal program is shown in Fig. 2.10. The devices are modeled as though they were mounted epitaxial side down. Thus, the boundary condition at the epitaxial side of the device is that the temperature is zero ($T = T_{hs} = 0$). The mirror reflectivities in each device are the same, thus taking into account the difference in thicknesses required to achieve the same reflectivity in different material systems.
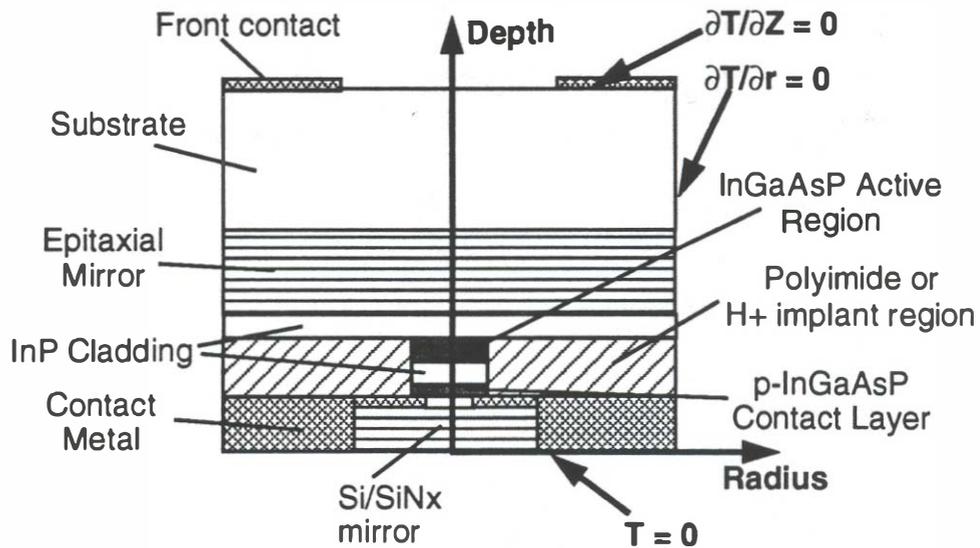
**Fig. 2.10** Schematic of device structure modeled in thermal resistance calculations.

Each device uses a 6-period $Si/SiN_x$ mirror next to the heat sink. The effects of convective cooling are ignored. This sets the boundary conditions at the top and side boundaries to

$$\left.\frac{\partial T}{\partial r}\right|_{r_{max}} = \left.\frac{\partial T}{\partial z}\right|_{z_{max}} = 0 \qquad\qquad (2\text{-}23)$$

The thermal conductivity of the mirror layers is taken as the geometric mean between the radial and longitudinal thermal conductivities as discussed in a previous section. The values for the thermal conductivities used in the calculations and their sources are shown in Table 2.3.

The selection of the grid spacing is important in order to get meaningful results from the program. An example of this is shown in Fig. 2.11. As we increase the number of grid points, the value for the thermal resistance converges on a single

answer. For more than 100 grid points, the error in the final answer is less than 5 %. The program is written so that if the grid points are placed symmetrically around a discontinuity in the thermal conductivity, an average value for the thermal conductivity is used at the discontinuity.
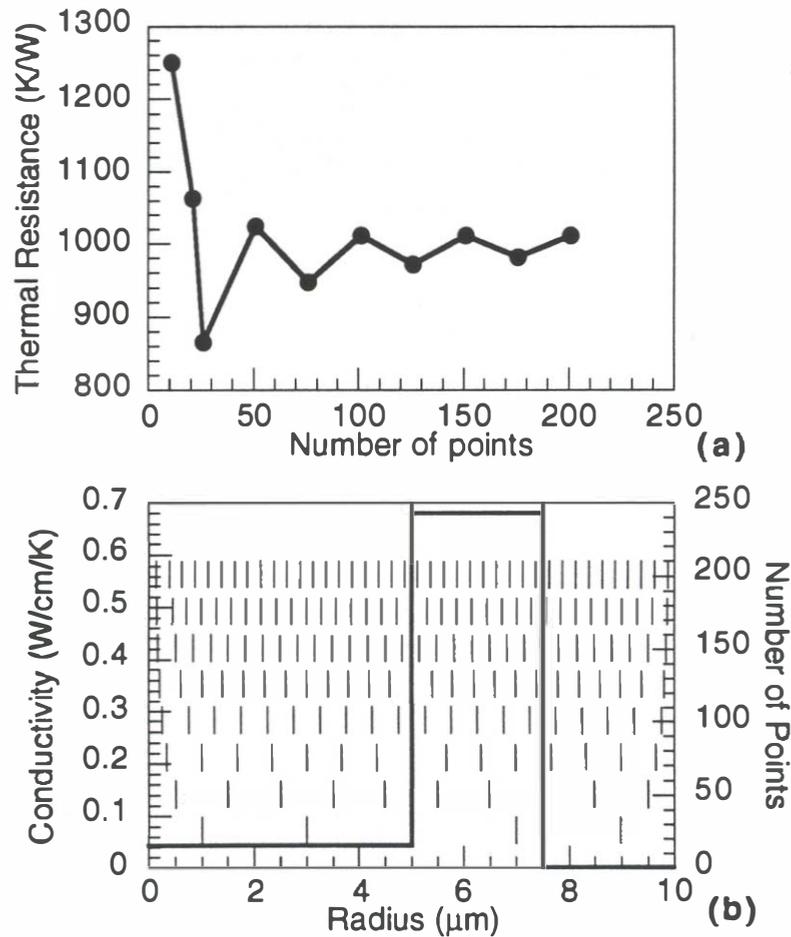


**Fig. 2.11** (a) Effect of grid spacing on the calculated thermal resistance for a given structure. The calculation approaches a single answer as the number of points increases. (b) Location of grid points in relation to a radial thermal conductivity step. Note that the grid points are spaced evenly around the step for 100, 150, and 200 points in this example.

The program converges to the correct answer as the number of points increases because the area around the discontinuity decreases. To ensure that the correct answer is obtained and to minimize the computation time necessary, the mesh points should be placed symmetrically around any thermal conductivity discontinuities [Fig. 2.11(b)]..

| Material | Thermal conductance, $\kappa$ (W/cm/K) | Reference |
|---|---|---|
| $\alpha$-Si | 0.026 | 21, 20 |
| $SiN_x$ | 0.16 | 23 |
| $SiO_2$ | 0.012 | 20 |
| $Ti_2O_3$ | 0.005 | 8 |
| MgO | 0.60 | 8 |
| InP | 0.68 | 24 |
| InGaAsP ($\lambda_{gap}$ = 1.15 $\mu$m) | 0.048 | 25 |
| InGaAsP ($\lambda_{gap}$ = 1.3 $\mu$m) | 0.043 | 25 |
| InGaAsP ($\lambda_{gap}$ = 1.42 $\mu$m) | 0.046 | 25 |
| InGaAsP ($\lambda_{gap}$ = 1.55 $\mu$m)s | 0.05 | 25 |
| GaAs | 0.44 | 26 |
| AlAs | 0.91 | 26 |
| polyimide | 0.0016 | 27 |
| gold | 3.18 | 28 |

**Table 2.3:** List of thermal conductivities used in the calculations in this chapter.

The thermal resistance of various device structures as a function of device radius is shown in Fig. 2.12. First notice structures A and C, the fused GaAs/AlAs structure and the etched well structures. Both structures use polyimide for current isolation. Because the GaAs/AlAs mirror allows heat flow through the top mirror more readily than the Si/SiN$_x$ mirror does, the fused structure has about 2/3 the thermal resistance of the more traditional etched well structure.
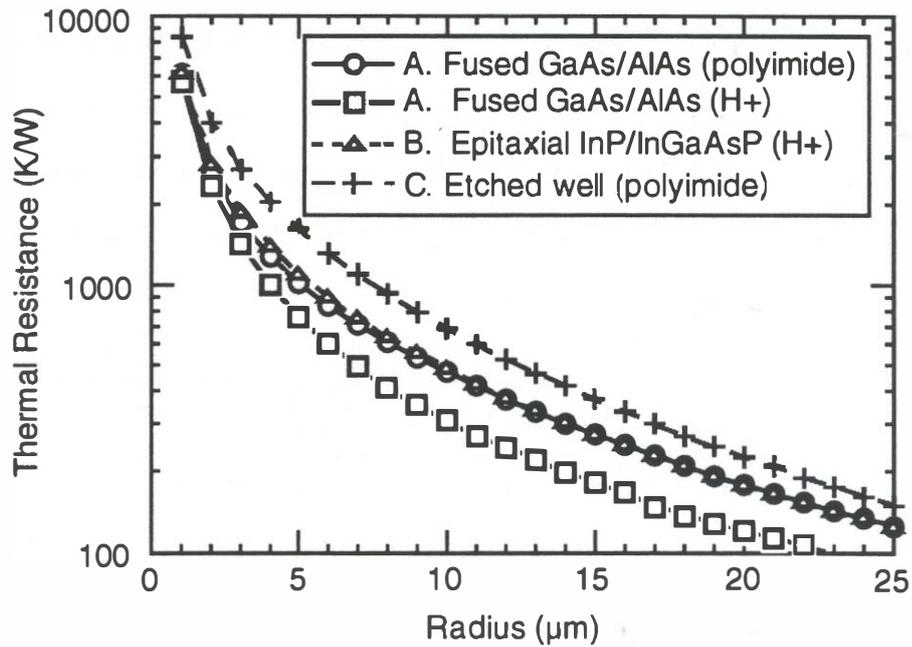
**Fig. 2.12** Calculated thermal resistances for various device structures. The method of current constriction used in each structure is given in parentheses, with H$^+$ designating proton implantation.

The thermal conductivity of polyimide is two orders of magnitude less than that of any III-V compound listed in Table 2.3. This suggests that one way to improve the thermal resistance of the devices is to replace the polyimide with a semiconductor. However, current confinement is important to improve the current injection efficiency. One way to confine current and improve the thermal conductivity of the structure is to use proton implantation. The effects of proton implantation on the thermal resistance of the fused structure is shown in lines A and A' of Fig. 2.12. Note the thermal resistance values are now half of the values for devices using polyimide. Because the best thermal resistance results come from using a proton implanted region, the rest of the devices compared all use this.

Now we can compare the other structure which has been traditionally employed in making long wavelength VCSELs, structure B which has an InP/InGaAsP mirror, with the fused structure, structure A'. The thermal resistance of the InP/InGaAsP structure using proton implantation is slightly *worse* than the fused structure using polyimide. This result is somewhat surprising considering that both structures are mounted epitaxial side down. In fact, another group[29] predicted that the thermal resistance of long wavelength VCSELs would be lower than that of the GaAs VCSELs due to the higher thermal conductivity of InP than GaAs. In that paper, the authors give an analytical expression for the thermal conductivity of a structure. However, their expression does not take into account heat spreading above the active layer. What our result shows is that the top mirror plays an active role in cooling the active layer by allowing heat to be removed through the mirror.

Besides the use of proton implantation, another method of reducing the thermal resistance in the fused VCSEL would be to replace the $Si/SiN_x$ mirror with another GaAs/AlAs mirror. The thermal resistance of this double fused structure is shown in line D of Fig. 2.12. This structure has the lowest thermal resistivity of all of the structures. It has about half of the thermal resistance of the single fused structure and one-quarter of the thermal resistance of the InP/InGaAsP structure. Work on making a double fused structure is an important direction for future research. This structure will be discussed in more detail in the final chapter.

## 2.3 Summary

This chapter analyzed the optical and thermal properties of mirrors used in long wavelength VCSELs. The mirrors were divided into two categories: those which

are insulators and those which allow electricity to pass through them. Analytic expressions were given to compare the different mirrors.

For a VCSEL, it is advantageous to have at least one conductive mirror. Based on the thermal and optical properties, mirrors made of GaAs/AlAs are the best choice for conductive mirrors at 1.3 and 1.55 $\mu$m. The advantages of GaAs/AlAs mirrors compared with InP/InGaAsP mirrors include the reduction in growth time and complexity to achieve the same reflectivity, the larger optical bandwidth, and the increased thermal conductivity of the GaAs/AlAs mirror. When comparing similar device structures using conductive mirrors, the GaAs/AlAs structure is expected to have half of the thermal resistance of the InP/InGaAsP structure.

The choice of an insulating mirror is not as simple. None of the mirrors are better than the rest in both optical and thermal properties. The $Ti_2O_3/SiO_2$ combination has the highest achievable reflectivities, but practical issues of stress of thick multilayer films and stoichiometry control still need to be addressed. These lead to lower achievable reflectivities because of increased loss and a decrease in the refractive index of the Ti layer, respectively. Measured $Ti_2O_3/SiO_2$ mirrors were only slightly higher in reflectivity than thinner $Si/SiO2$ mirrors, while the thermal conductivity of the $Si/SiO_2$ combination is twice that of $Ti_2O_3/SiO_2$. The thermal properties of Si/MgO mirrors are superior to any of the other insulating mirrors due to the high thermal conductivity of the MgO layers. However, the achievable reflectivity is less than that of $Ti_2O_3/SiO_2$ and $Si/SiO_2$. Thus, the choice of an insulating mirror to use in a VCSEL will depend on the exact structure chosen and the available resources for depositing the mirror layers.

One issue which was not addressed in this chapter is the ability to incorporate the GaAs/AlAs mirror with an InP double heterostructure. The lattice mismatch between the two material systems is 3.7 %, thus direct growth of the laser cavity on top of the GaAs/AlAs mirror would result in an active layer with too many defects. This issue will be discussed in the next chapter.

# References

[1]    Imajo, Y., Kasukawa, A., Kashiwa, S., and Okamoto, H., "GaInAsP/InP Semiconductor Multilayer Reflector Grown By Metalorganic Chemical Vapor Deposition And Its Application To Surface Emitting Laser Diode," *Japanese Journal Of Applied Physics, Part 2 (Letters)*, vol. 29, no. 7, 1130-2, July 1990.

[2]    Baba, T., Yogo, Y., Suzuki, K., Iga, K., and Koyama, F., "GaInAsP/InP Low-Mesa CPBH Surface Emitting Laser With An Optimally Deposited MgO/Si Multilayer Laser Mirror," *Japanese Journal Of Applied Physics, Part 1 (Regular Papers & Short Notes)*, vol. 32, no. 6A, 2692-4, June 1993.

[3]    Wada, H., Babić, D.I., Crawford, D.L., Reynolds, T.E., Dudley, J.J., Bowers, J.E., Hu, E.L., Merz, J.L., Miller, B.I., Koren, U., and Young, M.G., "Low-Threshold, High-Temperature Pulsed Operation Of InGaAsP/InP Vertical Cavity Surface Emitting Lasers," *IEEE Photonics Technology Letters*, vol. 3, no. 11, 977-9, Nov. 1991.

[4]    Baba, T., Yogo, Y., Suzuki, K., Koyama, F., and Iga, K., "Near Room Temperature Continuous Wave Lasing Characteristics Of GaInAsP/InP Surface Emitting Laser," *Electronics Letters*, vol. 29, no. 10, 913-14, 13 May 1993.

[5]    Wada, H., Babić, D.I., Ishikawa, M., and Bowers, J.E., "Effects Of Nonuniform Current Injection In GaInAsP/InP Vertical-Cavity Lasers," *Applied Physics Letters*, vol. 60, no. 24, 2974-2976, 15 Jun 1992.

[6]    Babić, D.I., "Measurement of Absolute Reflectivity on Metal and Dielectric Mirrors," April 1993, Unpublished.

[7]    Philipp, H.R., "Optical Properties of Silicon Nitride," *Journal of the Electrochemical Society*, vol. 120, no. 2, 295-300, 1973.

[8]    Tanobe, H., Oshikiri, M., Araki, M., Koyama, F., and Iga, K., *A Preliminary Study on MgO/Si Multilayer Reflectors for Improving Thermal Conductance in Surface Emitting Lasers*, Laser and Electro-Optics Society Annual Meeting, 1992.

[9]    Afromowitz, M.A., "Refractive Index of GaAlAs," *Solid State Communications*, vol. 15, 59-63, 1974.

[10]   Koch, T., private communication.

[11] Henry, C.H., Johnson, L.F., Logan, R.A., and Clarke, D.P., "Determination of the Refractive Index of InGaAsP Epitaxial Layers by Mode Line Luminescence Spectroscopy," *IEEE Journal of Quantum Electronics*, vol. QE-21, 12, 1985.

[12] Corzine, S.W., Yan, R.H., and Coldren, L.A., "A Tanh Substitution Technique for the Analysis of Abrupt and Graded Interface Multilayer Dielectric Stacks," *IEEE Journal of Quantum Electronics*, vol. QE-27, no. 9, 2086-2090, September 1991.

[13] Macleod, H.A., *Thin-Film Optical Filters*. Bristol, England: Adam Hilger Ltd., 1986.

[14] Hemingway, D.J. and Lissberger, P.H., "Properties of Weakly Absorbing Multilayer Systems in Terms of the Concept of Potential Transmittance," *Optica Acta*, vol. 20, 85-96, 1973.

[15] Babić, D.I. and Corzine, S.W., "Analytic Expressions for the Reflecting Delay, Penetration Depth, and Absorptance of Quarter-Wave Dielectric Mirrors," *IEEE Journal of Quantum Electronics*, vol. QE-28, no. 2, 514-524, February 1992.

[16] Watanabe, I., Koyama, F., and Iga, K., "GaInAsP/InP CBH Surface-Emitting Laser With A Dielectric Multilayer Reflector," *Japanese Journal Of Applied Physics, Part 1 (Regular Papers & Short Notes)*, vol. 26, no. 9, 1598-9, Sept. 1987.

[17] Babić, D.I., Chung, Y., Dagli, N., and Bowers, J.E., "Modal Reflection of Quarter-Wave Mirrors in Vertical-Cavity Lasers," *IEEE Journal of Quantum Electronics*, vol. 29, no. 6, 1950-62, June 1993.

[18] Shimizu, M., Babić, D.I., Dudley, J.J., Jiang, W.B., and Bowers, J.E., "Thermal Resistance of 1.3 μm InGaAsP Vertical Cavity Lasers," *Microwave and Optical Technology Letters*, vol. 6, no. 8, 455-57, 20 June 1993.

[19] Maycock, P.D., "Thermal Conductivity of Silicon, Germanium, III-V Compounds and III-V Alloys," *Solid-State Electronics*, vol. 10, 161-168, 1967.

[20] Cahill, D.G., Watson, S.K., and Pohl, R.O., "Lower Limit to the Thermal Conductivity of Disordered Crystals," *Physical Review B*, vol. 46, no. 10, 6131-6140, 1992.

[21] Goldsmid, H.J., Kaila, M.M., and Paul, G.L., "Thermal Conductivity of Amorphous Silicon," *phys. stat. sol. (a)*, vol. 76, K31-K33, 1983.

[22] Nakwaski, W. and Osinski, M., "Thermal Properties of Etched-Well Surface-Emitting Semiconductor Lasers," *IEEE Journal of Quantum Electronics*, vol. 27, 1391-1401, 1991.

[23] Incropera, F.P. and DeWitt, D.P., *Fundamentals of Heat and Mass Transfer.* 1990, pp. A6-A8.

[24] Swaminathan, V. and Macrander, A.T., *Materials Aspects of GaAs and InP Based Structures.* Prentice-Hall, 1992.

[25] Both, W., Gottschalch, V., and Wagner, G., "Thermal Resistivity of GaInAsP Alloy. Experimental Results," *Crystal Research Technology*, vol. 21, no. 5, K85-K87, 1986.

[26] Adachi, S.I.E.I., *Properties of GaAs*, IEE Inspec Data.  IEE, 1991, pp. 46-49.

[27] *Soluble Polyimides for Microelectronics, Probimide 200 Series, Physical, Electrical and Chemical Properties*, Ciba-Geigy Corp., Hawthorne, N.Y.

[28] Joyce, W.B. and Dixon, R.W., "Thermal Resistance of Heterostructure Lasers," *Journal of Applied Physics*, vol. 46, no. 2, 855-62, 1975.

[29] Osinski, M. and Nakwaski, W., "Effective Thermal Conductivity Analysis of 1.55 μm InGaAsP/InP Vertical-Cavity Top-Surface-Emitting Microlasers," *Electronics Letters*, vol. 29, no. 11, 1015-16, 27 May 1993.

# Chapter 3
# **Wafer Fusion**

## 3.1 Bonding and Long Wavelength VCSELs

Integrating GaAs/AlAs mirrors with InP double heterostructures to take advantage
of the optical, electrical, and thermal properties of the conductive mirrors presents a
challenge, due to the 3.7 % lattice mismatch. Typical heteroepitaxy techniques
involve growth of buffers layers several microns thick[1]. Even with the buffer
layers, threading dislocations and high etch pit densities on the surface remain a
problem. The inclusion of a thick buffer layer inside the cavity would degrade the
optical properties of the VCSEL by increasing the scattering and diffraction loss and
thus increasing the required threshold current. The threading defects often seen in
heteroepitaxy also have severe implications for the reliability of devices which use
this technique. This chapter addresses the issue of selecting a method other than
heteroepitaxy to integrate the InGaAsP active region with the GaAs/AlAs mirror.

The material interface which results from the chosen method will be inside the
cavity of the VCSEL. Thus, the interface must meet stringent optical, electrical,

and mechanical criteria. There should be no scattering or absorption loss at the interface as this would increase the threshold of the VCSEL. The interface should be electrically conductive to allow current injection through the GaAs/AlAs mirror into the active layer. The bond between the two semiconductors should be strong so that it will not break when the materials are temperature cycled during subsequent device fabrication and testing. The interface should be abrupt, with no gaps or intermediate layers causing a decrease in the thermal conductance. Finally, as the device ages, the interface should be stable and not degrade the device performance.

The next part of this chapter will compare several different bonding techniques to see which ones produce interfaces which meet the criteria for making a long wavelength VCSEL. Then I will describe the wafer fusing technique in detail. I will look at the mechanical, electrical, and optical properties of the wafer fused interface. Finally, I will propose a model for the fusing process which takes into account the measured properties of the fused interface and suggests further experiments to better understand the fusing process.

## 3.2 Wafer Bonding Techniques

The field of wafer bonding encompasses several techniques, each of which combines two semiconductors to form a whole which could not be obtained by epitaxial growth or deposition, or which has superior properties to that obtained by growth or deposition. The field can be divided into five techniques: Si direct bonding, low temperature $Si_3N_4$ bonding, interfacial metal bonding, epitaxial lift-off, and wafer fusing. Each of these techniques has strengths which make them

appropriate for use in various applications. In this section, I will review each technique and look at what has been done with it. Then I will analyze each technique for its utility in making long wavelength VCSELs.

## Silicon Direct Bonding

Silicon direct bonding (SDB) was the first technique used to bond two semiconductors together without using an external glue or solder. The technique, which has patents[2,3,4] dating back to 1964, has applications including the preparation of semiconductor-on-insulator substrates, the fabrication of high power MOSFETs[5], and the integration of high power sensor arrays[6]. It is useful to examine SDB to understand the mechanics involved in wafer bonding on a macroscopic level.

The wafers enter the process having either a bare Si surface or an oxidized Si surface[7]. The wafers are cleaned in an inorganic acid solution (e.g. aqua regia) and dried. The surfaces of the wafers are placed into contact with each other. Although the wafers adhere to each other at room temperature, the fracture strength of the interface is much less than that of the bulk crystal. The fracture strength is the amount of pressure which must be applied perpendicular to the interface to pull apart the two wafers. To increase the bond strength, the wafers are heated to temperatures between 1000 and 1200 °C for one hour in an ambient of pure nitrogen or a nitrogen-oxygen mixture, and complete bonding takes place. After complete bonding is achieved, voids or interference fringes cannot be seen when viewing the interface of the two wafers with an infrared camera. At temperatures

below 1000 °C, some voids caused by evaporated water can be seen. No pressure is exerted on the wafers during the bonding process.

It is critical in this process that the wafer surfaces be mirror smooth in order to achieve self-adhesion. Thus care is taken in polishing to create smooth surfaces, and care is taken during later handling not to introduce any particulates. Because the introduction of particulates is particularly difficult to prevent, groups have gone to great lengths to avoid this occurrence. One group[8] even developed an elaborate holder which keeps the two wafers separated using Teflon spacers during the substrate etching and drying. The spacers are removed just prior to bringing the wafers into contact.

One way to make a VCSEL using SDB is to deposit a $Si/SiO_2$ mirror onto a Si substrate and a $SiO_2$ layer onto an InP double heterostructure. The two could be bonded together to form the VCSEL cavity. However, the high temperature involved in SDB would cause severe diffusion and melting problems.


*Low Temperature $Si_3N_4$ bonding*

A solution to the problems associated with the high temperatures of Si direct bonding is given by low temperature $Si_3N_4$ bonding[9]. The low temperature $Si_3N_4$ process is similar to SDB, except that the surface of each wafer is covered with hydrophilic $Si_3N_4$ prior to bonding the wafers.

The advantage of this technique is that strong bonds can be achieved at temperatures as low as 90 °C. One proposed application for $Si_3N_4$ bonding is to combine GaAs and/or InP based devices with Si circuitry. Because the bonding temperature is low, problems with thermal expansion coefficient mismatch are

reduced, and it is possible to bond a GaAs or InP structure onto a completed Si integrated circuit without further annealing the metal interconnects.

Low temperature $Si_3N_4$ bonding could be used to join an insulating mirror with the VCSEL cavity.  After etching the InP substrate, normal processing of the VCSEL would continue.  The resulting device would sit on a mechanically robust Si substrate and use two insulating mirrors.  Previous structures which used two insulating mirrors required a hole etched into the substrate to form the short cavity, which resulted in a fragile structure which was difficult to handle.

The proposed $Si_3N_4$ bonded structure would have improved thermal properties over an etched hole VCSEL.  However, the thermal properties of the $Si_3N_4$ bonded structure would not be as good as the properties of a device which utilizes a GaAs/AlAs or InP/InGaAsP mirror, because the insulating mirrors have the highest thermal resistances.  The $Si_3N_4$ device would suffer from the same non-uniform current injection problems which etched hole VCSELs have[10].  If it is desirable to utilize low bonding temperatures in device fabrication, the wafers must be heated for long times.  For example, at 90 °C, the reported bonding time is 1100 hours or 45 days[9].  At 300 °C the bonding process takes a less arduous 9 hours.


*Epitaxial Lift-off*

Several groups have used epitaxial lift-off (ELO), also known as van der Waals bonding, to bond thin films onto arbitrary substrates.  This technique takes advantage of the large ($>10^7$) differential etch rates between $Al_xGa_{1-x}As$ ($x \geq 0.6$) and $Al_xGa_{1-x}As$ ($x \leq 0.4$) to separate the desired thin film from the original host substrate[11].  The desired structure is grown with an additional AlAs layer which

acts as the sacrificial etching layer. A layer of Apiezon W[12] is applied on top of the wafer, and the wafer is placed in an etching solution (typically a dilution of HF). When the sacrificial layer is completely removed, the thin film floats in the etching solution and can be placed on a new substrate, including glass[13], Si[14], and InP[15]. The bonding takes place as the water leaves the region between the thin film and the substrate. Epitaxial lift-off can be done without the use of interfacial materials, but the best results appear to occur when there is a new material at the interface such as epoxy[13], $SiN_x$[16], or metal[14,17].

Several different structures have been made using this technique. Epitaxial lift-off has been used to integrate GaAs photodetectors with Si receiver circuitry[18]. It has been used to combine GaAs solar cells with more durable and less expensive host substrates[19]. It has also been used to combine GaAs MSM detectors with $LiNbO_3$ waveguides[20,21].

Epitaxial lift-off has the advantage that it is a room-temperature process. Thus, it is not necessary to worry about dopant diffusion during the bonding process. When a thermally conductive layer is used at the ELO interface (e.g. an abrupt thin-film-to-substrate contact or a metal layer), heat can easily be transferred from the thin film to the substrate.

Although the ELO interface appears abrupt on a macroscopic scale, a closer examination reveals a fundamental limitation to the use of ELO. A 20-140 Å amorphous layer forms at the interface between two semiconductors which are placed in direct contact using ELO[22,15]. This amorphous layer has been shown to cause scattering loss[15] and would degrade the optical and electrical properties of an ELO-bonded VCSEL.

*Interfacial metal bonding*

The application of a Pd layer to a surface prior to bonding has been used to improve the reproducibility of ELO[17]. This interfacial metal bonding has also been done with full thickness wafers using various metals including Pd[23], Au[24], and In[25]. After the metal deposition, the surfaces are brought into contact and the samples are heated to complete the bonding process. One substrate is then removed down to an etch stop layer, revealing a smooth surface.

This technique has been used to integrate InP detectors with GaAs substrates[23]. In this paper it was shown that inclusion of a metal layer between the two materials does not degrade the electrical characteristics of the bonded devices. Metal bonding has been used to incorporate GaAs surface-normal modulators with Si wafers[25] and to integrate AlGaAs emitters with Si substrates[24].

The advantage of interfacial metal bonding is that it can be done at relatively low temperatures ($\leq 430$ °C). The interfacial metal provides a low resistance path for current flow through the interface.

However, this technique cannot be used with VCSELs. Although the metal does not degrade the electrical properties of the devices, it does detract from the optical quality of the bonded interface. The metal layer is lossy and does not have a high enough reflectivity to act as a mirror in a VCSEL.

**Table 3.1** Comparison of different bonding techniques discussed in Section 3.2 for use in long wavelength VCSELs.

| Bonding method | Process | | Interface | | |
|---|---|---|---|---|---|
| | Reproducible | Low temperature | Abrupt | No optical loss | Electrically conductive |
| Desired for VCSEL | yes | yes | yes | yes | yes |
| Silicon direct bonding | yes | $\geq 1000\ ^\circ$C | no | unknown | no |
| Si$_3$N$_4$ bonding | unknown | yes | no | unknown | no |
| Epitaxial lift-off | yes | yes | no | no | no |
| Interfacial metal bonding | yes | $\leq 430\ ^\circ$C | no | no | yes |
| Wafer fusion | yes | $\leq 650\ ^\circ$C | yes | yes | yes |

*Wafer Fusion*

Wafer fusion is similar to Si direct bonding in that two wafers are placed in direct contact and heated to achieve a stronger bond than is possible at room temperature. In wafer fusion, however, the temperature (600-650 °C) is lower than that used in SDB, and pressure is applied to the wafers during the bonding process to keep them together. More detailed information on this technique will be given in the next section of the chapter.

Wafer fusion has been applied to several different problems. The original work, done by Liau and Mull[26,] demonstrated the rectifying characteristics of p-n junctions formed by bonding bulk InP-to-InP and InP-to-GaAs wafers. Lo and

co-workers[27] later used wafer fusion to form InP in-plane lasers on GaAs substrates, calling the technique "bonding by atomic rearrangement." More recently, wafer fusion has been used to bond GaAs wafers together for second harmonic generation[28] and to integrate transparent substrates with AlInGaP LEDs[29].

Wafer fusion is ideal for use in making long wavelength VCSELs. The fused interface allows current flow and there is no scattering or absorption of the optical field at the interface. The mechanical contact is uniform across the fused interface and no amorphous layer has been found at the interface. This indicates that heat should be able to flow across the interface without problem.

The drawback to using wafer fusion is that it is a high temperature process. This may lead to dopant diffusion in the material. Stress caused by the different thermal expansion coefficients of the bonded wafers may enhance diffusion near the interface.

## 3.3 Wafer Fusion Technique

In this section I will describe in detail the wafer fusion technique. I will use a model for bowing in the wafers to explore which material properties are important for bonding two arbitrary substrates and which can be ignored. Experimental results in fusing GaAs to InP will be related to the model. Finally I will discuss substrate etching. Substrate etching is included in this section because in device applications, the success of the bonding process is measured by the ability to leave a thin film on the host substrate, not in the ability to bond bulk wafers.

*Wafer Fusion Process*

The fusing process is shown schematically[30] in Fig. 3.1. After cleaning the wafers in solvents (TCA, acetone, and methanol) to remove any particulates and organic contaminants, the wafers are placed in an acid mixture such as buffered HF or dilute (1:3) $HCl:H_2O$ solution. This step is important to remove any native oxides which may inhibit the fusing process. The samples are then rinsed and placed into contact, epitaxial layer to epitaxial layer. The samples are placed into a fixture which applies a uniform pressure perpendicular to the fused interface. The fixture is loaded into a converted LPE furnace which is heated to a temperature between 600 and 700 °C in a $H_2$ ambient. The fixture is held at that temperature for 10 to 30 minutes. The samples are cooled to room temperature and the bonded wafers are removed from the fixture.

In the process outlined above, there are several important details to achieve good fusing. The surface quality of the wafers prior to placing them in contact is critical. The surfaces to be fused must be smooth and flat. Any organic or inorganic contamination, especially particulates, should be removed by carefully cleaning the wafers. Using flat, smooth, and clean wafers decreases the gap between wafers which must be filled by mass transport during the fusing process and minimizes the break through of the film caused by trapped particulates after substrate removal. When these criteria are met, adhesion can be achieved at room temperature with a weak bond strength. The wafers stay together under normal handling, but intentional efforts to pull the wafers apart can succeed with little effort.

Clean wafers and remove native oxides.

Fuse wafers together at 630 °C in H2.

Remove InP substrate. Process devices.
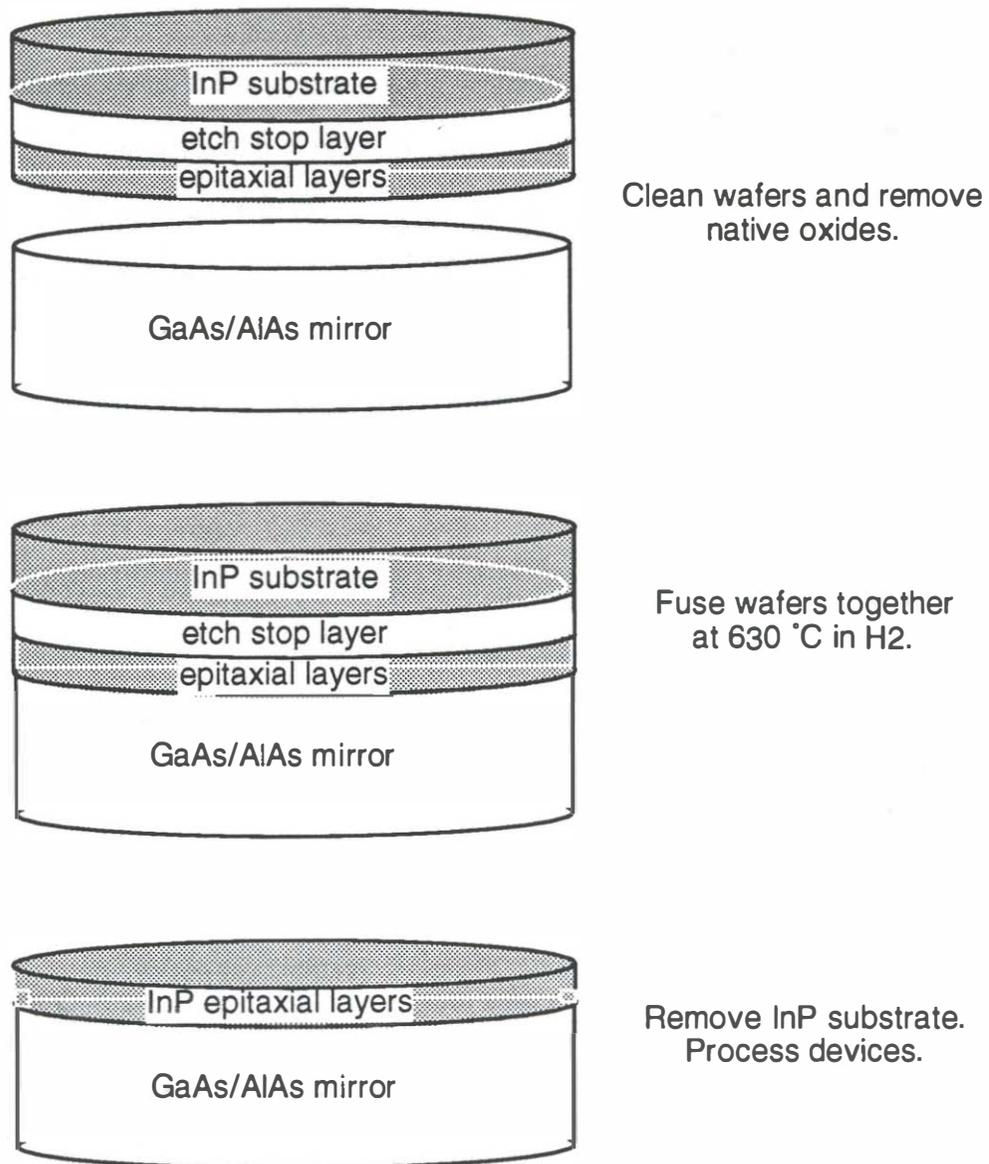
**Fig. 3.1** Flowchart for the wafer fusing process.

The presence of native oxides and dangling bonds at the wafer surface will also affect the fusing process. Different surface treatments were tried to remove the native oxides and passivate any dangling bonds, including an HF etch followed by

a DI water rinse, a buffered HF etch followed by a DI water rinse, and a $P_2S_5:(NH_4)_2S$ treatment followed by a DI water rinse. The HF treatment was adequate for bonding bulk substrates. However, if the sample to be bonded includes epitaxial AlGaAs layers, the HF will undercut the layers an undesirable amount. Buffered HF etch also gives good results without severe undercutting of the AlGaAs layers. A different approach to terminating the dangling bonds on the GaAs surface was to use a $P_2S_5:(NH_4)_2S$ treatment[31,32]. This gave good results for bonding, but the results were no better than those with buffered HF and the process was more time consuming.

Another important parameter in the bonding process is the pressure exerted on the wafers. The pressure must be uniform, large enough to flatten the wafers and place the samples in intimate contact, and small enough not to cause mechanical damage to the wafers. If these conditions are not met, fusing will occur only in selected parts of the surface or not at all. By placing different masses on top of the samples, I have observed that the GaAs and InP samples do not stick together when the pressure is less than or equal to 20 $g/cm^2$. Pressures of 400 $g/cm^2$ are sufficient to give good fusing. Intermediate pressures were not tried.

Finally, it is not clear what role the ambient gas in which the samples are fused plays. Lo *et al.*[27] and Wada *et al.*[33] suggested that the $H_2$ reacts with any remaining oxides at the interface to allow bonding between the InP and GaAs surfaces. This implies that the use of $H_2$ is necessary for achieving good bonding. However, we have shown that fusing can take place in a $N_2$ ambient, so it does not appear that $H_2$ is critical for the bonding process. More work needs to be done to see what affect, if any, the ambient gas has on the bonding process.

*Material Parameters*

Some of the material properties which are important to the fusing process can be found by looking at a model for bending in two wafers after cooling (after work done by Timoshenko[34]). The bowing in fused wafers is given by

$$\frac{1}{\rho} = \frac{6(\alpha_2 - \alpha_1)(T - T_0)(1+m)^2}{(t_1 + t_2)\left[3(1+m)^2 + (1+mn)\left(m^2 + \frac{1}{mn}\right)\right]} \tag{3-1}$$

where $\rho$ is the radius of curvature, $\alpha_1$ and $\alpha_2$ are the thermal expansion coefficients of the individual wafers, $T$-$T_0$ is the difference between the fusing temperature and the final temperature, $m$ is the ratio of the material thicknesses, $t_1/t_2$, and $n$ is the ratio of the Young's moduli for the two different materials. This equation is valid in the case where the combined thickness of the substrates is much less than the length and width of the substrates, which is the case for fusing most wafers. It is valid in regions away from the edges of the wafer, where one can neglect the effects of shear stresses on the wafers. The effects of the shear stresses will be discussed later in this section.

**Table 3.2** The thermal expansion coefficients, $\alpha$, and Young's moduli along the <100> crystal axis, $E_{<100>}$, for various III-V compounds[35]. The biaxial stresses and strains parallel to the substrate are related by $E/(1-v)$ for spherical bowing, where $v$ is the Poisson ratio.

| Compound | $\alpha$ ($10^{-6}/\,^{\circ}$C) | $E_{<100>}$ (dyne/cm$^2$) | $\left(\dfrac{E}{1-v}\right)_{<100>}$ (dyne/cm$^2$) |
|---|---|---|---|
| AlP  | 4.5  | 0.917 | 1.351 |
| AlAs | 4.9  | 0.935 | 1.333 |
| AlSb | 4.0  | 0.590 | 0.882 |
| GaP  | 4.5  | 1.028 | 1.481 |
| GaAs | 6.86 | 0.850 | 1.233 |
| GaSb | 7.75 | 0.632 | 0.920 |
| InP  | 4.75 | 0.606 | 0.947 |
| InAs | 4.52 | 0.514 | 0.794 |
| InSb | 5.37 | 0.409 | 0.633 |

Equation (3-1) reveals some of the intrinsic properties of the chosen materials which affect the internal stresses and the bowing of the wafers. We see that by choosing two materials with similar thermal expansion coefficients, there should be little bowing in the wafers after cooling. A plot showing how the ratio of Young's moduli affects the bowing in the fused sample is given in Fig. 3.2. When the wafers are of equal thickness, the ratio of Young's moduli does not play an important role in the macroscopic properties of the fused wafers. As thinner layers are bonded to the substrate, however, it becomes advantageous to have materials which have a small value of $n$. This gives the maximum radius of curvature and the smallest bowing. In addition to the thermal expansion coefficients and Young's moduli, the ability of the material to diffuse and fill in the gaps between the wafers via mass transport during the fusing process affects the area over which complete

fusing takes place.  The maximum congruent evaporation temperature of a material

places a lower limit on the fusing temperature, as will be discussed in Section 3.5.
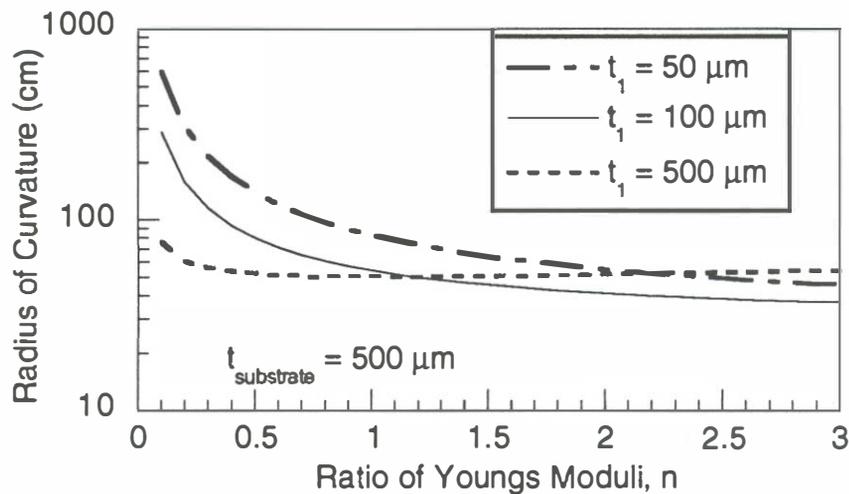


**Fig. 3.2**  The affect of the ratio of Young's moduli, n, on the radius of
curvature of the fused wafer after cooling.  The bottom wafer thickness is
500 μm, while the top wafer thickness is 50, 100, and 500 μm.  The thermal
expansion coefficient (TEC) difference for this example was $2.11 \times 10^{-6}/°C$ and
the temperature difference was 630 °C.  The plot can be scaled for different
material systems and bonding temperatures by noting that the radius of curvature
is inversely proportional to the TEC and the temperature differences.

While the previous paragraph described intrinsic properties of the materials, we

can control other parameters involved in wafer fusion.  The maximum temperature

and the rate of cooling affect the stress in the wafers and the ability to achieve

bonding over large areas.  From Eq. (3-1), the bowing can be decreased by

lowering the fusing temperature.  However at too low temperatures, the materials

do not bond together completely.  The temperature (for a given time) must be high

enough to allow mass transport to fill in the gaps at the interface.  In bonding InP to

GaAs wafers, we varied the temperature from 550 °C to 750 °C with fusion times ranging from 5 min. to 120 min. Fusing did not occur at temperatures below 600 °C. The lowest temperature at which reproducible results were obtained over the entire surface was at 630 °C. However, work by Wada *et al.* has shown fusing at temperatures as low as 450 °C, indicating that there may be some residual oxide on the surface in the fusing process described here.
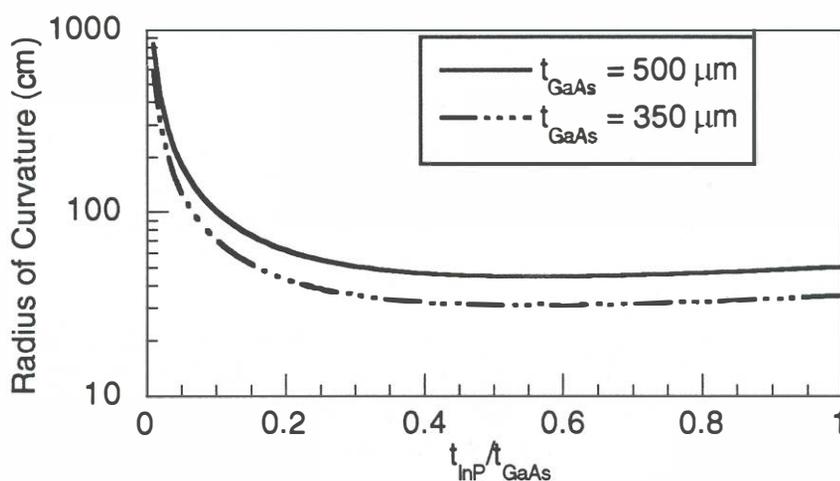


**Fig. 3.3** The calculated radius of curvature of an InP wafer bonded to a GaAs wafer as a function of the ratio of the wafer thicknesses. The GaAs thickness is held constant at 350 and 500 μm. The wafers are bonded together at 650 °C. All other parameters used in the calculation are found in Table 3.2.

Another important parameter which we varied was the cooling rate of the furnace. Samples which were cooled slowly (4 °C/min.) were found to bond more often than those samples which were allowed to cool quickly. This is probably due to the rapid increase of strain when the samples are cooled quickly.

In addition to the temperature profile, the substrate thickness ($t_1$ and $t_2$) or the ratio of the material thicknesses ($m$) will change the temperature induced stress. Figure 3.3 shows the radius of curvature of the fused wafers as a function of $m$ for two different thicknesses of GaAs substrate. Note that as the GaAs substrate becomes thicker, the bowing is decreased. Also, as the ratio of material thicknesses decreases, the bowing goes towards zero.
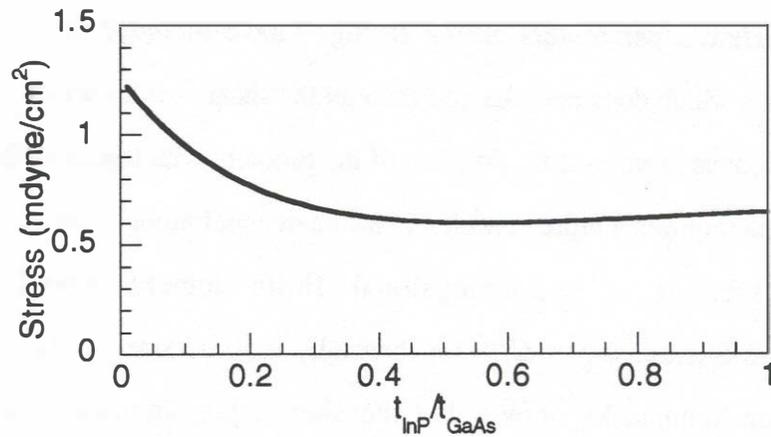


**Fig. 3.4** Stress near the center of fused InP-on-GaAs as a function of the ratio of InP thickness to GaAs thickness.

The maximum stress in the fused film *near the center* of the wafer can be estimated by looking at the stress due to the compressive forces and the stress due to bowing[34]

$$\sigma_{max,1} = \frac{1}{\rho}\left( \frac{1}{6ht_1}\left( t_1^3 E_1 + t_2^3 E_2 \right) + \left( \frac{t_1 E_1}{2} \right) \right) \tag{3-2}$$

where $\rho$ is found from Eq. (3-1), $h$ is the sum of the two layer thicknesses, and $E_1$ and $E_2$ are the Young's moduli of the materials. A plot of the calculated stress is shown in Fig. 3.4. Note that the stress near the center of the wafer is quite small. By thinning the wafer prior to fusing, one actually *increases* the maximum stress in the fused film away from the edges.

The area of the fused wafers which has the greatest problems with stress, however, lies at the edges of the wafers. In order to give a flavor for the effects of the different parameters on the fusing, I have included the above elementary analysis which does not take into account the shear stresses which play a major role at the edges of the wafer. Solution of the problem with the inclusion of these shear stresses requires a more complex two-dimensional model. These issues have been addressed in a two-dimensional finite-element model presented by Grupen-Shemansky *et al.*[36] for thermally induced stress in GaAs bonded to Si. Grupen-Shemansky shows that the shear stress increases by two orders of magnitude from the center to the edge of the wafer for wafers of the same thickness. Reducing the top wafer thickness to 26 % of the bottom wafer thickness reduces the shear stress to 70 % of the same-thickness value, while reducing the thickness ratio to 8 % reduces the shear stress 50 %. Also, tapering the top wafer edges before bonding reduces the stress at the edges more than one order of magnitude compared to a sample with cleaved edges. The results from Grupen-Shemansky's analysis suggest that further improvements can be made in the fusing process by thinning one wafer substantially before fusing and by beveling the edges of that wafer to reduce the stresses at the edges.

Handling such thin wafers during surface preparation for the wafer fusion process is nearly impossible. Thus, to gain the maximum benefit of using thinner wafers when fusing, it will be necessary to take a different approach to achieving a thin InP wafer before temperature cycling the wafers. This could be accomplished, for example, by a hybrid epitaxial lift-off and wafer fusing process, or by etching away one substrate after the wafers adhere at room temperature.

*Substrate Etching*

During the etching of the substrate, the thermally induced stresses in the bonded wafers are relieved. The etch rate determines the rate at which the stress is relieved. It is desirable to have as high an etch rate as possible to maximize the throughput, yet it must be slow enough to keep the change in stress from causing the wafers to fly apart. The greatest stress appears at the edge of the wafer where the etch rate is highest and the torque caused by the bowing in the wafers is greatest.

To reduce the edge effects, the edges of the wafer can be covered with wax. This will produce an I-beam shaped sample which has greater strength than an etched sample of uniform thickness throughout. This also prevents undercutting of the epitaxial layers at the edges of the sample. However, the areas that were protected by wax must be removed prior to device fabrication, leading to large loss of real estate.

Another method to prevent the InP wafer from delaminating during the etching is to decrease the concentration of etchant with time. This decreases the etch rate, making the stress relief rate more constant. This is not a quantitatively controllable

process using HCl:H$_2$O for the etchant, however, because the etch rate of InP in an HCl solution tends to change with time.
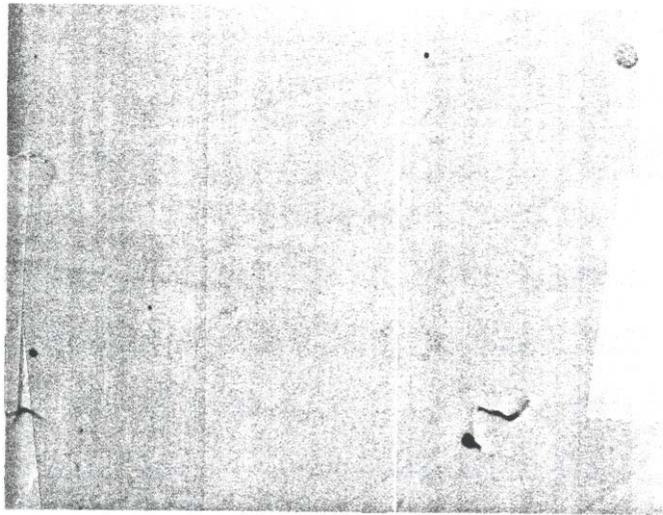


**Fig. 3.5** Surface of a fused wafer after removing the GaAs substrate. The magnification is 50 x.

## 3.4 Analysis of Fused Interface

In the previous section of this chapter, I described the mechanics of the wafer fusion technique. It is important not only to understand how to bond wafers, but also to understand how the bonded interface affects the finished device. In this section I will look at the important properties of the wafer fused interface that relate to the realization of long wavelength VCSELs. I will discuss the mechanical,

optical, and electrical properties of the fused interface.    Much of this
characterization was done by Rajeev Ram and co-workers at HP Laboratories, and
they deserve credit for the EBIC, AFM, reflectivity, and TEM studies[37,38,39].


*Mechanical Properties*

The first measurement of the success of the wafer fusion process is a mechanical
one.  We look to see if the wafers have stuck together and then remove the InP
substrate, stopping at an etch stop layer.  If the bonding worked well, there should
be a smooth surface on top of the sample which cannot be distinguished by eye
from an epitaxially grown film.  The surface of a bonded wafer after removing the
substrate should be flat, smooth, and without cracks (Fig. 3.5).

A more quantitative view of the wafer fused surface can be obtained by using
the atomic force microscope (AFM)[38].  The measured RMS roughness from a 10
$\mu$m x 10 $\mu$m scan of the surface is 3.8 nm.  This is similar to the measured RMS
roughness of the as-grown InP epitaxial layer prior to bonding to the GaAs
substrate.  Thus, the fusing process does not increase the roughness of the epitaxial
layer.    This is important for the realization of low optical-loss interfaces, as
increased surface roughness leads to higher scattering losses, which has been
shown in AlGaAs waveguides bonded to InP substrates via epitaxial lift-off[15].

To understand the bonding process better, it is important to look directly at the
interface.  A cross-sectional scanning electron micrograph of an InP wafer bonded
to GaAs is shown in Fig. 3.6.  The interface was studied across the entire cleaved
cross section and no voids were observed.  Thus, any gaps which existed after the
wafers were placed into contact have been filled in.  The exact mechanisms of this

process are discussed in the next section. The epitaxial layers remained smooth and well defined. There is a clear delineation between the InP and GaAs layers in the fused structure.
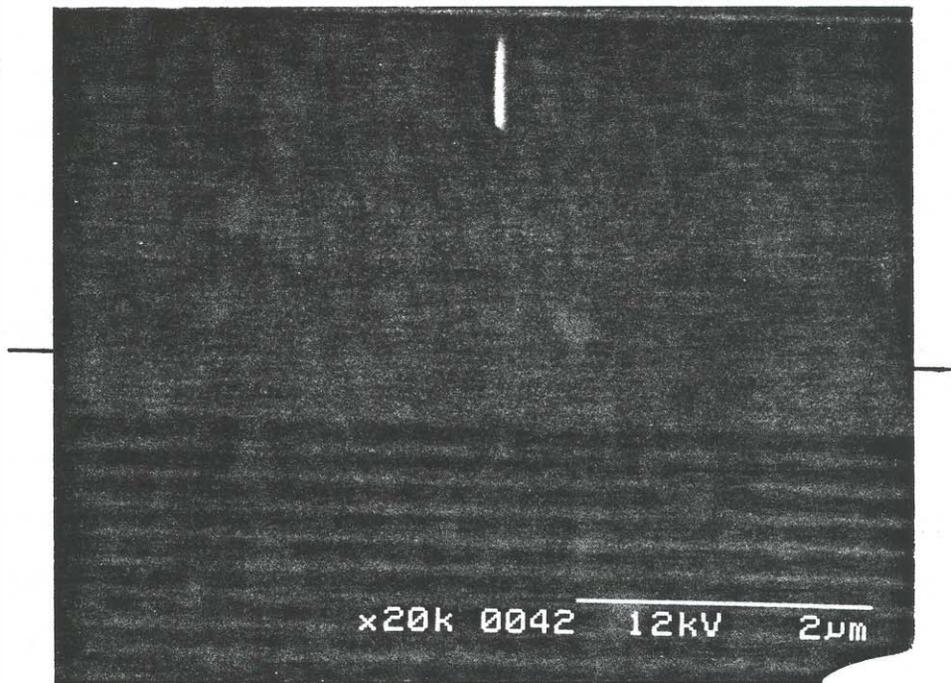


**Fig. 3.6** A cross-sectional scanning electron micrograph of a fused interface. Immediately above the black line on the sides is an InP layer, while below the lines is a GaAs layer. No voids are observed at the interface across the entire wafer.

A closer look at the interface can be obtained via the transmission electron microscope. TEM analysis of fused InP/GaAs interfaces have been undertaken independently by three different groups[38,27,33] with similar results in each study. S. J. Rosner[40] has looked in particular at the samples which have been fused with

the conditions used in this study. The cross sectional TEM images of all three

groups show abrupt interfaces, indicating that this property is inherent to the fusing

process and not a result of special processing techniques. Misfit dislocations occur

close to the interface indicating that all of the strain due to the lattice mismatch has

been relieved within 500 Å of the interface.
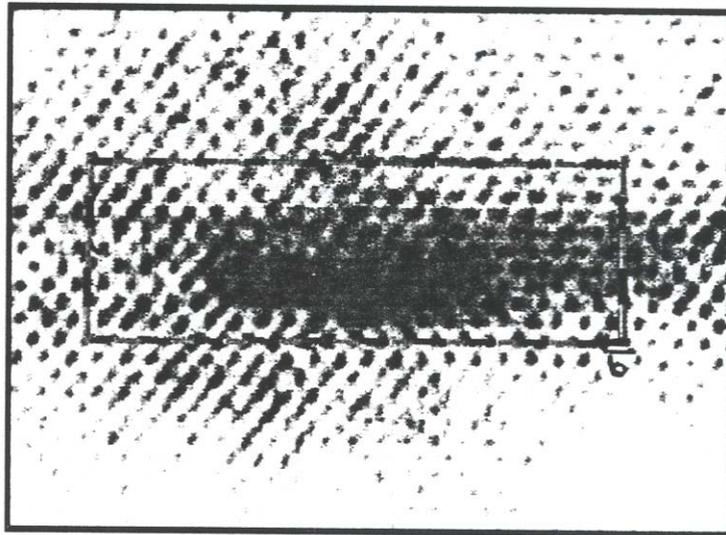


**Fig. 3.7** A cross-sectional transmission electron micrograph of a fused interface. The InP crystal is on top and the GaAs crystal is on bottom. A Burgers circuit is drawn around the fused interface.

The completion of a Burgers circuit around the interface (Fig. 3.7) shows that

the Burgers vector is parallel to the fused interface. This indicates that the

dislocations are mechanically stable edge dislocations. Because the strain which is

accommodated by a dislocation is the projection of the Burgers vector onto the

plane parallel to the fused interface, these edge dislocations are the most effective

dislocations at accommodating the strain caused by the lattice mismatch[41]. A

dislocation with its Burgers vector at an angle to the fused interface would have a

smaller projection onto the plane, resulting in less strain accommodation per dislocation. Had the Burgers vector been inclined towards the fused interface, the dislocations could easily move onto the slip planes and generate threading dislocations[42], which are known to cause catastrophic failure in laser operation. The mechanically stable edge dislocations found in this TEM analysis show promise for the lifetime properties of devices which utilize fused InP and GaAs.

Stacking faults and threading dislocations were not observed in the TEM study. Unlike other bonding processes (e.g. ELO), no amorphous layers were observed at the wafer fused interface. This indicates that the combination of the surface preparation prior to joining the wafers and the $H_2$ ambient used in the fusing are sufficient to remove any oxide layers from the surfaces of the wafers. However, some structures with a cross sectional diameter of 100 Å have been observed[39] near the fused interface, suggesting the formation of an InGaAsP alloy at the interface. The mechanism for this formation and why it is only seen rarely is discussed in the next section.
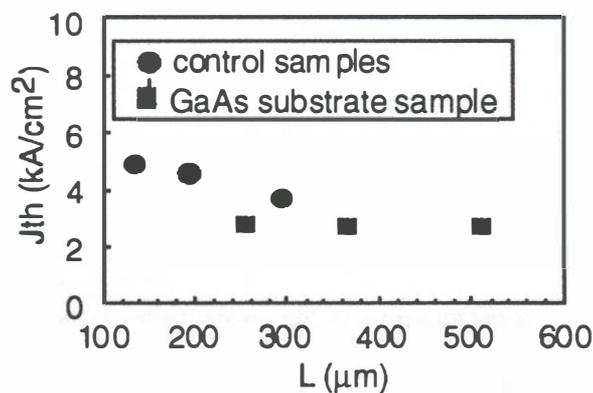


**Fig. 3.8** Threshold current density as a function of cavity length for InP lasers fused to GaAs substrates and for control samples on the original InP substrate.

*Electrical and Optical Properties*

In order to fully integrate a thin film device with its substrate, it is desirable to inject

current through the bonded interface. To test the fused interface, I compared a set

of in-plane lasers which had been fused to a GaAs substrate to the same lasers on

their original InP substrate. Figure 3.8 shows the threshold current density for the

fused and non-fused lasers as a function of cavity length. We see that wafer fusion

does not appear to alter the optical properties of the in-plane lasers or to introduce

non-radiative recombination centers which would increase the threshold current

density. The electrical properties of the fused wafers are also very good. From the

current-voltage curve shown in Fig. 3.9, we see that the reverse breakdown voltage

is approximately 7 volts. All of these measurements were made with the current

flowing through the fused InP/GaAs heterojunction. Thus the electrical properties

of the in-plane lasers do not appear to be degraded by the fusing process.
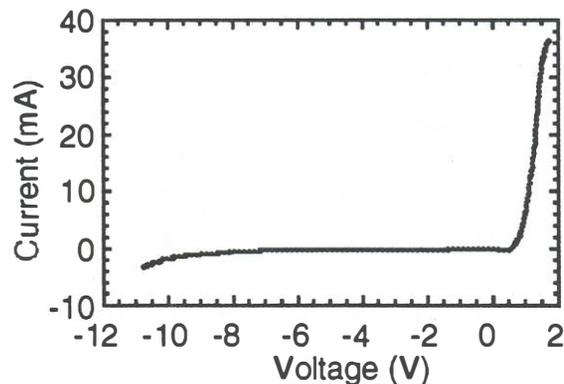


**Fig. 3.9** Room temperature, DC current-voltage characteristic for a fused in-plane laser.

A method for determining the effects of dislocations on the electrical properties

of the devices is to use electron beam induced current measurements (EBIC) of

fused p-InP/n-GaAs junctions[37]. The EBIC measurements are carried out in a scanning electron microscope, where the primary electrons are directed along the growth direction and rastered across the samples to acquire a two-dimensional image. The built-in field from the fused p-n junction sweeps out any electrons and holes locally generated due to the electron beam. An electrically active defect will cause the generated electron-hole pairs to recombine, leading to a reduction in the measured current.

When the carrier generation volume is centered at the fused interface, no voids are seen between the InP and GaAs over the entire fused area. When the accelerating voltage is approximately 13 keV, the carrier generation volume is centered at the fused interface and the beam diameter is approximately 700 nm. The average distance between dark lines in the EBIC scan is 4.5 µm, significantly less than what is expected for the heteroepitaxy of InP on GaAs. (The dark lines in the EBIC scans indicate electrically active dislocations, which should not be confused with dark line defects reported in laser electroluminescence studies.) Typical results for InP on GaAs heteroepitaxy show threading dislocation densities on the order of $10^{12}$ cm$^{-2}$ at the surface of the crystal after 8 µm of buffer layer growth. The distance between lines on a plain-view EBIC measurement is estimated to be 10 nm, which is below the resolution of the technique. This results in the EBIC images being dark, as most of the injected electrons recombine at the dislocations.

As the accelerating voltage in the primary electron beam changes, the carrier generation volume moves. As the carrier generation volume moved away from the fused interface, the spacing between dark lines increased, indicating a reduction in the defect density. Negligible defect densities were found 0.4 µm away from the

fused interface, indicating that fusing does not cause significant degradation in the InP more than 0.4 μm from the interface. In fact, this distance is an overestimate of the extent of the dislocations, because the carrier generation volume has a finite length perpendicular to the growth interface. Thus, when the carrier generation volume is centered at 0.4 μm from the interface, there is still recombination occurring at defects located closer to the interface.

An important property for the VCSEL is the mirror reflectivity. In order to look at the mirror properties after fusing, Ram and co-workers[37] measured the reflectivity spectra and transmission of a 10-period GaAs/AlAs mirror before and after fusing. The transmission through the mirror increased by 3 %, while the reflectivity decreased by the same amount. These results indicate that the fused interface does not introduce significant optical loss. The cause for the decrease in reflectivity and increases in transmission may be due to a change in the refractive index profile. This also explains the observed change in fringe spacing in the reflectivity spectra. The strain near the fused interface may enhance aluminum interdiffusion in the mirror, causing the proposed change in refractive index profile and the observed decrease in reflectivity and increase in transmission. Because the strain is localized near the interface, the addition of an extra $\lambda/2$ or $\lambda$ of GaAs in the first period of the mirror is sufficient to prevent the decrease in reflectivity[38].


## 3.5  Fusing Mechanism

Although the field of wafer fusing is nascent, enough data have been collected to propose a preliminary model of the physics involved in wafer fusing. In this section, I describe a model and use it to predict basic parameters for fusing

materials other than InP and GaAs. The model explains the existing data on fused interfaces, and further experiments can be made to confirm the validity of this model.

I will look first at the InP/GaAs material combination as an example for explanation of the model. When the InP and GaAs wafers are placed together, they touch at several points while gaps occur elsewhere between the wafers. At sufficiently high temperatures, mass transport takes place to allow the gaps to fill in. Thus, there are no voids between the InP and GaAs wafers as shown in the SEM, TEM and EBIC images. The rate limiting reaction in the "filling in" process is the dissociation of InP given by

$$In(s) + \frac{1}{2}P_2(g) \leftrightarrow InP(s) \tag{3-3}$$
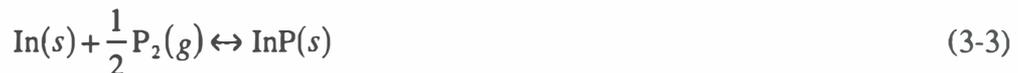
The equilibrium evaporation rate of $P_2(g)$ is almost 3 orders of magnitude higher than the evaporation rate of $P_4(g)$ and $In(g)$[43] at the temperatures involved in fusing, so we can neglect the evolution of $P_4(g)$ and $In(g)$. The GaAs wafer acts as an effective cap for keeping $P_2(g)$ near the InP surface, thus preventing the surface of the InP from decomposing. If the GaAs wafer were not an effective cap, the decomposition of InP would lead to the creation of metallic indium at the fused interface which would be observable in the TEM analysis and would cause noticeable optical losses at the interface.

Because the surfaces of the InP and GaAs wafers are not perfectly flat, voids exist between the two wafers when they are placed into contact at room temperature. The convex areas on the InP substrate have a greater surface energy

than the flat areas, leading to higher equilibrium vapor pressures on the convex surfaces[44,45]. Thus the reaction in Eq. (3-3) is driven from right to left resulting in a higher concentration of mobile In atoms on the convex surfaces than on the flat surfaces. The concave surfaces have less surface energy than the flat InP surfaces, leading to a smaller equilibrium vapor pressure and a smaller concentration of In atoms near the surface. This difference in In concentration leads to diffusion of the In atoms towards the concave surfaces.

Liau and Zieger[46] studied the mass transport of InP in a $PH_3$ atmosphere and measured the activation energy of the In diffusion to be 1.5 eV. Because of the availability of $P_2(g)$ in this experiment provided by the $PH_3$, the rate limiting mechanism was the diffusion of In atoms. Experiments by Hansen et al.[44] involving the mass transport of InP without the use of $PH_3$ showed a higher activation energy of 4.9 eV for the mass transport process. Hansen's results are in good agreement with his model which shows that the limiting mechanism in mass transport is the dissociation of InP given by Eq. (3-3). As the environment used in wafer fusing has no external source for $P_2(g)$, mass transport to fill in the gaps between the wafers can only occur once InP has dissociated, Eq. (3-3). After the InP has dissociated, In atoms are free to diffuse on the surface. Because the activation energy for the dissociation of InP is much higher than the activation energy for the diffusion of In atoms, the dissociation of InP is the rate limiting effect in wafer fusion, not the diffusion of In atoms as suggested by other researchers[27].

The InP is believed to play the major role in the mass transport as compared to the GaAs because of the lower energy required to cause evolution of the group V

element in the vapor phase in InP than in GaAs. Foxon *et al.* [47] have identified the species involved in the evaporation of InP, GaAs, and GaP as a function of temperature. They have identified two temperature regimes in the evaporation of these III-V compounds. At lower temperatures, the fluxes of the group III and V elements are approximately equal and congruent evaporation occurs. Above the maximum congruent evaporation temperature (CET), the group V element is the dominant element in the gas with vapor pressures much higher than those of the group III element. In all cases reported, wafer fusing has occurred at temperatures above the CET of at least one of the two wafers. Farrow and Foxon report congruent evaporation temperatures of 360 °C, 625 °C, and 675 °C for InP, GaAs, and GaP[43,47]. The lowest reported fusing temperature for InP and GaAs is 450 °C at a time of 30 min.[33] The only reported fusing temperature for GaAs bonded to GaAs is 840 °C[28]. This model suggests that it should be possible to fuse GaAs at temperatures near 700 °C, following the same trend as InP fusing.

The CET of GaAs suggests that there should be some mass transport of GaAs and possible formation of InGaAsP during fusing at temperatures above 625 °C. Indeed, Yang *et al.*[39] have seen a low density of structures which they attribute to the formation of InGaAsP with cross-sectional diameters of 100 Å in TEM images of a GaAs/InP interface fused at 650 °C. At this temperature, however, the dominant vapor pressure is that of $P_2(g)$ which leads to an abrupt InP/GaAs junction over most of the interface.

**Table 3.3** Maximum temperatures of congruent evaporation, minimum reported fusing temperatures, and melting points for various III-V compounds. The melting points of InAs and InSb are shown for reference. No data on the CET or fusing of these materials was found.

| Material | Maximum CET[43,47] | Fusing Temperatures[3] [3,28] | Melting Point[48] |
|----------|--------------------|-------------------------------|-------------------|
| InP      | 360 °C             | 450 °C                        | 1060 °C           |
| GaAs     | 625 °C             | 840 °C                        | 1240 °C           |
| GaP      | 675 °C             | not reported                  | 1480 °C           |
| InAs     |                    |                               | 940 °C            |
| InSb     |                    |                               | 530 °C            |

As mass transport occurs and the InP and GaAs surfaces come into contact at the fusing temperature, the individual atoms bond together at the interface. The atoms from the different crystals bond together at the interface because the energy required to form the interfacial bonds is less than the energy required to maintain the dangling bonds of free surfaces.

Extension of this theory to bonding of other materials requires knowledge of the relative dissociation energies of the materials used in order to predict the best temperature and times to achieve bonding. Adequate removal of native oxides, organic contaminants, and particulates from the wafer surfaces should allow fusing to occur at temperatures as low as the CET of one of the materials to be fused. Although there is not much data on the CET of most materials, the melting points for III-V compounds are well known and follow the same trend as the CETs. For example, it has been suggested[49] that InAs be used as a thin buffer layer for bonding e.g. Si to GaAs. While previous work by Lo *et al.* [50] has shown that thin

InP layers work as a buffer between Si and GaAs, based on the model proposed above for the bonding process InAs should allow even lower bonding temperatures than InP layers. The melting point of InAs is 940 °C while that of InP is 1060 °C [48], and the CETs for the two materials are expected to follow the same trend. Thus, $As_2(g)$ should evolve from the InAs surface at lower temperatures than $P_2(g)$ evolves from InP, allowing the In atoms to diffuse freely on the InAs surface and fill in the gaps between the two wafers. A less-commonly grown material, InSb may offer the interfacial layer which would result in the lowest bonding temperature. The melting point of InSb is 530 °C, less than half of the melting point of InP.

## 3.6 Summary

This chapter has presented an overview of different methods for bonding semiconductor wafers. Although various methods such as epitaxial lift-off and interfacial metal bonding have important applications, only wafer fusion meets the stringent requirements for making a VCSEL. The interface plays an important role in both the optical and electrical properties of the VCSEL. All other bonding techniques resulted in interfaces with high resistances or optical losses. Wafer fusion does have the disadvantage that it takes place at temperatures around 650 °C which may result in diffusion of dopants. This needs further study to determine how much, if any, diffusion occurs.

A model of the wafer bending caused by cooling illuminated several of the important parameters which affect the wafer fusion process and pointed to ways to improve the process. The model predicts that more robust fusing can be done if the final substrate is very thick compared to the bonded film. This can be achieved through a combination of epitaxial lift off and fusing or through other methods to leave a thin film on the GaAs/AlAs mirror.

An analysis of the fused interface gave design criteria for making optoelectronic devices. The active layer should be placed greater than 2000 Å away from the fused interface to avoid defect induced degradation in the luminescence efficiency. When using an (Al,Ga)As double heterostructure, the first aluminum containing layer should be more than 2000 Å from the fused interface to avoid aluminum interdiffusion. The appearance of thermodynamically stable edge dislocations to relax the stress due to lattice mismatch indicates that device lifetimes should not suffer due to the fusing process.

Finally, a model is proposed for the fusing process. It is predicted that fusing between InP and GaAs should occur at lower temperatures with the correct choice of interfacial layers. In particular, InAs and InSb are good candidates for bonding layers due to the low energy necessary to dissociate these compounds. The limiting mechanism for fusing is suggested to be the evaporation of the group V element while leaving the group III element on the surface free to diffuse. This model can then be used to predict fusing temperatures for different material systems.

Wafer fusion is still rich with opportunities both to exploit this technique and to better understand the resulting interfaces. Some suggestions for future work involving fusion will be given in Chapter 6.

## References

[1]     Chang, J.C.P., Chin, T.P., Tu, C.W., and Kavanagh, K.L., "Multiple Disolocation Loops in Linearly Graded $In_xGa_{1-x}As$ (0≤x≤0.53) on GaAs and $In_xGa_{1-x}P$ (0≤x≤0.32) on GaP," *Applied Physics Letters*, vol. 63, no. 4, 500-502, 26 July 1993.

[2]     Nakamura, T., U. S. Patent 3239908, 1964.

[3]     Kenney, D.M., *Method of Isolating Chips of a Wafer of Semiconducting Material.*, U. S. Patent 3332137, 1967.

[4]     Riseman, J., *Method of Forming an Integrated Circuit Structure with Fully-Enclosed Air Isolation.*, U. S. Patent 4169000, 1979.

[5]     Nakagawa, A., Watanabe, K., Yamaguchi, Y., Ohashi, H., and Furukawa, K., "1800 V Bipolar-Mode MOSFETs: A First Application of Silicon Wafer Direct Bonding (SDB)," in *Technical Digest of the International Electron Devices Meeting*, IEEE, New York, NY, 1986, pp. 122-5.

[6]     Ohura, J., Tsukakoshi, T., Fukuda, K., Shimbo, M., and Ohashi, H., "A Dielectrically Isolated Photodiode Array By Silicon-Wafer Direct Bonding," *IEEE Electron Device Letters*, vol. EDL-8, no. 10, 454-6, Oct. 1987.

[7]     Furukawa, K. and Nakagawa, A., "Applications Of The Silicon Wafer Direct-Bonding Technique To Electron Devices," *Applied Surface Science*, vol. 41-42, 627-32, 1989.

[8]     Stengl, R., Ahn, K.Y., and Gosele, U., "Bubble-Free Silicon Wafer Bonding in a Non-Cleanroom Environment," *Japanese Journal of Applied Physics*, vol. 27, no. 12, L2364-6, Dec. 1988.

[9]     Bower, R.W., Ismail, M.S., and Roberds, B.E., "Low Temperature $Si_3N_4$ Direct Bonding," *Applied Physics Letters*, vol. 62, no. 26, 3485-7, 28 June 1993.

[10]    Wada, H., Babić, D.I., Ishikawa, M., and Bowers, J.E., "Effects Of Nonuniform Current Injection In GaInAsP/InP Vertical-Cavity Lasers," *Applied Physics Letters*, vol. 60, no. 24, 2974-2976, Jun 15 1992.

[11]    Yablonovitch, E., Gmitter, T., Harbison, J.P., and Bhat, R., "Extreme Selectivity In The Lift-Off Of Epitaxial GaAs Films," *Applied Physics Letters*, vol. 51, no. 26, 2222-24, 28 Dec. 1987.

[12]    Apiezon W, a very handy substance for use in the processing lab, is commonly referred to as 'black wax.'

[13] Yablonovitch, E., Kapon, E., Gmitter, T.J., Yun, C.P., and Bhat, R., "Double Heterostructure GaAs/AlGaAs Thin Film Diode Lasers On Glass Substrates," *IEEE Photonics Technology Letters*, vol. 1, no. 2, 41-2, Feb. 1989.

[14] Pollentier, I., Buydens, L., Daele, P.V., and Demeester, P., "Fabrication Of A GaAs-AlGaAs GRIN-SCH SQW Laser Diode On Silicon By Epitaxial Lift-Off," *IEEE Photonics Technology Letters*, vol. 3, no. 2, 115-17, Feb. 1991.

[15] Yi-Yan, A., Seto, M., Gmitter, T.J., Hwang, D.M., and Florez, L.T., "Grafted GaAlAs Rib Waveguides On An InP Substrate," *Electronics Letters*, vol. 26, no. 19, 1567-9, 13 Sept. 1990.

[16] Hargis, M.C., Carnahan, R.E., Brown, J.S., and Jokerst, N.M., "Epitaxial Lift-Off GaAs/AlGaAs Metal-Semiconductor-Metal Photodetectors With Back Passivation," *IEEE Photonics Technology Letters*, vol. 5, no. 10, 1210-12, Oct. 1993.

[17] Yablonovitch, E., Sands, T., Hwang, D.M., Schnitzer, I., Gmitter, T.J., Shastry, S.K., Hill, D.S., and Fan, J.C.C., "Van Der Waals Bonding Of GaAs On Pd Leads To A Permanent, Solid-Phase-Topotaxial, Metallurgical Bond," *Applied Physics Letters*, vol. 59, no. 24, 3159-61, 9 Dec. 1991.

[18] Ralph, S.E., Hargis, M.C., and Pettit, G.D., "Large Area, Low Voltage, Transit Time Limited InGaAs Metal Semiconductor Metal Photodetectors," *Applied Physics Letters*, vol. 61, no. 18, 2222-4, 2 Nov. 1992.

[19] Konagai, M., Sugimoto, M., and Takahashi, K., "High Efficiency GaAs Thin Film Solar Cells By Peeled Film Technology ," *Journal Of Crystal Growth*, vol. 45, no. 1, 277-80, Dec. 1978.

[20] Chan, W.K., Yi-Yan, A., Gmitter, T.J., Florez, L.T., Jackel, J.L., Hwang, D.M., Yablonovitch, E., Bhat, R., and Harbison, J.P., "Optical Coupling Of GaAs Photodetectors Integrated With Lithium Niobate Waveguides," *IEEE Photonics Technology Letters*, vol. 2, no. 3, 194-6, March 1990.

[21] Yi-Yan, A., Chan, W.K., Gmitter, T.J., Florez, L.T., Jackel, J.L., Yablonovitch, E., Bhat, R., and Harbison, J.P., "Grafted GaAs Detectors On Lithium Niobate And Glass Optical Waveguides," *IEEE Photonics Technology Letters*, vol. 1, no. 11, 379-80, Nov. 1989.

[22] Yablonovitch, E., Hwang, D.M., Gmitter, T.J., Florez, L.T., and Harbison, J.P., "Van Der Waals Bonding Of GaAs Epitaxial Liftoff Films Onto Arbitrary Substrates," *Applied Physics Letters*, vol. 56, no. 24, 2419-21, 11 June 1990.

[23] Tan, I.H., Reaves, C., Dudley, J.J., Holmes, A.L., Babić, D.I., Hu, E.L., Bowers, J.E., and DenBaars, S., "Low-Temperature Pd Direct Bonding and Electrical Transport Across InP-Pd-GaAs Interfaces," *Proceedings of the 6th Intl. Conference on InP and Related Materials*, paper ThG4, Mar. 1994.

[24] Venkatasubramanian, R., Timmons, M.L., Humphreys, T.P., Keyes, B.M., and Ahrenkiel, R.K., "High-Quality Eutectic-Metal-Bonded AlGaAs-GaAs Thin Films On Si Substrates," *Applied Physics Letters*, vol. 60, no. 7, 886-888, 17 Feb 1992.

[25] Goossen, K.W., Cunningham, J.E., and Jan, W.Y., "GaAs 850-nm Modulators Solder-Bonded To Silicon," *IEEE Photonics Technology Letters*, vol. 5, no. 7, 776-78, Jul 1993.

[26] Liau, Z.L. and Mull, D.E., "Wafer Fusion - A Novel Technique For Optoelectronic Device Fabrication And Monolithic Integration," *Applied Physics Letters*, vol. 56, no. 8, 737-39, 19 Feb 1990.

[27] Lo, Y.H., Bhat, R., Hwang, D.M., Koza, M.A., and Lee, T.P., "Bonding By Atomic Rearrangement Of InP/InGaAsP 1.5-$\mu$m Wavelength Lasers On GaAs Substrates," *Applied Physics Letters*, vol. 58, no. 18, 1961-63, May 6 1991.

[28] Gordon, L., Woods, G.L., Eckardt, R.C., Route, R.R., Feigelson, R.S., Fejer, M.M., and Byer, R., "Diffusion-Bonded Stacked GaAs For Quasiphase-Matched Second-Harmonic Generation Of A Carbon Dioxide Laser," *Electronics Letters*, vol. 29, no. 22, 1942-4, 28 Oct. 1993.

[29] Kish, F.A., Steranka, F.M., Defevere, D.C., Vanderwater, D.A., Park, K.G., Kuo, C.P., Osentowski, T.D., Peanasky, M.J., Yu, J.G., Fletcher, R.M., Steigerwald, D.A., Craford, M.G., and Robbins, V.M., "Very High-Efficiency Semiconductor Wafer-Bonded Transparent-Substrate $(Al_xGa_{1-x})_{0.5}In_{0.5}P/GaP$ Light-Emitting Diodes," *Applied Physics Letters*, vol. 64, no. 21, 2839-2841, 23 May 1994.

[30] The process which we are currently using was developed as part of a collaboration between Hewlett-Packard Laboratories and UCSB. Because of our agreements with Hewlett-Packard, the details of the process cannot be mentioned in this thesis.

[31] Dagata, J.A., Tseng, W., Bennett, J., Schneir, J., and Harary, H.H., "$P_2S_5$ Passivation of GaAs Surfaces for Scanning Tunneling Microscopy in Air," *Applied Physics Letters*, vol. 59, no. 25, 3288-90, 16 Dec. 1991.

[32] Hwang, K.C. and Li, S.S., "A Study of New Surface Passivation Using $P_2S_5/(NH_4)_2S$ on GaAs Schottky Barrier Diodes," *Journal of Applied Physics*, vol. 67, no. 4, 2162-65, 15 Feb. 1990.

[33] Wada, H., Ogawa, Y., and Kamijoh, T., "Electrical Characteristics Of Directly-Bonded GaAs And InP," *Applied Physics Letters*, vol. 62, no. 7, 738-40, 15 Feb. 1993.

[34] Timoshenko, S., "Analysis of Bi-Metal Thermostats," *Journal of the Optical Society of America*, 233-55, Sept. 1925.

[35] Swaminathan, V. and Macrander, A.T., *Materials Aspects of GaAs and InP Based Structures.* Prentice-Hall, 1992.

[36] Grupen-Shemansky, M.E., Hawkins, G.W., and Liaw, H.M., "Stress in GaAs Bonded to Si," in *Proceedings of the First International Symposium on Semiconductor Wafer Bonding,* vol. 11992, pp. 132-145.

[37] Ram, R.J., Yang, L., Nauka, K., Houng, Y.M., Ludowise, M., Mars, D.E., Dudley, J.J., and Wang, S.Y., "Analysis Of Wafer Fusing For 1.3 μm Vertical Cavity Surface Emitting Lasers," *Applied Physics Letters*, vol. 62, no. 20, 2474-76, 17 May 1993.

[38] Ram, R.J., Yang, L., Nauka, K., Fouquet, J., Ludowise, M., Houng, Y.M., Mars, D.E., Dudley, J.J., and Wang, S.Y., "Characterization of Wafer Fusing for Hybrid Optoelectronic Devices," *Proceedings of the Electronics Materials Conference*, paper S2, June 1993.

[39] L. Yang, K. Carey, M. Ludowise, W. Perez, D. E. Mars, J. E. Fouquet, K. Nauka, S. J. Rosner, R. J. Ram, J. J. Dudley, D. I. Babic and J. Bowers, "Wafer Bonding Of InP And GaAs: Interface Characterization And Device Applications," in *Proceedings of the Sixth International Conference On Indium Phosphide,* Santa Barbara, CA, 1994, pp. 214-15.

[40] The TEM study was done at the Hewlett-Packard Integrated Circuit Business Division.

[41] Fischer, R., Morkoc, H., Neumann, D.A., Zabel, H., Choi, C., Otsuka, N., Longerbone, M., and Erickson, L.P., "Material Properties of High-Quality GaAs Epitaxial Layers Grown on Si Substrates," *Journal of Applied Physics*, vol. 60, no. 5, 1640-47, 1 Sept. 1986.

[42] Goel, A.K. and Shah, H., "Gallium Arsenide-On-Silicon Technology-An Overview," in *Proceedings Of The 32Nd Midwest Symposium On Circuits And Systems,* Champaign, Il, 1990, pp. 1259-62 Vol.2.

[43] Farrow, R.F.C., "The Evaporation of InP Under Knudsen (Equilibrium) and Langmuir (Free) Evaporation Conditions," *Journal of Physics D: Applied Physics*, 2436-48, 1974.

[44]  Hansen, K., Peiner, E., Tang, G., and Schlachetzki, A., "A Theoretical Model of InP Mass Transport," *Japanese Journal of Applied Physics*, vol. 32, no. 1A, 234-38, January 1993.

[45]  Ayabe, M., Nagasawa, H., and Kaneko, K., "Vapor-Phase Transport of GaAs on a V-Shape Grooved GaAs Substrate," *Journal of Crystal Growth*, vol. 58, 180-84, 1982.

[46]  Liau, Z.L. and Zeiger, H.J., "Surface-Energy-Induced Mass-Transport Phenomenon in Annealing of Etched Compound Semiconductor Structures: Theoretical Modeling and Experimental Confirmation," *Journal of Applied Physics*, vol. 67, 2434, 1990.

[47]  Foxon, C.T., Joyce, B.A., Farrow, R.F.C., and Griffiths, R.M., "The Identification of Species Evolved in the Evaporation of III-V Compounds," *Journal of Physics D: Applied Physics*, vol. 7, 2422-35, 1974.

[48]  *Handbook of Chemistry and Physics*.  CRC Press, 1993.

[49]  This idea was originally suggested by John Bowers.

[50]  Lo, Y.H., Bhat, R., Hwang, D.M., Chua, C., and Lin, C.H., "Semiconductor Lasers On Si Substrates Using The Technology Of Bonding By Atomic Rearrangement," *Applied Physics Letters*, vol. 62, no. 10, 1038-1040, Mar 8 1993.

# Chapter 4
# **Optically Pumped VCSELs**

### 4.1 Introduction

Optical pumping provides a simple method to test whether wafer fusion can be used to create a long wavelength VCSEL. It simplifies the study of the device physics, allowing us to look simply at the active region placed inside a short cavity with a fused GaAs/AlAs mirror on one side and an insulating mirror on the opposite side. Optical pumping gives the most simple test of whether the fused interface prohibits or allows lasing to occur in a vertical cavity laser. The fabrication procedure is straightforward and does not require deposition and optimization of ohmic contacts, definition of current confining regions, etc. Optical pumping eliminates the contact resistance, mirror resistance, and device fabrication procedure as possible mechanisms for failure of a fused VCSEL.

In this chapter I will discuss the results of the optical pumping experiment, which allowed us to demonstrate lasing for the first time in a VCSEL which utilized non-lattice matched, epitaxially grown mirrors. The wafer fused VCSEL operated

at temperatures as high as 144 °C, the highest operating temperature reported for a long wavelength VCSEL. The wafer fused VCSEL had pulse widths as short as 34 psec, the shortest pulses reported to date for a long wavelength VCSEL[1].

In this chapter, I will briefly discuss the device fabrication and measurement technique. Then I will examine the room temperature lasing characteristics of the wafer fused VCSELs. The high speed characteristics of the devices will be analyzed. Finally I will look at the performance of the optically pumped VCSELs over a range of temperatures.
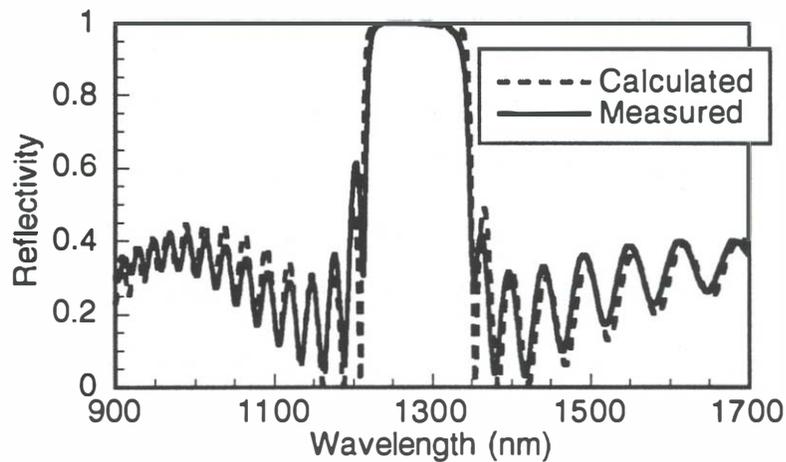
**Fig. 4.1:** Measured (solid line) and calculated (dashed line) reflectivity spectra of the GaAs/AlAs mirror used in the optically pumped VCSEL.

## 4.2 Device fabrication

The InP double heterostructure wafer was grown by metalorganic vapor phase epitaxy (MOVPE) on a p-type (100) InP substrate. The complete wafer structure is

shown in Table 4.1. Zinc was used for the p-type dopant, while S was used for the

n-type dopant.

**Table 4.1** The layer structure for the InP double heterostructure used in the optically pumped VCSEL.

| Material | Thickness | Doping | Comments |
|---|---|---|---|
| n-InP | 2.0 μm | $N_D = 1 \times 10^{18}$ cm$^{-3}$ | |
| p-InGaAsP ($\lambda_{gap}$ = 1.3 μm) | 0.6 μm | $N_A = 2 \times 10^{17}$ cm$^{-3}$ | active layer |
| p-InP | 1.5 μm | $N_A = 7 \times 10^{17}$ cm$^{-3}$ | |
| p-InGaAsP ($\lambda_{gap}$ = 1.1 μm) | 0.1 μm | | etch stop layer |
| p-InP | 0.5 μm | | buffer layer |
| p-InP | | | substrate |

The molecular beam epitaxy grown GaAs/AlAs mirror consists of 27 periods of

quarter-wavelength thick layers of AlAs (112 nm) and GaAs (95 nm) grown on a

GaAs substrate. The interfaces have a linearly changing, digitally-graded alloy

composition with a period of 2 nm and a total length of 18 nm$^2$. The top GaAs

layer of the mirror is 1.25 wavelengths thick to prevent any bonding-induced strain

from decreasing the mirror reflectivity. The measured and modeled mirror spectra

are shown in Fig. 4.1. The top mirror is a 5-period Si/SiN$_x$ quarter wave mirror

for coupling light out of the VCSEL. The mirror is designed to achieve close to the

maximum available reflectivity while allowing approximately half of the available

light to be transmitted through the mirror as shown in Fig. 4.2.
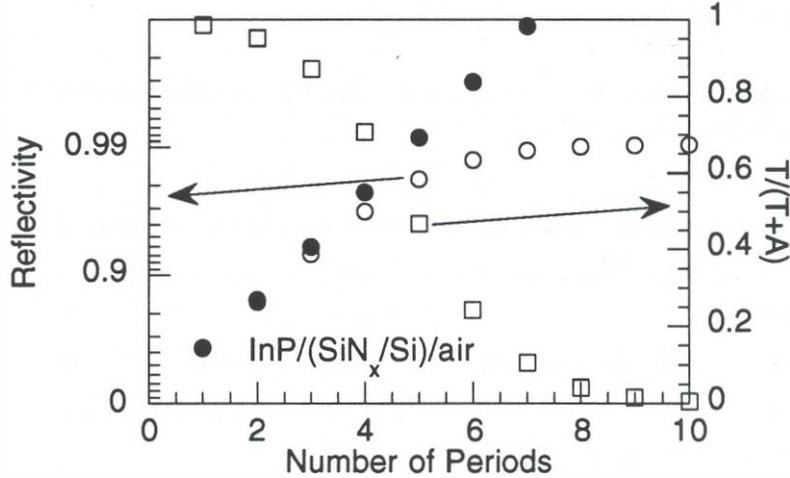
**Fig. 4.2** The calculated reflectivity with (hollow circles) and without (solid circles) loss in Si/SiNx mirrors as viewed from InP. The hollow squares show the fraction of the non-reflected light which can be transmitted through the mirror to air.

Before bonding, both wafers undergo a solvent clean, are etched in buffered HF, and are rinsed in dionized water. The wafers are placed into contact immediately after blow drying with $N_2$ and loaded into a furnace tube with a 200 g graphite weight on top of the samples. The wafers are fused together at 650 °C for 2 hours in a $H_2$ ambient. After removing the fused wafers from the furnace, we remove the InP substrate using HCl. Finally, a five-period Si/SiN$_x$ mirror is reactively sputtered onto the top surface. A cross-sectional scanning electron micrograph of the completed device is shown in Fig. 4.3.
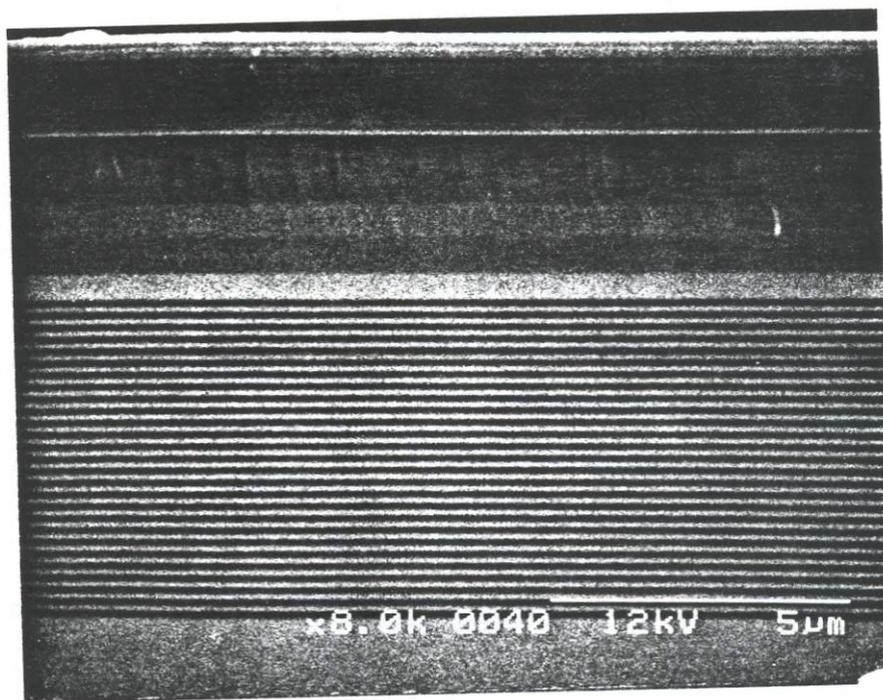
**Fig. 4.3**  A cross-sectional scanning electron micrograph of the optically pumped, wafer-fused VCSEL.

## 4.3 Optical Pumping Measurements

In this section I will describe the experimental set-up which was used to characterize the wafer fused VCSELs.  Power-in vs. power-out, spectra, pulsewidth, and chirp were all measured as a function of temperature.

The optical pumping set-up is shown in Fig. 4.4.  A mode-locked Nd:YAG ($\lambda = 1.06$ $\mu$m) laser optically excites the VCSEL wafer with 80-psec pulses at a repetition rate of 80 MHz.  The pump beam power is regulated with a manually controlled variable attenuator.

Nd:YAG

$\lambda = 1.06 \, \mu m$
**80 psec, 80 MHz**

→ **Pump beam**
▷ **VCSEL output**

**Dichroic
Beamsplitter**

**Heater**

**Attenuator**

**Detector**

**Lens**

**Lens          Band stop
filter**

**Lens**

**Surface Emitting
Laser**

**Detector**
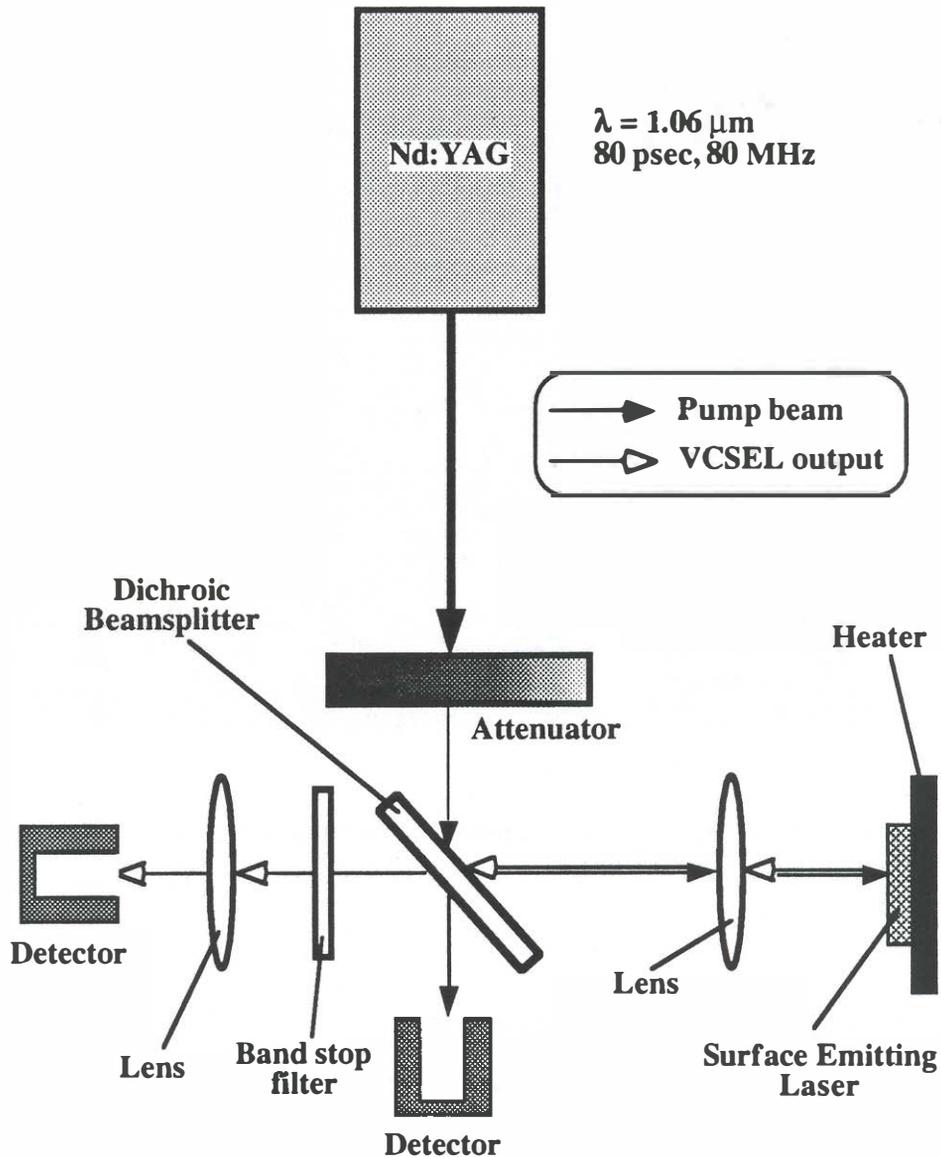
**Fig. 4.4** The measurement setup used to characterize the optically pumped
VCSELs.

A dichroic beam splitter reflects the pump beam through a focusing lens
($f = 19$ mm) onto the sample at a spot size of approximately 30 μm. The portion
of the pump light which passes through the beam splitter focuses onto a Ge detector

which is used to monitor the input power. The output of the VCSEL is collinear with the pump beam and passes through the dichroic beam splitter into either a detector, an optical fiber, or a streak camera. A band stop filter in front of the detector removes any residual pump light. The efficacy of the band stop filter is verified using an optical spectrum analyzer.

The sample rests on a temperature controlled stage which can be varied from room temperature to greater than 150 °C. The stage temperature is measured by a platinum thermistor which is located next to the sample.

## 4.4 Room Temperature Characteristics

At room temperature (20 °C), two distinct slopes appear in the power-in vs. power-out (L-L) curve (Fig. 4.5): one from threshold (140 mW) to 300 mW input power and one above 300 mW. In the first region, the laser operates in a single longitudinal mode at 1.22 $\mu$m. The full width at half maximum of this mode is 1.7 nm. I will discuss the cause of this broad spectrum in Section 5. A second mode at 1.28 $\mu$m appears when the input power reaches 300 mW, corresponding to the start of the second region in the L-L curve. The band stop filter used to block the pump beam enhances the two slope effect in the L-L curve because it transmits only 40% of the shorter wavelength compared to 73% of the longer wavelength. Because of the long cavity length in this device (4.7 $\mu$m), we expect to see two cavity modes, unlike in shorter wavelength VCSELs which typically have cavity lengths of 0.5 wavelengths and a single longitudinal mode. Below threshold (Fig. 4.5(a)), the two cavity modes can be seen in the spectra. Just above threshold (Fig. 4.5(b)), the mode at 1.22 $\mu$m dominates the spectrum.
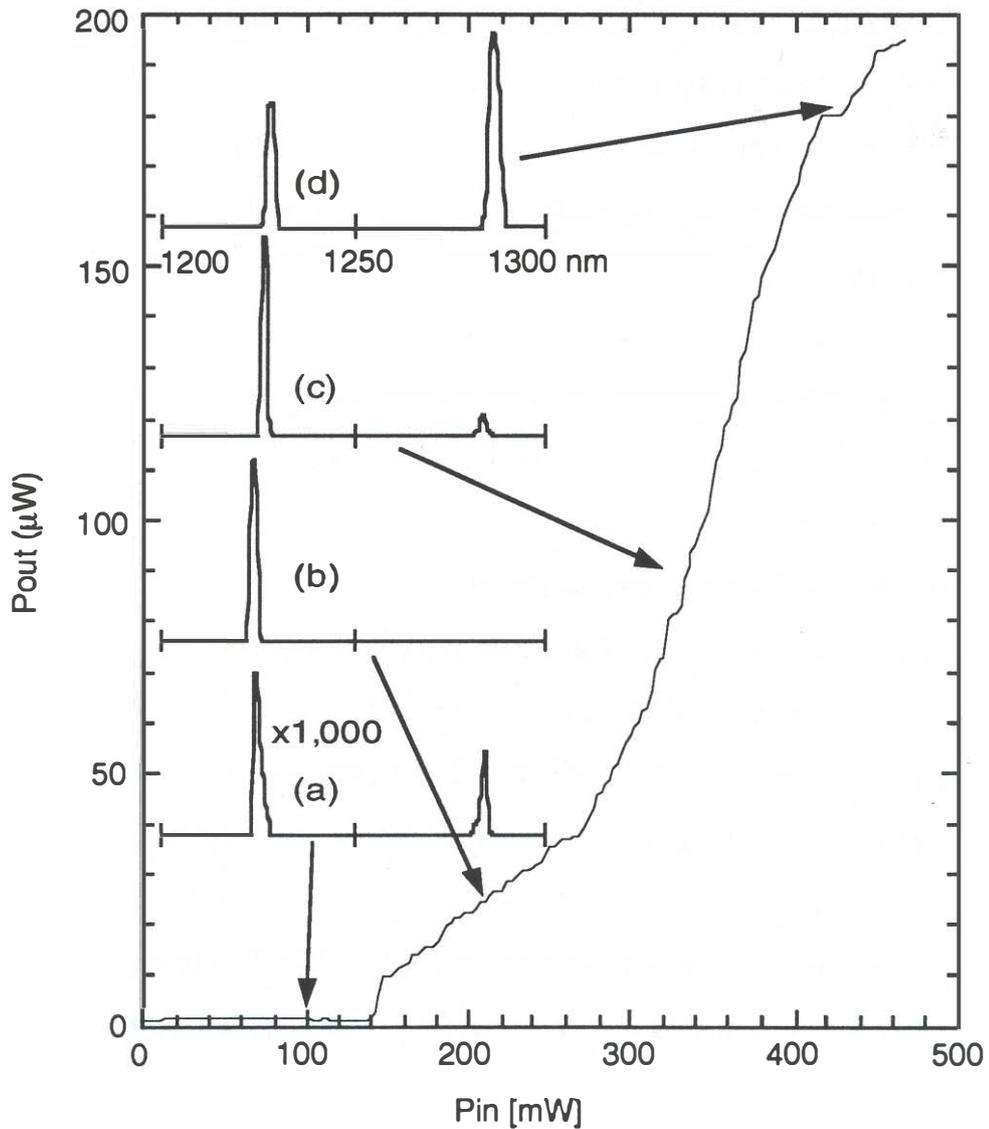
**Fig. 4.5** Room temperature average light-in vs. average light out characteristic of the optically pumped VCSEL. Inset are spectra at various pump levels.

As the input power increases, the cavity modes move toward longer wavelengths. The longer wavelength, 1.28 μm mode appears (Fig. 4.5(c)) and increases in strength relative to the first mode at higher input power (Fig. 4.5(d)).

The shift in modes with increasing power is caused by pump-induced heating of the device. The time between pulses is only 12.5 nsec, while VCSELs typically have a thermal time constant on the order of 1 $\mu$sec[3]. There is not enough time between pulses for the active region of the laser to cool down to the stage temperature, so as the input power increases the active region heats up. The increase in temperature causes the gain spectrum and cavity modes to red shift. The gain peak red shifts at a rate much greater than the cavity mode. Thus, as the active layer temperature increases, the gain peak moves out of resonance with the shorter wavelength mode and into resonance with the longer wavelength mode.

From measurements of temperature dependent spectra at the spot on the sample measured in Fig. 4.5, the cavity mode moves at a rate of 1.7 Å/°C. The longer wavelength cavity mode moves 52 Å when the input power increases by 260 mW, corresponding to a temperature rise of 31 °C. Taking into account the reflectivity of the Si/SiN$_x$ mirror at the pump wavelength ($\approx$ 50 %) and estimating that the absorption in the active region is $10^4$ cm$^{-1}$, approximately 20 % of the incident power is absorbed in the active region. This indicates that the thermal resistance of this device is 600 K/W. This agrees well with a calculated thermal resistance of 550 K/W.

## 4.5 High Speed Measurements

As was mentioned in the previous section, the full width at half maximum of the spectrum of the optically pumped VCSEL is 17 Å. This is much broader than the expected value for the linewidth of the VCSEL, which should be < 1 Å. One possible explanation of the observed spectral broadening could involve device

heating during lasing, causing an increase in the refractive index of the cavity which leads to a red shift of the cavity mode and is observed through the broadened time averaged spectra. However, the heating process typically takes on the order of 1 μsec, while the pulse width is only 80 psec. Thus heating is not a likely cause of the pulse broadening.

A more likely cause of the spectral broadening is that the optical pumping induces self-phase modulation, causing the VCSEL pulse to be chirped[4]. As the pump beam excites the VCSEL, the active layer absorbs the incident light causing the excitation of electrons from the valence band to the conduction band. This increases the carrier density until the active region is bleached by the pump beam. The carrier density and the refractive index of the active region are coupled together. As the refractive index changes, the instantaneous frequency changes. This frequency change is observed in a time-averaged measurement as a broadening of the spectral width.
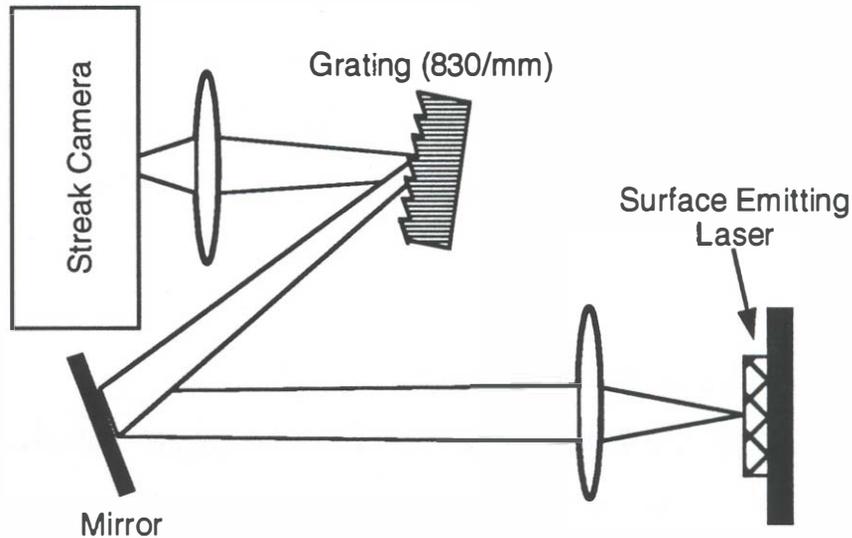


**Fig. 4.6** Measurement technique used to confirm chirping in the VCSEL output. The pump beam is not shown in this figure.

In order to determine if the pulse is chirped, we need to observe the output spectra as a function of time.  A streak camera can be used to measure the pulse width of the VCSEL output.  By directing the output of the VCSEL onto a grating and then taking the diffracted beam into the streak camera (Fig. 4.6), the spectrum of the VCSEL pulse can be measured simultaneously with the pulse width.  The wavelength resolution is determined by the spatial resolution of the streak camera and the resolution of the grating which is used.  The measured resolution of the streak camera is 3 Å/channel.  (There are 500 channels in the vertical axis.)

The resolution of the grating can be calculated using the Rayleigh criterion[5],

$$\frac{\Delta\lambda}{\lambda} = \frac{1}{nm} = \frac{\lambda}{nd(\sin\theta_m - \sin\theta_i)} \tag{4-1}$$

where $\Delta\lambda$ is the minimum resolvable wavelength difference, $\lambda$ is the average wavelength, $n$ is the number of lines illuminated on the grating, $m$ is the order of the diffraction, $d$ is the separation between grating lines, $\theta_m$ is the angle of diffraction, and $\theta_i$ is the incident angle.  The spot diameter at the grating (830 lines/mm) was approximately 5 mm, giving $n = 4150$, and the first order ($m = 1$) diffracted beam was monitored.  The center wavelength was 1.27 µm, giving a resolution of 3 Å.  Thus, the grating and the streak camera equally limit the resolution of the spectral measurement.

Figure 4.7 shows the streak camera trace at 42 °C with an input power of 400 mW.  The wavelength is calibrated using an optical spectrum analyzer to measure the center wavelength at two different temperatures and measuring the locations of the streak traces at the two different temperatures.  This calibration was confirmed

by noting the spacing between the shorter wavelength and longer wavelength mode with the spectrum analyzer and with the streak camera. The center wavelength of the mode moves 1.4 ± 0.3 nm during the output pulse, which agrees with the FWHM of 1.6 nm measured using an optical spectrum analyzer. The pulse width is approximately 34 psec, which is the shortest pulse recorded for a long wavelength VCSEL.
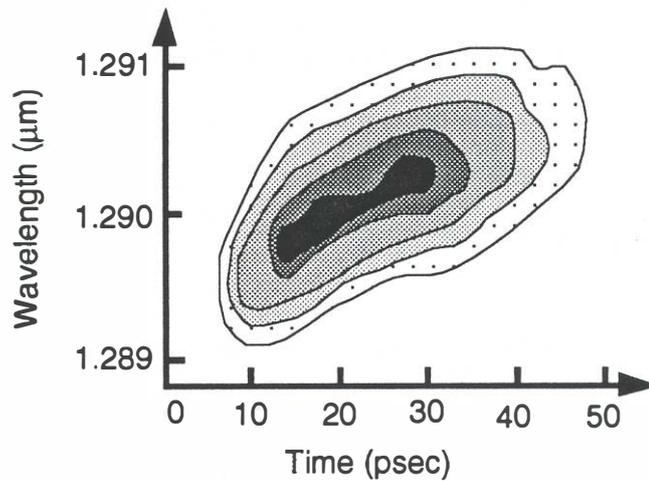


**Fig. 4.7** Output wavelength as a function of time for one of the two modes in the optically pumped VCSEL. The shading corresponds to the intensity of the VCSEL output.

## 4.6 High Temperature Characteristics

Figure 4.8 shows the effect of increasing temperature on the threshold power at a different place on the wafer than in the data shown in Fig. 4.5. The placement of the gain peak relative to the cavity modes and the long optical cavity which gives two longitudinal modes help to give this device a large temperature range over which it can operate. The device lases at temperatures as high as 144 °C. The

threshold power increases over the temperature range of 23 to 80 °C with a $T_0$ of 42 K, where $T_0$ is defined by

$$P_{th} = P_0 \exp\left(T/T_0\right) \tag{4-2}$$

Over this temperature range the gain peak moves out of resonance with the shorter wavelength cavity mode. From 80 to 90 °C, the threshold *decreases* due to the gain peak beginning to move into resonance with the longer wavelength mode. From 90 to 144 °C the gain peak continues to move into resonance with the longer wavelength mode. The threshold power is less sensitive in this temperature range than it is from 23 to 80 °C as indicated by the higher $T_0$ of 81 K.
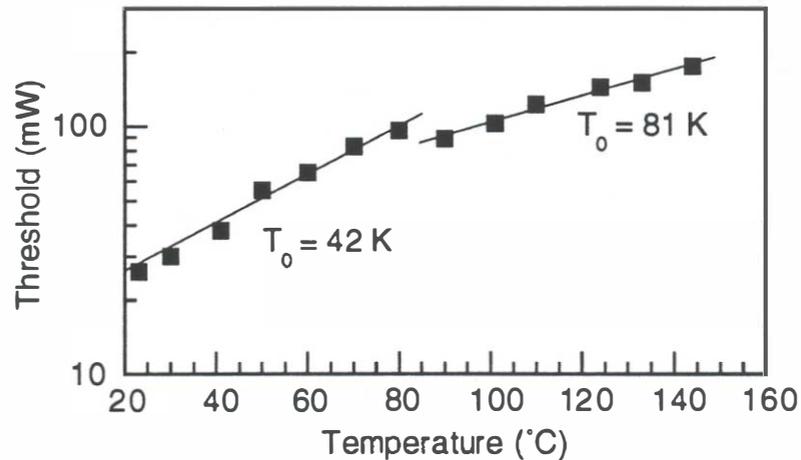


**Fig. 4.8** Measured threshold power as a function of temperature.

Figure 4.9 shows the effects of increasing temperature on the cavity modes. The spectra of the device were measured at 150 mW input power at all

temperatures. The fused VCSEL operates in a single longitudinal mode at 1.23 μm

from 23 °C to 50 °C. At 60 °C, a second mode appears at 1.29 μm. The shorter

wavelength mode is the predominant mode until the temperature reaches 144 °C.

The shorter wavelength mode changes with temperature with a rate of 1.2 Å/ °C.

The longer wavelength mode changes with temperature at a rate of 1.3 Å/ °C.
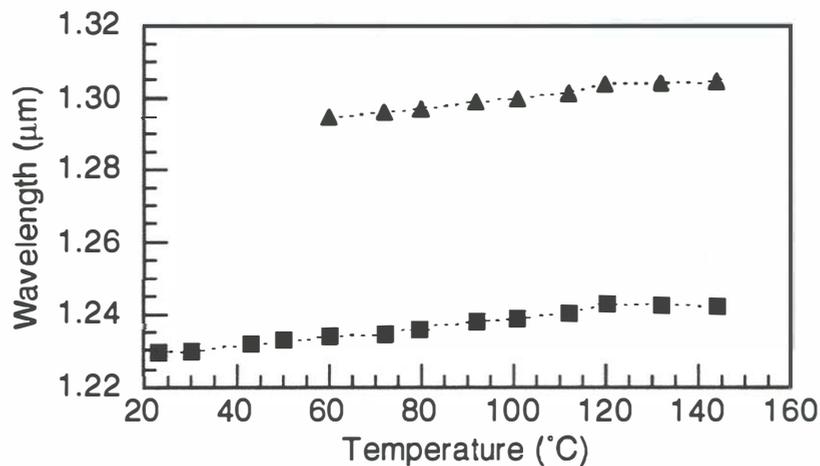
**Fig. 4.9**  Variation of the cavity modes with temperature.

## 4.7  Conclusions

In this chapter I described the optical pumping of a wafer fused VCSEL. This

allowed us to study the physics in, and demonstrate the feasibility of, long

wavelength VCSELs which use GaAs/AlAs mirrors. The use of a long cavity gave

two longitudinal modes and helped to achieve lasing operation at temperatures as

high as 144 °C.

A broader than expected spectrum at room temperature of these lasers led to the study of the high speed characteristics of these devices. The broad spectrum was found to be caused by chirping in the VCSEL pulse. The pulse width was measured to be 34 psec, which is the shortest pulse measured to date for a long wavelength VCSEL.

Although the optically pumped device was used to study the physics of wafer fused long wavelength VCSELs, it also has practical applications for devices in which a diode laser or a shorter wavelength VCSEL acts as the pump laser for the fused VCSEL. This device structure would eliminate problems with non-uniform carrier injection from contacts, heating in the device due to resistive drops in the cladding layers and mirror layers, etc. which currently limit the performance of electrically injected, long wavelength VCSELs.

## References

[1]  Dudley, J.J., Ishikawa, M., Babić, D.I., Miller, B.I., Mirin, R., Jiang, W.B., Bowers, J.E., and Hu, E.L., "144 °C Operation Of 1.3 μm InGaAsP Vertical Cavity Lasers On GaAs Substrates," *Applied Physics Letters*, vol. 61, no. 26, 3095-7, 28 Dec. 1992.

[2]  Geels, R.S., Corzine, S.W., and Coldren, L.A., "InGaAs Vertical-Cavity Surface-Emitting Lasers," *IEEE Journal Of Quantum Electronics*, vol. 27, no. 6, 1359-67, Jun 1991.

[3]  Hasnain, G., Tai, K., Yang, L., Wang, Y.H., Fischer, R.J., Wynn, J.D., Weir, B., Dutta, N.K., and Cho, A.Y., "Performance Of Gain-Guided Surface Emitting Lasers With Semiconductor Distributed Bragg Reflectors," *IEEE Journal Of Quantum Electronics*, vol. 27, no. 6, 1377-85, June 1991.

[4]  Jiang, W., Derickson, D.J., and Bowers, J.E., "Analysis Of Laser Pulse Chirping In Mode-Locked Vertical Cavity Surface-Emitting Lasers," *IEEE Journal Of Quantum Electronics*, vol. 29, no. 5, 1309-18, May 1993.

[5]  Hecht, E. and Zajac, A., *Optics.* Addison-Wesley, 1974.

# Chapter 5
# Electrically Injected Lasers

## 5.1 Introduction

The previous chapter described the first wafer fused VCSEL. Lasing occurred using a Nd:YAG laser to optically pump the VCSEL. The need for a more compact, inexpensive, and easily operated device drives us to move from an optically pumped device to an electrically injected device. Although an electrically injected device provides a more practical laser source, it presents far greater difficulties in its realization than an optically pumped device. In a VCSEL, both the carriers and the optical mode travel perpendicular to the substrate. Ideally, both the peak carrier density and the peak optical intensity occur in the same area. This complicates the design of the device. Furthermore, the fabrication procedure for an electrically injected device can be quite complex. A current confining structure must be defined. Contacts on top and bottom must be formed with the minimum resistance and placed in a location which does not interfere with the optical mode.

This chapter details how those difficulties have been handled to realize an electrically injected, wafer fused VCSEL. First, I will discuss the design of the lasers, looking at the effects of mirror detuning and heating on the performance of the devices. Then I will outline the fabrication of the lasers. I will describe the self-aligned fabrication procedure which incorporates several measurements to allow early diagnosis of problems with the process and/or materials and to better understand the fabrication process. After discussing the fabrication, the room temperature characteristics of the lasers will be examined. Light versus current measurements and spectral measurements will be reported, as will measurements of the optical mode. The wafer fused VCSELs have the lowest threshold current and threshold current density at room temperature reported to date for a long wavelength VCSEL. Before concluding the chapter, I will look at the temperature-dependent characteristics of the lasers. These characteristics give important information for the improvement of the next generation of wafer fused VCSELs.

## 5.2 Design

Once the decision has been made to use GaAs/AlAs mirrors, the selection of the exact mirror structure requires consideration of the ability to grow the desired layer structure and the consequences of any deviations from that layer structure. It is also important to determine the optimum active layer to choose. The design of the VCSEL cavity, including the choice of active layer thickness and number of mirror periods, is the topic of this section.

*Calculation method*

The basic cavity layer structure which is modeled is given in Table 5.1. For calculating a given design curve, different parts of the structure (e.g. the active layer thickness or the number of mirror periods) are varied. The threshold gain for a given structure is found numerically using a procedure outlined by Bjork and Nilsson[1] and discussed by Corzine[2] for applications to VCSELs. The program used to calculate the gain was written by Dubravko Babić.

In the method proposed by Bjork and Nilsson, the relationship between the input and output fields of an arbitrary multilayer structure is found using transmission matrices. That relationship is given by:

$$\begin{bmatrix} E_{in}^+ \\ E_{in}^- \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} E_{out}^+ \\ E_{out}^- \end{bmatrix} \tag{5-1}$$

The waves traveling to the right are represented with a '+', while the waves traveling to the left are represented with a '-'. If the input wave starts at the left-hand side of the structure and travels to the right, the input wave is given by $E_{in}^+$ and the transmission through the structure is given by $E_{out}^+ / E_{in}^+$. If there is gain in the active region, the amplitude of the output field can exceed the amplitude of the input field. Because the active region is placed inside a resonator, when the gain inside the active region reaches threshold, the ratio of output to input fields goes to infinity. Assuming no field is incident from the right hand side (i.e. $E_{out}^- = 0$), the threshold condition can be given as

$$\frac{E_{in}^+}{E_{out}^+} = T_{11} = 0 \tag{5-2}$$

The transmission coefficient $T_{11}$ is a complex function of both the wavelength and the gain. The solution to Eq. (5-2) thus gives the threshold gain and the wavelength of the cavity mode in the VCSEL. Efficient methods to find this solution are discussed by Corzine[2].

**Table 5.1** Cavity structure used in modeling gain and threshold current densities. Thicknesses in parentheses for layers 9-12 are used when keeping a constant optical thickness for the cavity.

| Layer Number | Material | Thickness | Index, $n$ | Loss (cm$^{-1}$) |
|---|---|---|---|---|
| 1-8 | 4-period Si/SiO$_2$ mirror: | | | |
| | Si | $\lambda_0/4n$ | 3.3 | 800 |
| | SiO$_2$ | $\lambda_0/4n$ | 1.45 | 0 |
| 9 | p-InGaAsP (1.1 $\mu$m) contact | 0.3 $\mu$m ($3\lambda_0/4n$) | 3.32 | 30 |
| 10 | p-InP | 0.58 $\mu$m ($3\lambda_0/2n$) | 3.20 | 15 |
| 11 | p-InGaAsP (1.3 $\mu$m) active | 0.3 $\mu$m ($3\lambda_0/4n$) | 3.5 | |
| 12 | n-InP | 0.5 $\mu$m ($5\lambda_0/4n$) | 3.20 | 10 |
| 13 | n-GaAs buffer layer | $\lambda_0/n$ | 3.41 | 10 |
| 14-67 | 27-period GaAs/AlAs mirror: | | | |
| | n-GaAs | $\lambda_0/4n$ | 3.41 | 10 |
| | n-AlAs | $\lambda_0/4n$ | 2.91 | 10 |
| 68 | n-GaAs substrate | | 3.41 | |

Once the threshold gain is found, the threshold carrier density is estimated using the linear relationship[3]:

$$g_{th} = a\left(n_{th} - n_{tr}\right) \tag{5-3}$$

where $g_{th}$ is the threshold gain, $a$ is the gain coefficient, $n_{th}$ is the carrier density, and $n_{tr}$ is the transparency carrier density. The values for $a$ and $n_{tr}$ used in these calculations are given in Table 5.2. Equation (5-3) gives a simple model for the maximum available gain in the active region which is instructive for use in deciding on a particular cavity design. More complete models of the lasing characteristics of a VCSEL, however, need to incorporate more sophisticated gain models. The cavity mode and the gain peak in a VCSEL do not necessarily fall at the same energy, thus a complete model should incorporate the spectral characteristics of the gain.

Once the threshold carrier density has been found, the current density required to reach threshold can be found using the relationship

$$
\begin{aligned}
J_{th} &= J_{rad} + J_{Auger} \\
&= q\,d\,Bn_{th}^2 + q\,d\,Cn_{th}^3
\end{aligned}
$$

$$(5\text{-}4)$$

where $J_{th}$ is the threshold current density, $J_{rad}$ and $J_{Auger}$ are the radiative and Auger components of $J_{th}$, q is the electronic charge, $d$ is the active layer thickness, $B$ is the radiative recombination coefficient, and $C$ is the Auger recombination coefficient. The values for $B$ and $C$ are found in Table 5.2.

This model is a one-dimensional model for finding the threshold current density in a given structure. As such, it does not take into account the effects of overlap between the injected carriers and the gain profile (i.e. current crowding or non-uniform injection), or the effects of diffraction loss. Less than optimal overlap between the gain profile and the injected carriers caused by non-uniform current injection is expected to play a role in the structure described later in the chapter, due

to the injection of carriers through a ring contact. The effects of diffraction loss would be difficult to include due to the complex physical design of the fabricated structure. The effects of diffraction loss are expected to be minimal, however, because of the use of the GaAs/AlAs mirror, as discussed in Chapter 2. By not including either of these two effects, this model is expected to give an optimistic value of the achievable threshold currents.

**Table 5.2** Physical constants used in the calculations of the design curves. These values come from Ref. 4.

| constant | symbol | value |
|---|---|---|
| Gain coefficient | $a$ | |
| 300 K | | $4.69 \times 10^{-16} \, cm^2$ |
| 350 K | | $3.60 \times 10^{-16} \, cm^2$ |
| Transparency carrier density | $n_{tr}$ | |
| 300 K | | $1.29 \times 10^{18} \, cm^{-3}$ |
| 350 K | | $1.57 \times 10^{18} \, cm^{-3}$ |
| Radiative recombination coefficient | $B$ | |
| 300 K | | $1.0 \times 10^{-10} \, cm^3/s$ |
| 350 K | | $1.0 \times 10^{-10} \, cm^3/s$ |
| Auger recombination coefficient | $C$ | |
| 300 K | | $5.0 \times 10^{-29} \, cm^6/s$ |
| 350 K | | $1.3 \times 10^{-28} \, cm^6/s$ |

*Threshold for Various Mirror Reflectivities*

The choice of active layer thickness and number of mirror periods to use in a given cavity are linked. In the calculations carried out for this section, I have chosen to use a 4-period Si/SiO$_2$ mirror ($R = 99.4$ %) on one side of the cavity and a

GaAs/AlAs mirror with varying number of mirror periods on the other side. The reflectivity for a given number of periods in the GaAs/AlAs mirror and the mean reflectivity for the GaAs/AlAs and Si/SiO$_2$ mirror combination is shown in Table 5.3.

**Table 5.3** Calculated values of the GaAs/AlAs mirror reflectivity as a function of number of periods using the parameters in Table 5.1. The reflectivity of the 4-period Si/SiO$_2$ mirror used in the calculations is 99.44 %. All reflectivities are calculated looking from the InP side of the mirror with the appropriate terminating material on the other side.

| Number of periods | Reflectivity | Mean reflectivity, $\sqrt{R_{GaAs/AlAs} R_{Si/SiO_2}}$ |
|---|---|---|
| 11 | 0.8045 | 0.8944 |
| 15 | 0.8906 | 0.9411 |
| 19 | 0.9897 | 0.9920 |
| 23 | 0.9962 | 0.9953 |
| 27 | 0.9980 | 0.9962 |
| 31 | 0.9998 | 0.9971 |

Early published calculations of threshold current densities for long wavelength VCSELs[5,6] neglected the effects of the refractive index differences between the active layer and the cladding layers in the VCSEL cavity, while keeping the cavity length constant. This early approach enherently ignored the effects of the standing wave pattern in the VCSEL cavity on the threshold gain, while the numerical procedure outlined here takes these effects into account. By keeping the cavity length fixed, the optical length (i.e. the physical distance multiplied by the refractive index) that the mode sees and hence the resonant wavelength of the VCSEL cavity changes, as shown in Fig. 5.1. The physical cavity length is kept constant in this calculation by varying the thickness of the active layer and changing the thicknesses

of the InP cladding layers evenly to compensate for the change in active layer
thickness.
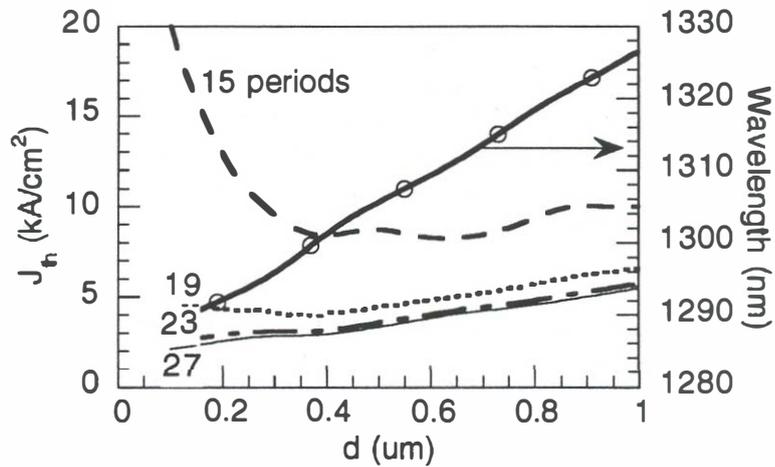


**Fig. 5.1**  Threshold current density as a function of active layer thickness, d,
for various number of GaAs/AlAs mirror periods keeping the physical length of
the VCSEL cavity 1.68 μm.  The resulting cavity mode wavelength is shown on
the right-hand axis.

The result of the change in the optical length of the cavity is a variation in cavity
wavelength of over 35 nm for a change in active region thickness from 0.1 to 1.0
μm.  This is an important effect in a VCSEL, because the gain peak and the cavity
mode do not necessarily fall at the same wavelength.  Thus, calculations using gain
data at the center wavelength of the mirrors will give erroneous results.

The threshold current density as a function of active layer thickness for a cavity
of fixed optical length is shown in Fig. 5.2.  This calculation is done by changing
the optical length of the InP cladding layers evenly to compensate for the change in
optical length of the active layer.  Note that on the same scale as shown in Fig. 5.1,

the cavity mode does not appear to change because the optical length of the cavity is the same. However, the reflection of the wave at the refractive index discontinuities in the cavity does cause a fluctuation of ±4 Å around the center wavelength of 1300 nm.
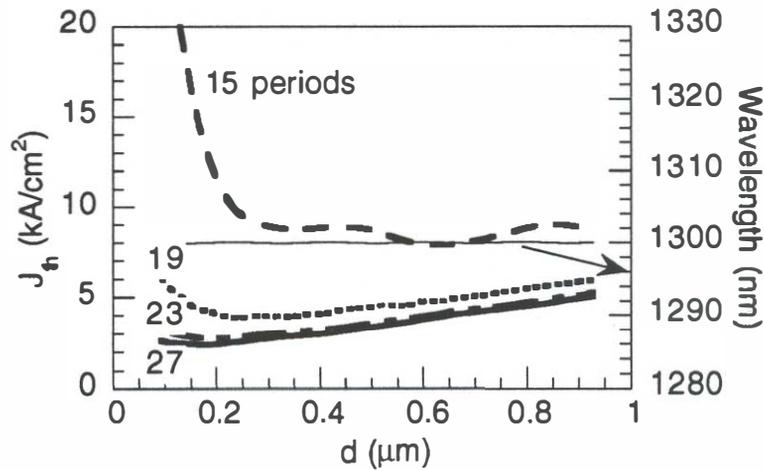


**Fig. 5.2** Threshold current density as a function of active layer thickness, $d$, for various number of GaAs/AlAs mirror periods keeping the *optical* length of the VCSEL cavity constant at 4.25 wavelengths. The total round-trip phase in the cavity is a multiple of $2\pi$ because the phase change at the GaAs/AlAs mirror ($\phi = \pi$) is different from the phase change at the Si/SiO$_2$ mirror ($\phi = 0$). The resulting cavity mode wavelength is shown on the right-hand axis.

Figure 5.2 shows that to achieve threshold current densities below 5 kA/cm$^2$, a GaAs/AlAs mirror with 19 periods (R = 98.97 %) is required. Lower thresholds can be achieved using 23 or 27 period mirrors. At active region thicknesses greater than 0.2 μm, however, there should be little difference between mirrors with more than 23 periods. Note that as the active region thickness decreases below 0.2 μm, the threshold current density starts to increase. As the active region thickness

decreases below 0.2 µm, more gain is required to overcome the losses in the cladding layers. Thus in VCSELs designed for maximum power output (i.e. lower mirror reflectivity), it is desirable to design the active region of the laser to be slightly greater than 0.2 µm thick to allow for variations in growth thickness. As the mirror loss decreases (i.e. the number of mirror periods increases), the increase in threshold current density with decreased active layer thickness becomes less pronounced. In devices designed for the minimum threshold current, active regions of 0.2 µm with 27 period mirrors are preferable.
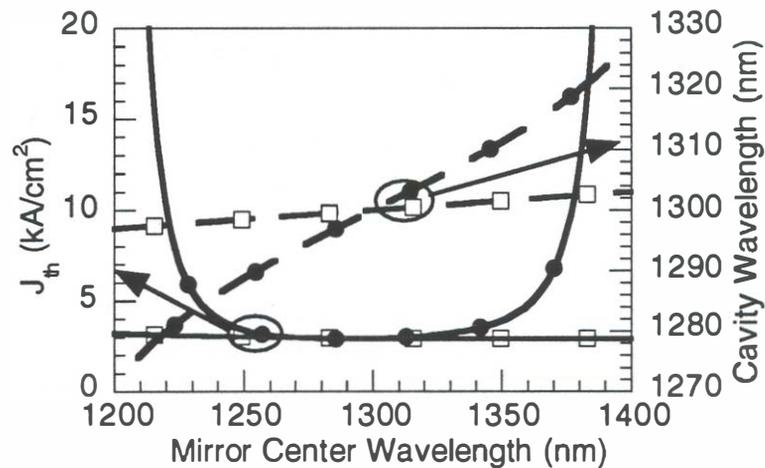


**Fig. 5.3** Effect of changing the mirror center wavelength on the threshold current (solid lines) and cavity mode (dashed lines) for a device with a 4-period Si/SiO$_2$ mirror and a 23-period GaAs/AlAs mirror. The effects of changing the peak wavelength of the GaAs/AlAs mirror (solid circles) is much greater than that of changing the center of the Si/SiO$_2$ mirror (hollow squares).

*Mirror Detuning*

The ability to deposit or grow mirrors with the desired center wavelength is still being developed. Thus, the designer must take into account possible variations in, or detunings of, the mirror center wavelength . The threshold current as a function of mirror center wavelength for a fixed optical thickness cavity (see Table 5.1 for dimensions) is given in Fig. 5.3. Note that the effect of detuning the center wavelength of the $Si/SiO_2$ mirror (hollow squares) is minimal because of the large optical bandwidth of the $Si/SiO_2$ mirror. The cavity wavelength changes by 5 nm for a mirror detuning of ±100 nm, while the threshold current density varies by 10 %. Thus, we there is a broad latitude of thickness variations for the $Si/SiO2$ mirror deposition.

The GaAs/AlAs mirror, however, is much more sensitive to variations in mirror center wavelength than the $Si/SiO_2$ mirror. The cavity mode changes wavelength by ±25 nm for the 200 nm mirror detuning shown. The threshold gain for this cavity structure also varies greatly, from less than 3 $kA/cm^2$ to more than 20 $kA/cm^2$. There is a 70 nm range over which the threshold current does not increase by more than 10 % from its minimum value. This translates into a growth accuracy of ±2.7 % for the GaAs/AlAs mirrors. Thus, careful calibration of growth rates and *in-situ* monitoring of the mirror reflectivity are necessary to achieve reproducible growth of these mirrors.

The effect of mirror detuning on the threshold current for various GaAs/AlAs mirror reflectivities is shown in Fig. 5.4. By increasing the number of periods in the GaAs/AlAs mirror, the flat, high reflectivity portion of the optical spectrum increases in width, resulting in less sensitivity of the threshold current on the mirror

detuning. Thus, if the center wavelength of the epitaxially grown mirrors is not well controlled it may be advantageous to use the GaAs/AlAs mirror for a high reflectivity mirror with 27 or more periods and to couple light out of the top mirror. This, however, can lead to resistance and heating problems in the GaAs/AlAs mirror.
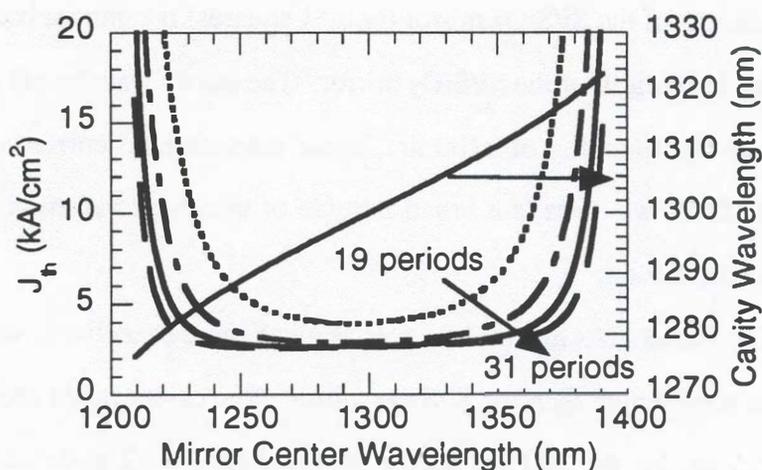


**Fig. 5.4** Effect of changing the center wavelength of the GaAs/AlAs mirror on the threshold current density and cavity mode for various number of GaAs/AlAs mirror periods. The number of mirror periods varies from 19 to 31 in steps of 4 periods.

*Temperature Sensitivity*

Vertical cavity lasers have inherent heating problems which can lead to active region temperatures 50 °C or more higher than the stage temperature, as shown in Chapter 2. Long wavelength material systems have large Auger recombination coefficients which increase quickly with temperature. The combination of these

two effects makes the achievement of room temperature, CW operation in a long

wavelength VCSEL a difficult task.
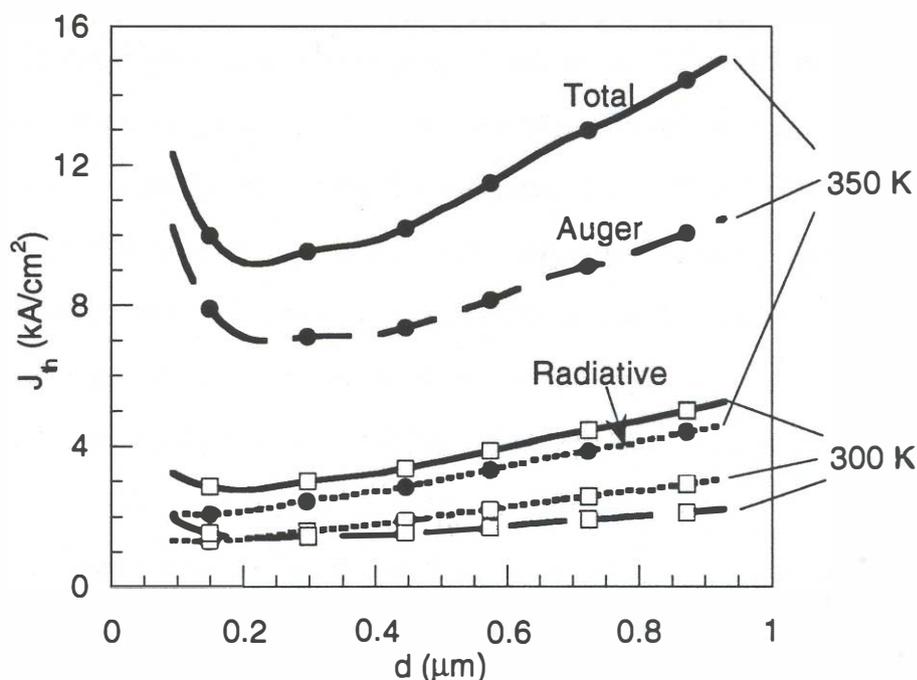


**Fig. 5.5** The threshold current density of a long wavelength VCSEL with a 23-period GaAs/AlAs mirror and a 4-period Si/SiO$_2$ mirror at 300 K (hollow squares) and at 350 K (solid circles). The contributions to the total current density (solid lines) from radiative recombination (small dashes) and Auger recombination (large dashes) are shown. (JthVsTemp_23pds)

Figure 5.5 shows the calculated threshold current density for a VCSEL with a

23-period GaAs/AlAs mirror at room temperature and at 350 K. At room

temperature, the radiative and non-radiative Auger components to the threshold

current density are approximately equivalent. However, as the temperature of the

device increases, the available gain for a given carrier density decreases, causing an

increase in the threshold carrier density and the radiative component of the threshold current density. Because of the third-power dependence of Auger recombination on the carrier density, and the increase in the Auger recombination coefficient with temperature, the Auger component of the threshold current density increases dramatically with the increase in temperature. At a temperature of 350 K, Auger recombination becomes the dominant effect, making up more than 70 % of the current necessary to reach threshold. Figure 5.5 points out the need for care in the thermal design of long wavelength VCSELs in order to achieve room temperature, CW operation. Note that at higher temperatures, the threshold current becomes more sensitive to active layers which are grown too thinly. Thus, it is necessary to use active layers thicker than 0.2 μm or to use more mirror periods to decrease the mirror loss.

In this analysis, I have not included the effects of the mismatch between the gain peak and cavity mode for temperatures other than the design temperature. I have assumed that the gain peak and cavity mode are matched at the temperature of operation. Thus, this is an optimistic assessment of the potential device performance. If the gain peak and cavity mode are matched at room temperature, the movement of the gain peak away from the cavity mode with heating will lead to even higher threshold currents than are calculated in Fig. 5.5.

*Implementation of the Design*

The active layer thickness and number of GaAs/AlAs mirror periods used in the electrically injected device discussed in this chapter are 0.3 μm and 27 periods. These values were chosen conservatively, as much of the work showing the effects

of fusing on mirror reflectivity and non-radiative recombination had not been undertaken at the time of the device design. Thus, a slightly thicker than optimal 0.3 $\mu$m active region is used along with a 27-period GaAs/AlAs mirror. Future designs should incorporate thinner active regions to decrease the threshold current, and fewer mirror periods to increase the light output. Multiple quantum well active layers are promising for the reduction of the threshold current and of the Auger recombination. Dubravko Babić is currently pursuing the use of quantum well active regions in fused VCSELs and will discuss their design and implementation in his dissertation.

## 5.3 Fabrication

In this section, I discuss the fabrication procedure for the wafer fused VCSELs studied in this chapter. The layer structures of the InP double heterostructure and GaAs/AlAs mirror wafers are given. The rest of the section gives a detailed description of the fabrication.
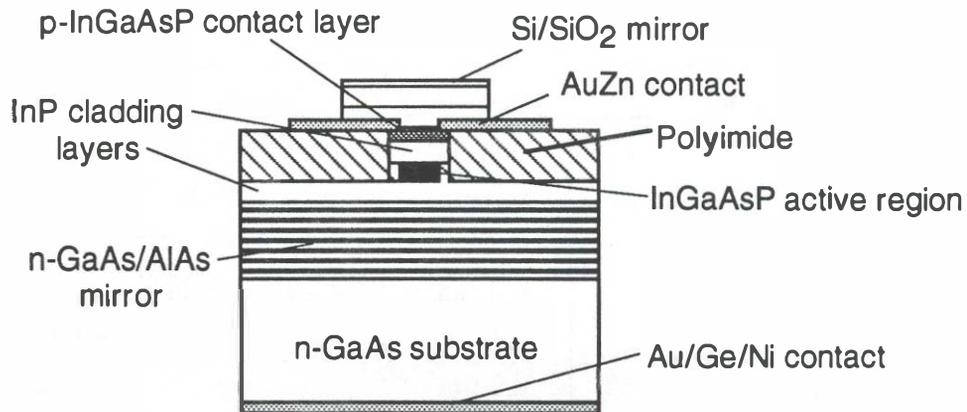
**Fig. 5.6** Schematic of the finished device structure.

*Wafer Structure*

A schematic of the finished wafer fused VCSEL structure is shown in Fig. 5.6. The InP double heterostructure wafer was grown by metalorganic vapor phase epitaxy (MOVPE) on a p-type (100) InP substrate. The complete wafer structure is shown in Table 5.4 and Fig. 5.7(a). Zinc was used for the *p*-type dopant, while S was used for the *n*-type dopant. The molecular-beam-epitaxy grown, *n*-type GaAs/AlAs mirror consists of 27 periods of quarter-wavelength thick layers of AlAs (112 nm) and GaAs (95 nm) grown on a GaAs substrate. The interfaces have a linearly changing, digitally-graded alloy composition with a period of 2 nm and a total length of 18 nm[7]. The top GaAs layer of the mirror is 1.25 wavelengths thick to prevent any bonding-induced strain from decreasing the mirror reflectivity. The top mirror is a 4-period $Si/SiO_2$ quarter wave mirror for coupling light out of the VCSEL.

**Table 5.4** The layer structure for the InP double heterostructure used in the wafer fused VCSEL.

| Material | Thickness | Doping | Comments |
|---|---|---|---|
| n-InP | 0.5 μm | $N_D = 1 \times 10^{18}$ cm$^{-3}$ | cladding layer |
| p-InGaAsP ($\lambda_{gap}$ = 1.3 μm) | 0.3 μm | $N_A = 2 \times 10^{17}$ cm$^{-3}$ | active layer |
| p-InP | 0.58 μm | $N_A = 1 \times 10^{18}$ cm$^{-3}$ | cladding layer |
| p-InGaAsP ($\lambda_{gap}$ = 1.1 μm) | 0.3 μm | $N_A = 2 \times 10^{18}$ cm$^{-3}$ | contact layer |
| p-InP | 0.2 μm | | buffer layer |
| p-InGaAs | 0.2 μm | | etch stop layer |
| p-InP | | | substrate |
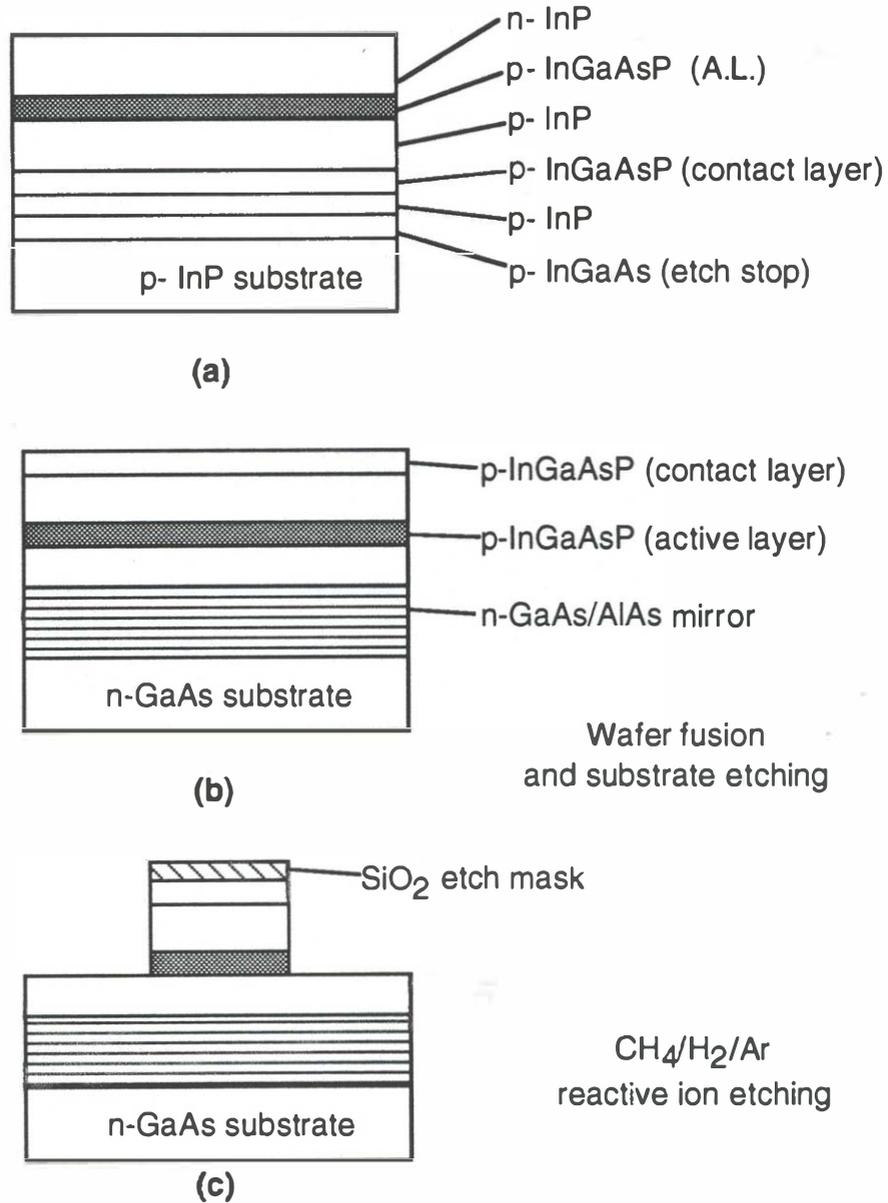
**Fig. 5.7** Schematic of the fabrication procedure for the wafer fused VCSELs.
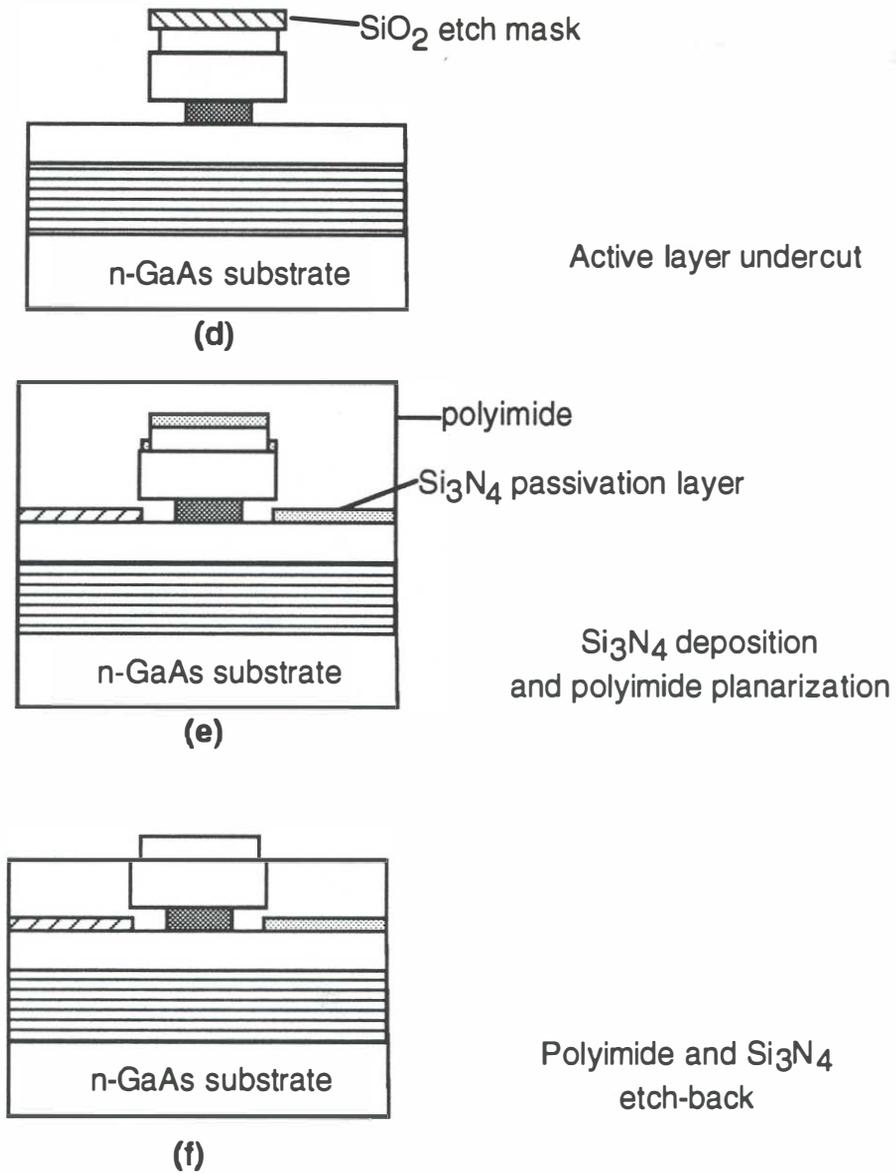
**Fig. 5.7** Schematic of the fabrication procedure (continued).

Pd/Zn/Pd/Au contact

(g)

AuGe/Ni/Au contact

Ring contact and back contact formation

Ni etch mask

Si/SiO$_2$ mirror

(h)

Mirror sputtering and patterning

(i)

Mirror etching and mask removal

n-GaAs substrate
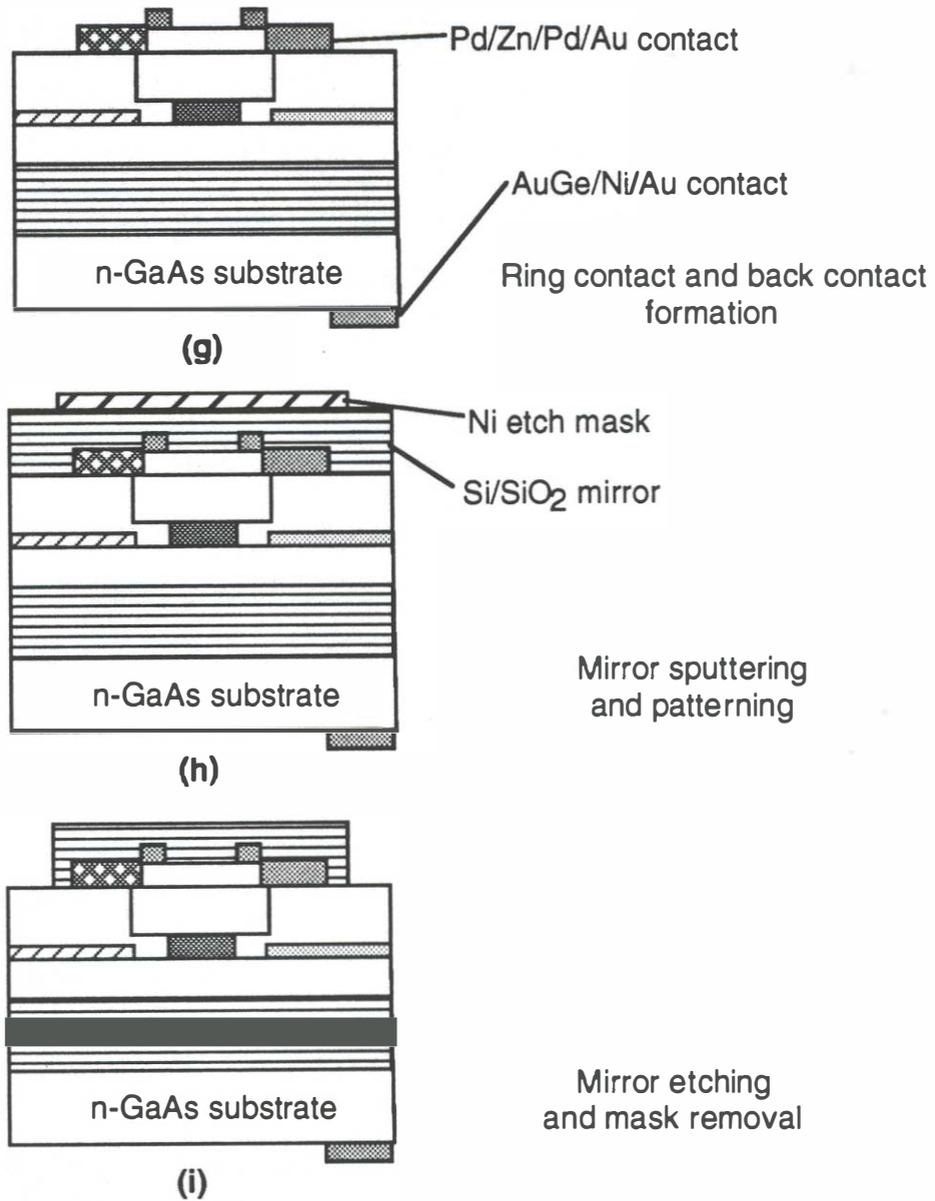
**Fig. 5.7** Schematic of the fabrication procedure (continued).

*Mesa Definition*

The fabrication procedure is shown in Fig. 5.7. The InP double heterostructure and the GaAs/AlAs mirror fuse together at 630 °C in an $H_2$ ambient for 30 min. After wafer fusion, the InP substrate is removed using an HCl solution to etch down to an InGaAs etch stop layer. Use of a separate InGaAs etch stop layer improves the reproducibility of the substrate removal process and the selectivity of the etching process compared to a process which uses an InGaAsP ($\lambda_{gap} = 1.1$ $\mu$m) etch stop layer. The thickness of the InGaAs etch stop layer has not been optimized, however. Layers less than 200 nm thick may also work well. Following the substrate removal, the InGaAs etch stop layer and the InP buffer layer are removed using selective wet chemical etchants [Fig. 5.7(b)]. The room temperature photoluminescence and photoreflectance of the sample is measured to determine the location of the optical mode and to demonstrate that the material is still optically active after the fusing process.

Next, a 3000 Å thick $SiO_2$ layer is deposited onto the InGaAsP contact layer using plasma enhanced chemical vapor deposition. The $SiO_2$ layer is patterned using photoresist and etched using buffered HF. The etch time is determined using a Si calibration sample having had $SiO_2$ deposited on it concurrently with the fused wafers. The calibration sample is put into buffered HF and monitored until the surface changes from a hydrophilic, $SiO_2$ covered surface to a hydrophobic Si surface. The $SiO_2$ on the fused sample is then etched for the amount of time that the Si piece was etched, and the photoresist mask is removed in acetone.

The patterned $SiO_2$ is used as a mask for $CH_4$:$H_2$:Ar reactive ion etching [Fig. 5.7(c)]. After cleaning the RIE chamber using an $O_2$ plasma and coating the

chamber with a $CH_4:H_2$ plasma, the patterned sample and a dummy sample are loaded onto the platen. A HeNe laser is used to monitor the etch depth on the dummy sample. The samples are etched using flow rates of 4, 20, and 10 sccm for $CH_4$, $H_2$, and Ar at a total pressure of 75 mTorr. To ensure a more vertical profile, the self-bias voltage starts at 250 V and is increased to 500 V after the first 6 minutes. Once the active layer is reached, any polymers which may have formed on the $SiO_2$ etch mask are removed using an $O_2$ plasma. Then the etch depth is confirmed with a surface profilometer.
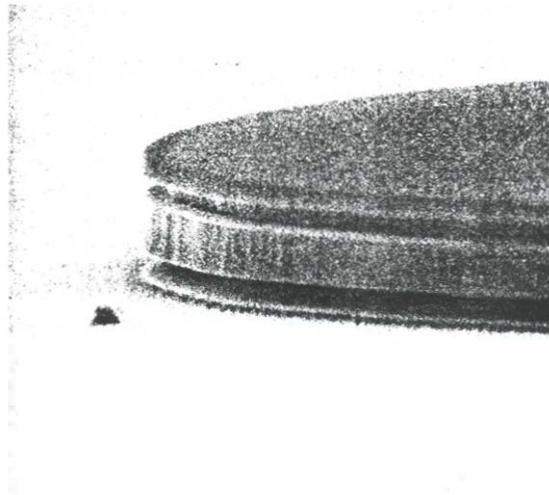


**Fig. 5.8** Scanning electron micrograph of a VCSEL mesa after reactive ion etching and active layer undercut. The top layer of the mesa is the $SiO_2$ mask.

The $SiO_2$ mask which was used for etching the mesas acts as a self-aligned mask for creating a constricted mesa [Fig. 5.7(d)]. The active layer is undercut using a room temperature mixture of $H_2SO_4:H_2O_2:H_2O$ in a ratio of 3:1:5. The etching is monitored using test mesas of 6, 8, and 10 $\mu$m diameters on the sample.

After etching for one-to-two minutes, the test mesas are examined with an optical microscope to determine if they have been etched through. This etching-examination procedure is repeated until the 10 μm diameter mesas are removed. To prevent the test mesas from redepositing on the surface after being etched off, the sample is held upside down during the etching. After etching, the undercut profile is examined using the scanning electron microscope (SEM) as shown in Fig. 5.8. Note that in addition to the active region, the top contact layer has also been slightly undercut. Although there is etch selectivity between different compositions of InGaAsP, it is not large enough to prevent some of the contact layer from being removed. The removal of part of the contact layer will increase the *p*-contact resistance as some of the metal will alloy with InP instead of the InGaAsP contact layer.

*Isolation and Metallization*

Following the active layer undercut, the $SiO_2$ mask is removed in HF and a $SiN_x$ passivation layer is sputter deposited everywhere on the surface of the sample [Fig. 5.7(e)]. The color of the $SiN_x$ film is noted for reference later in the process. Next, a polyimide film is spin-cast to achieve electrical isolation between the top contact and the n-type InP layer. The polyimide is cured in a $N_2$ environment, gradually increasing the temperature until the temperature of the final alloy step is achieved. The temperature is then ramped down slowly. The $N_2$ environment is used because it has been found to give less brittle films than curing in air[8]. It is important to ramp the temperature up and down slowly. Rapid temperature changes cause the mesas to break due to the difference in thermal expansion coefficients

between the polyimide and the InP. The final temperature is chosen to be the contact alloy temperature. Experiments in which the polyimide was cured at lower temperatures often led to bubbles appearing under the top contact film after alloying, indicating the release of solvents from the polyimide. Following the curing, a 3 $\mu$m thick layer of photoresist is spin casted to improve the planarity of the surface.

Figure 5.7(f) shows the device after the polyimide and $Si_3N_4$ etch back. The polyimide is etched in $O_2$ plasma. After every 2-to-5 minute etch, the sample is examined using an optical microscope to check the progress of the etching. When the top of the mesas has the color of the $SiN_x$ film, the polyimide removal is complete. The samples are then etched in $CF_4$ plasma to remove the $SiN_x$ film. The smaller diameter mesas ($\leq 26$ $\mu$m) complete etching first because the polyimide is more planar across the tops of the smaller mesas. Because of the large difference in size between the smallest 16-$\mu$m and largest 40-$\mu$m diameter mesas, it is not possible to remove the polyimide from the 40 $\mu$m mesas without completely removing it from around the 16 $\mu$m mesas. This could be improved in later devices by including an additional mask step to open holes in the photoresist above the largest diameter mesas.

After the tops of the mesas have been cleared of polyimide and $SiN_x$, the top ring contact consisting of Pd/Zn/Pd/Au in thicknesses of 100 Å/ 50 Å/ 300 Å/ 2000 Å is evaporated and patterned using standard lift-off techniques. Next, a AuGe/Ni/Au contact is evaporated onto the back side of the device. A piece of Si or cover glass is used to cover most of the back side of the sample, so that the contact is made on one side of the wafer [Fig. 5.7(g)] while

light can be detected across the remainder of the GaAs substrate. Using this shadow mask eliminates one mask step and the need for a back side alignment. The contacts are alloyed using a rapid thermal annealer at 410 °C for 30 sec. in a $N_2$ ambient. After alloying, electrical and optical measurements are made on the device. The spectra, light-current characteristics, and current-voltage characteristics of the fused LED are measured as a process check.

*Mirror Definition*

To turn the LED into a laser, the top mirror is reactively sputtered onto the device [Fig. 5.7(h)]. A 4-period Si/SiO$_2$ mirror is sputtered using Ar as the sputtering gas and introducing $O_2$ to react with the Si to form the $SiO_2$ layers. A laser monitor is used to determine the deposition rate of the mirror layers. Because the laser monitor is at 1.3 μm wavelength, the layers are deposited until a peak or a trough is reached in the reflectivity[9,10]. Then the sample is removed from the plasma and the sputtering gasses are switched before the next layer is deposited. In this way very accurate control over the layer thickness can be achieved, resulting in the placement of the center wavelength of the mirror at the desired location. After the mirror deposition, a Ni etch mask is deposited on top of the mirror and patterned using standard liftoff techniques. Nickel is chosen for the etch mask because it is not attacked by the plasma which is used to etch the mirror.

The mirror is etched using RIE with $CF_4$ as the etch gas at a flow rate of 25 sccm, a pressure of 50 mTorr, and a self-bias voltage of 500 V. The Si layers tend to etch faster than the $SiO_2$ layers, resulting in undercutting of less than 0.5 μm in the Si layers of the 1.3 μm thick mirror. The end point of the etch is determined by

measuring current continuity in the lasers. If the mirror is overetched, the Au contacts and contact pads become exposed to the plasma. The plasma then sputters the contacts, resulting in short-circuited devices. Thus, endpoint determination in the mirror etching is critical. The problem of sputtering the contacts could be solved by etching the mirror at lower self-bias voltages. However, this would result in more sloped sidewalls. After the mirror etch is complete, the Ni etch mask is removed using a commercially available $FeCl_3$ solution[11]. Although this mixture contains HCl, it does not etch the InP layers because they are protected by the polyimide layer.
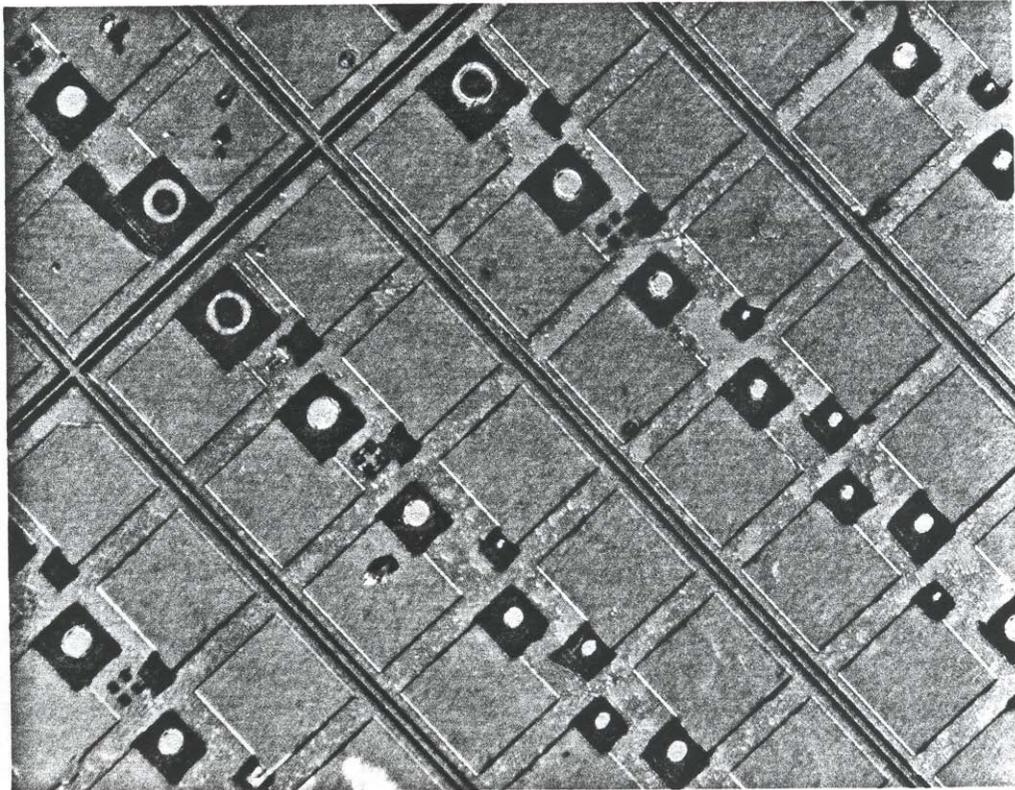


**Fig. 5.9** An array of finished VCSELs.

The etching of the mirror etch mask completes the VCSEL fabrication process [Fig. 5.7(i)]. A photograph of the finished device is shown in Fig. 5.9.

## 5.4 Room Temperature Characteristics

Several measurements have been made at room temperature to characterize the wafer fused VCSELs. In this section I will describe those measurements, beginning with the light-current characteristics and the spectrum. The polarization properties of the devices will then be explored. Then the near field and far field patterns will be examined.

*Light-current Characteristics*

The devices are characterized at a stage temperature of 300 K under pulsed operation using 100 nsec, 20 kHz pulses. Light is measured out of the top $Si/SiO_2$ mirror. The data is recorded using software which I wrote in the Labview programming environment on the Macintosh. The software controls the input voltage using a function generator, records the input current and light output, and downloads the measured spectrum from an optical spectrum analyzer. It is also used to record line scans from a digital oscilloscope for measuring the near field pattern.

The 11 µm diameter active region VCSELs operate pulsed at a stage temperature of 300 K with a threshold current of 9 mA and a threshold current density of 9 kA/cm$^2$ (Fig. 5.10). These are the lowest reported threshold current and threshold current density at room temperature to date for a long wavelength VCSEL. The lasers operate in a single longitudinal mode at 1301 nm with a full

width at half-maximum of the spectra of 0.15 nm. The measurement of the spectral full width is limited by the resolution of the optical spectrum analyzer.
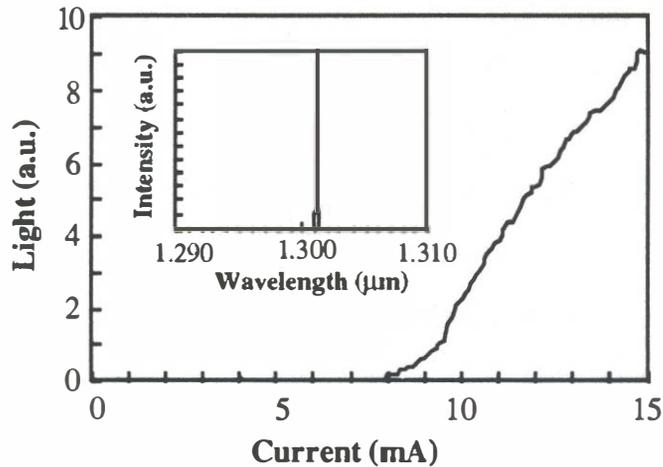


**Fig. 5.10** Room temperature, pulsed light-current and spectra characteristics of an 11 μm active layer laser.

The differential resistance and voltage of the device at threshold are 300 Ω and 4 V. From contact resistance measurements made on similar material, I estimate that the maximum contribution from the $p$-type ring contact of area 125 μm$^2$ is 80 Ω, while the GaAs/AlAs mirror accounts for most of the remainder of the resistance. Future device performance should be enhanced by optimization of the GaAs/AlAs mirror structure to achieve lower threshold voltages. The resistance of the top contact is increased by having the InGaAsP ($\lambda_{gap}$ = 1.1 μm) contact layer etched during the active layer etching. Lower contact resistances are achievable by adding a $p$-InGaAs contact layer and grading the bandgap of the contact material from the ternary composition to InP[12]. With this contact scheme, contact resistances of $1.5 \times 10^{-6}$ Ω-cm$^2$ have been measured, including the effects of the heterobarrier in the contact. This would lead to contact resistances of approximately

$1\ \Omega$. The InGaAs layer must be removed from the output window, however, to prevent increased absorption losses because of the smaller bandgap of InGaAs compared to the active layer.

The differential quantum efficiency of these lasers is approximately 0.5 %. This can be improved by increasing the injection efficiency through the incorporation of a current spreading layer in the structure to increase the overlap between the injected carriers and the optical mode. Further improvements can be made by reducing the loss in the dielectric mirror by replacing the absorptive $\alpha$-Si layers in the $Si/SiO_2$ mirror with a low-loss material such as $TiO_2$ and by better matching the gain peak and cavity mode at room temperature, as will be discussed in the next section.

*Polarization*

Figure 5.11 shows the light output as a function of input current for an 11 $\mu$m diameter active region device with a polarizer placed in front of the detector. The L-I curve marked "Polarizer at 0°" has the polarizer aligned such that the maximum amount of light is transmitted to the detector with the polarizer at this angle. This corresponds to the polarization axis being aligned with one of the (011) crystal axes. When the polarizer is rotated 90°, some light is still observed at the detector. This indicates that the mode coming from the fused VCSEL is not completely linearly polarized, but is slightly elliptically polarized. As the input current increases, the angle for which the maximum light output occurs remains constant.

More than 10 devices across the wafer were studied to see if there were any trends in the polarization characteristics. All of these devices had slightly elliptically

polarized modes, with the polarization angle aligned with the same (011) crystal axis as in the device whose polarization properties are shown in Fig. 5.11. The uniformity of the polarization across the wafer eliminates the possibility that the preferred polarization angle is effected by some non-uniformity in the material properties.
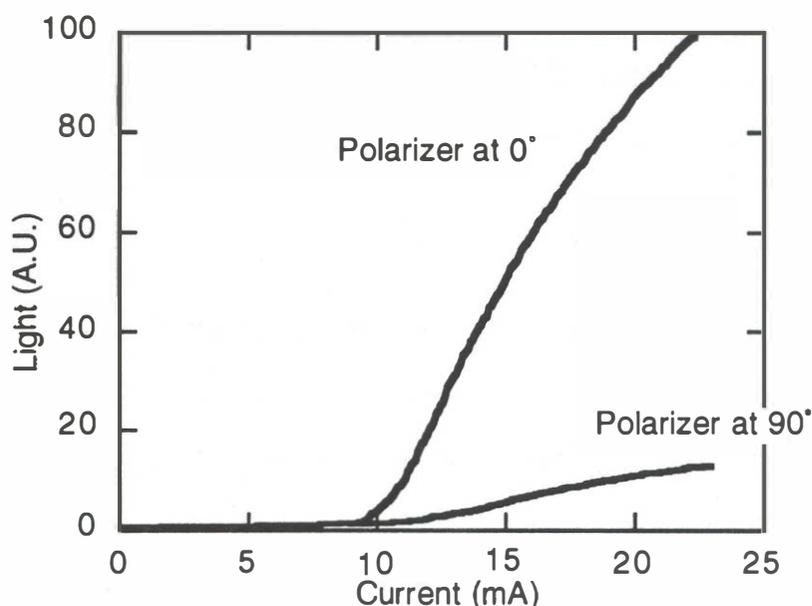
**Fig. 5.11** Light-current characteristics with a polarizer in front of the detector. When the polarizer is at 0°, the maximum signal is received at the detector.

A perfect cylindrical waveguide would have linear polarization in the lowest order mode, but the direction of the polarization would be random. Thus, it is interesting that in these devices the polarization tends to be directed along the same (011) crystal axis. Because the active region which is used in this device is made of bulk material, there is no reason that the gain should have a preferred polarization

direction. The only other possibility is that the fabrication process has created an anisotropy in the optical waveguide to affect the optical loss and hence the preferred polarization direction. The most likely candidate to create this anisotropy would be non-uniformity in the wet etching of the active and contact layers. However, it is also possible that the preferred polarization direction is caused by a non-uniformity in the current injection caused by misalignment of the top ring contact or by a bonding-induced stress. The issue of polarization is an important one which needs to be solved so that VCSELs can be implemented in systems, as most systems tend to have at least one polarization sensitive device (e.g. an optical switch).

*Near Field Pattern*

Figure 5.12 shows the near field pattern of an 11 μm diameter active region device under pulsed operation at room temperature. The near field is measured by imaging the output of the VCSEL onto an infrared camera using a microscope. A line scan through the center of each mode is taken by directing the output of the infrared camera to a digital oscilloscope and downloading the line scan onto a Macintosh computer using Labview.

Just above threshold (Fig. 5.12(a)), the laser operates in the circularly symmetric, fundamental transverse mode with a single lobe in the center of the output window. At two times threshold (Fig. 5.12(b)), the emission pattern changes to the higher order modes with two lobes. The dominance of the higher order mode is due to non-uniformity of the carrier distribution which is caused by spatial hole burning[13,14] and non-uniform current injection into the active layer from the ring contact[15,16].
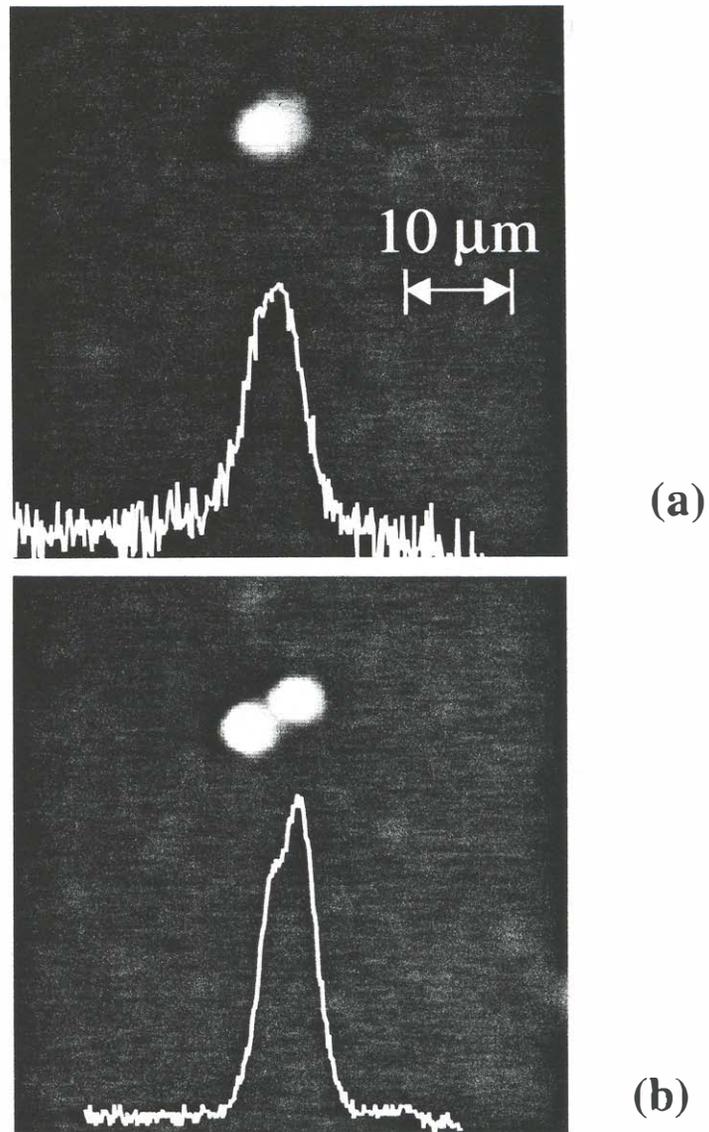
**Fig. 5.12** Near field characteristics at room temperature (a) at 1.1 $I_{threshold}$ and (b) at 2 $I_{threshold}$.

*Far Field Pattern*

The far field pattern for an 11 μm diameter active region device operating at room temperature under pulsed conditions is shown in Fig. 5.13. The far field is

measured as shown in Fig. 5.14. A Ge detector is mounted below one end of a post which pivots on a potentiometer at the other end of the post. The fused VCSEL is centered below the potentiometer. A constant current is driven through the potentiometer. As the post rotates from -90° to +90°, the detector moves and the resistance of the potentiometer varies, causing the voltage across the potentiometer to change. The voltage across the potentiometer is measured and plotted against the current from the detector using an x-y plotter.
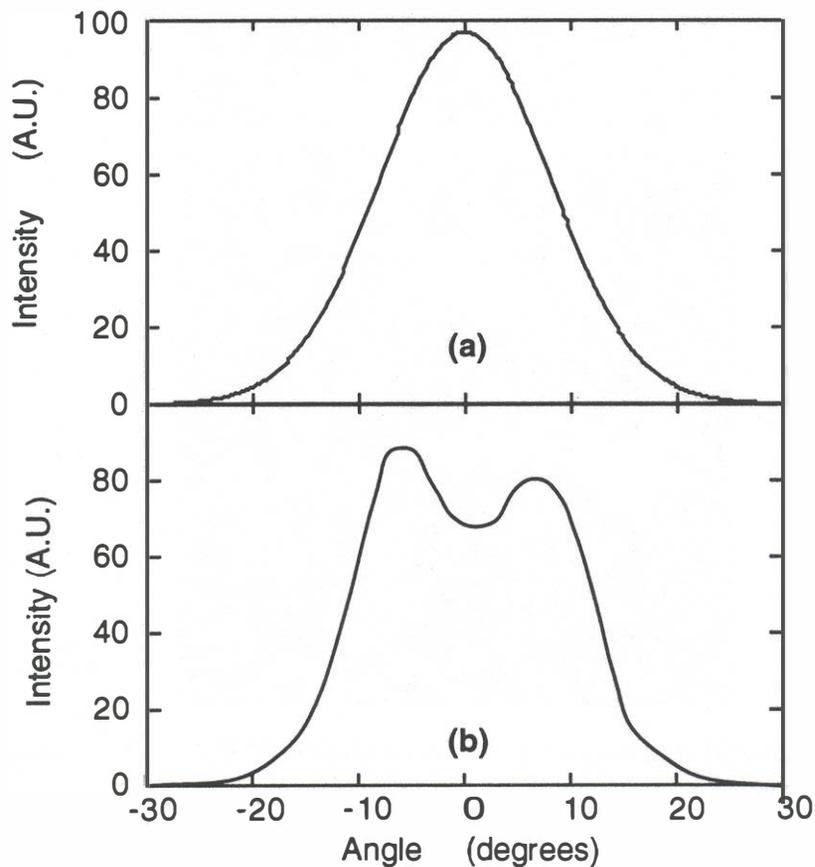


**Fig. 5.13** Far field characteristics at room temperature (a) just above threshold and (b) at 2 $I_{threshold}$.

Just above threshold [Fig. 5.13(a)], the far field pattern has a single lobe with a full width at half maximum of 19 degrees. The far field pattern is symmetric when the detector is swept across the direction perpendicular to the first measurement.

As the input current increases, a second order mode appears in the far field at two times threshold, as shown in Fig. 5.13(b). This is expected from the measurements of the near field pattern, in which a second order mode appeared at twice threshold.
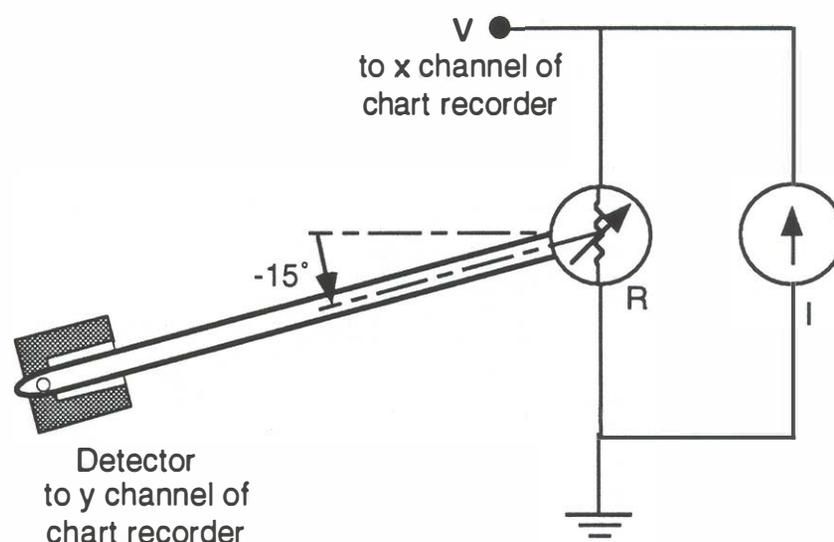


**Fig. 5.14** Diagram of the apparatus used for measuring the far field pattern.

## 5.5 Temperature Dependent Characteristics

A significant difference between in-plane lasers and VCSELs is the behavior of the threshold current with temperature[17]. This difference is caused by the difference in size of the devices. With their long optical cavities, in-plane lasers have several closely spaced longitudinal modes and the gain spectra spans several of the cavity

modes. In a VCSEL, however, the short cavity gives a greater separation between longitudinal modes than can be spanned by the gain spectrum. The VCSEL must lase at the frequency of the single cavity mode, causing the threshold current to have a minimum where the gain peak and cavity mode are aligned. Thus, measuring the threshold current variation as a function of temperature in a VCSEL provides an important diagnostic tool to determine the displacement of the gain peak from the cavity mode. In this section I present and analyze measurements of threshold current variation with temperature. I discuss in detail the differences between VCSELs and in-plane lasers. Finally, I look at the issue of non-uniform current injection.
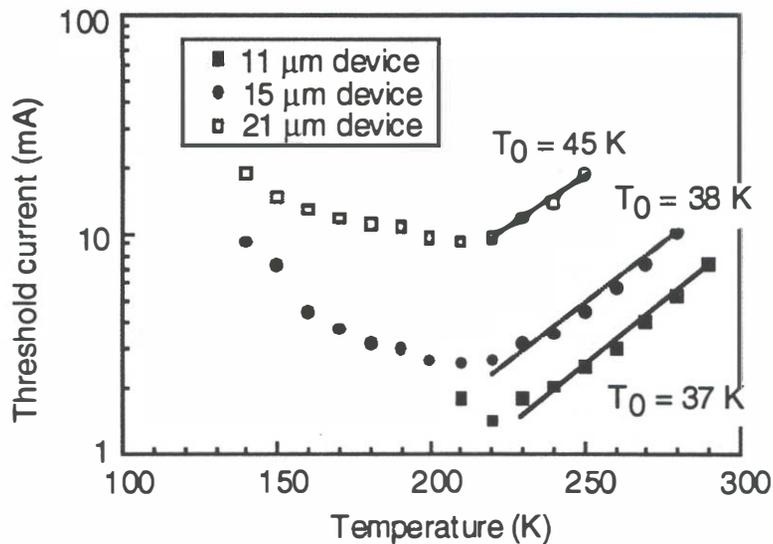


**Fig. 5.15** Threshold current as a function of temperature for 11, 15, and 21 μm active region devices.

*Temperature Dependence of Threshold*

Figure 5.15 shows the measured threshold current as a function of temperature for devices with three different active layer diameters: 11, 15, and 21 μm. The three different devices were located on adjacent cells on the wafer to minimize the effects on the measured characteristics of any variations in the layer thicknesses, mirror properties, or crystal quality. The measurement is taken under pulsed conditions to eliminate active layer heating. Thus, the active region temperature should be very close to the measured stage temperature.

The stage temperature is varied from 140 to 300 K in 10 K intervals. As the temperature is increased from 140 K, the threshold current decreases until a minimum is reached for each device size at a temperature of 210 (15 and 21 μm diameter) or 220 K (11 μm diameter). This indicates that the gain peak and cavity mode are matched at 80-90 °C below room temperature. The large mismatch of the gain peak and cavity mode prevents room temperature, CW operation of these devices. The maximum CW operation temperature of these devices is 230 K with a threshold current of 3.6 mA, as shown in Fig. 5.16.

As the temperature increases from 220 K, the threshold current rises in an exponential fashion which can be described using the phenomenological relationship

$$I_{th} \propto \exp\left(T/T_0\right). \tag{5-5}$$

Near room temperature, the 11 μm device has a $T_0$ of 37 K, while the 15 μm device has a $T_0$ of 38 K. Between 220 and 250 K the 21 μm device has a $T_0$ of 45 K.
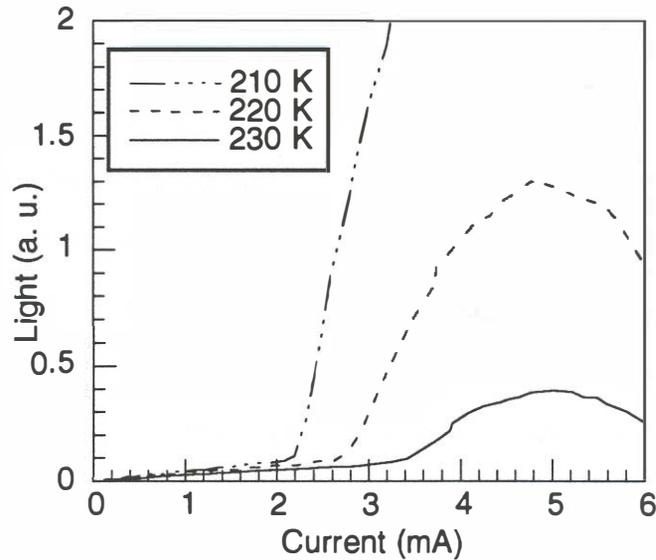
**Fig. 5.16** Continuous wave light-current characteristics at 210, 220, and 230 K for 11 μm active region devices.

Note that although Eq. (5-5) can be used to describe the entire temperature range of operation for an in-plane laser, it only describes that temperature region *above* the temperature of minimum threshold in a VCSEL which is operated under pulsed bias[17,18,19]. The temperature characteristics of the VCSEL differ in nature from the characteristics of an in-plane laser. The difference in the characteristics can be understood by looking at the relationship between the gain peak and cavity modes in the two different devices, as shown in Fig. 5.17. In the in-plane laser, there are several closely spaced cavity modes due to the long length of the cavity (typically 300 μm). As any laser heats up, the gain peak and cavity modes of the laser shift. For a laser with an InGaAsP active region, the gain peak moves at a rate of approximately 5 Å/°C, while the cavity modes move at around 1 Å/°C. Thus,

the gain peak red shifts in relationship to the cavity modes. In a Fabry-Perot in-plane laser, this means that the peak of the gain spectrum shifts to longer wavelength cavity modes and the lasing wavelength shifts to those modes.
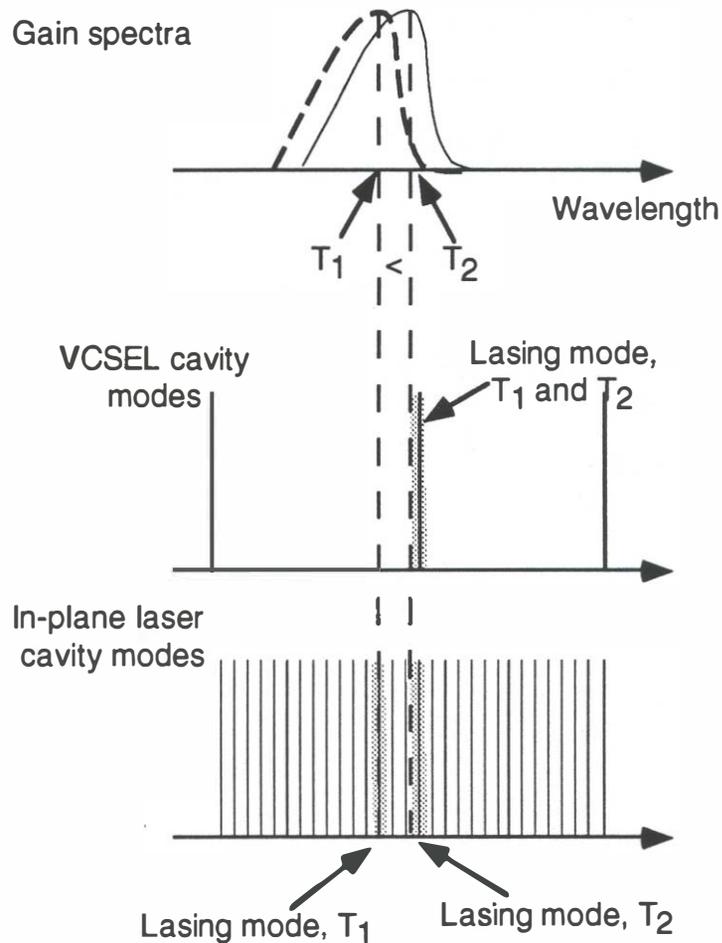


**Fig. 5.17** Comparison of the cavity modes in VCSELs and in-plane lasers, and the relationship of the mode spacing with the gain spectra.

In a VCSEL, however, the spacing between longitudinal modes is typically larger than the gain bandwidth due to the short length of the cavity. Thus as the device heats up, the gain peak red shifts in relationship to the cavity mode. When

the gain peak is at a shorter wavelength than the cavity mode, an increase in temperature results in a decrease in the threshold current because the gain peak moves towards resonance with the cavity mode. The minimum in threshold current occurs when the gain peak and cavity mode are aligned at the same wavelength. As the temperature increases further, the threshold increases because the gain peak moves out of resonance with the cavity mode.
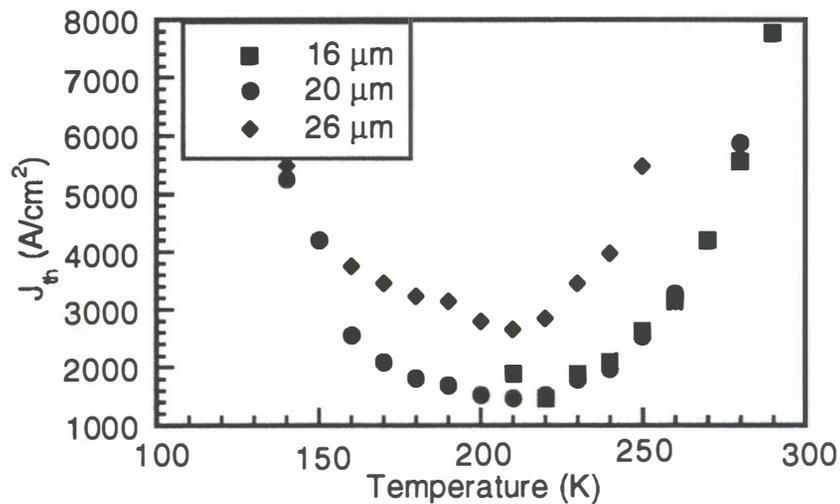


**Fig. 5.18** Threshold current density as a function of temperature for 11, 15, and 21 μm active region devices.

*:Non-uniform Injection*

If the current injection in the devices is uniform, the threshold current density for each device size should be the same. I explored this for the three device sizes discussed above. The threshold current density as a function of temperature for different device sizes is shown in Fig. 5.18. Note that $J_{th}$ for the 11 and 15 μm

devices are the same from 210 to 280 K, while the larger area 21 μm device has higher threshold current densities at all temperatures. As the device size increases and as the current level increases, the current injection becomes more non-uniform[15,16]. From the data shown in Figs. 5.15 and 5.18, it appears that non-uniform injection becomes a problem as the current level increases above 10 mA. This is corroborated by the observation in Figs. 5.12 and 5.13 that a second order transverse mode appears near a current level of 18 mA for an 11 μm diameter device.

Qualitative comparisons can be made between these results and the results of Wada et al.[16]. The active layer areas which he studied were similar to the ones in these fused VCSELs. Because both sets of devices used at least one ring contact, similar physical processes will result during the current injection. Wada's measurements agree with my observation that for devices with areas on the order of 100 μm$^2$ and larger, and current levels of 10 mA or greater, non-uniform injection becomes a problem. One should be careful in making exact comparisons between the two sets of data, however, as Wada's etched hole VCSEL used two ring contacts to inject current, had thicker InP cladding layers ($n$-InP = 2 μm and $p$-InP = 1.5 μm) to inject the current through, and had an active layer twice as thick ($d$ = 0.6 μm) as those of this fused VCSEL.

## 5.6  Conclusions

This chapter described the design, fabrication, and characterization of electrically injected, long wavelength VCSELs on GaAs substrates. The wafer fused VCSELs operate at record low threshold currents and threshold current densities at room

temperature due to the incorporation of high reflectivity GaAs/AlAs mirrors. The narrow beam divergence angle and circular output demonstrated in the far field measurements make these devices ideal for coupling into optical fibers. The self-aligned fabrication procedure utilizes optical monitoring to ensure precise etching depth of the InP double heterostructure and precise thickness control of the reactively sputtered Si/SiO$_2$ mirror.

Measurements discussed in this chapter point to possible improvements in this device structure which should lead to higher CW operation temperatures and improved quantum efficiencies. Foremost among the improvements is better matching of the gain peak and cavity mode at room temperature. Decreased device resistance, improved carrier uniformity at high injection levels, and lowered loss in the output mirror also need to be achieved.

The solution of these problems and the goal of designing an easily manufactured device have led me to the development of a new device structure. This *double-fused*, long wavelength VCSEL looks similar to an (In)GaAs VCSEL, with the exception that it uses InGaAsP active regions. The design and development of the double-fused VCSEL will be discussed in the next chapter.

# References

[1]     Bjork, G. and Nilsson, O., "A New Exact and Efficient Numerical Matrix Theory of Complicated Laser Structures: Properties of Asymmetric Phase-Shifted DFB Lasers," *IEEE Journal of Lightwave Technology*, vol. 5, 140, 1987.

[2]     Corzine, S.W., "Design of Vertical-Cavity Surface-Emitting Lasers with Strained and Unstrained Quantum Well Active Regions," Ph.D. thesis, Appendix H, UCSB, 1993.

[3]     Agrawal, G.P. and Dutta, N.K., *Long-Wavelength Semiconductor Lasers.* Van Nostrand Reinhold, 1986.

[4]     Dutta, N.K. and Nelson, R.J., "The Case for Auger Recombination in InGaAsP," *Journal of Applied Physics*, vol. 53, no. 1, 74-92, Jan. 1982.

[5]     Uchiyama, S. and Iga, K., "Consideration On Threshold Current Density Of GaInAsP/InP Surface Emitting Junction Lasers," *IEEE Journal Of Quantum Electronics*, vol. QE-22, no. 2, 302-9, Feb. 1986.

[6]     Iga, K., Koyama, F., and Kinoshita, S., "Surface Emitting Semiconductor Lasers," *IEEE Journal Of Quantum Electronics*, vol. 24, no. 9, 1845-55, Sept. 1988.

[7]     Geels, R.S., Corzine, S.W., and Coldren, L.A., "InGaAs Vertical-Cavity Surface-Emitting Lasers," *IEEE Journal Of Quantum Electronics*, vol. 27, no. 6, 1359-67, Jun 1991.

[8]     *Soluble Polyimides for Microelectronics, Probimide 200 Series, Physical, Electrical and Chemical Properties*, Ciba-Geigy Corp., Hawthorne, N.Y..

[9]     Dudley, J.J., Melcer, L., Bowers, J.E., Hu, E., and Storz, F., "Surface Emitting GaInAsP/InP Lasers," *LEOS Annual Meeting Proceedings*, OE11.3, 1989.

[10]    Babić, D.I., Dudley, J.J., Shirazi, M., Hu, E.L., and Bowers, J.E., "Sputter Deposition of Precision Si/Si3N4 Bragg Reflectors Using Multi-Tasking Interactive Processing Control," *Journal of Vacuum Science and Technology A*, vol. 9, no. 3, 1113-17, May/June 1991.

[11]    *PC BoardEtching Solution*, Manufactured by CG Electronics, 1801 Morgan St., Rockford, Ill..

[12]    Wey, Y.G., "High-speed DoubleHeterostructure GaInAs/InP p-i-n Photodiodes : Theory, Fabrication, and Measurement," Ph.D. thesis, UCSB, 1993.

[13] Scott, J.W., Geels, R.S., Corzine, S.W., and Coldren, L.A., "Modeling Temperature Effects And Spatial Hole Burning To Optimize Vertical-Cavity Surface-Emitting Laser Performance," *IEEE Journal Of Quantum Electronics*, vol. 29, no. 5, 1295-1308, May 1993.

[14] Wilson, G.C., Kuchta, D.M., Walker, J.D., and Smith, J.S., "Spatial Hole Burning And Self-Focusing In Vertical-Cavity Surface-Emitting Laser Diodes," *Applied Physics Letters*, vol. 64, no. 5, 542-4, 31 Jan. 1994.

[15] Joyce, W.B. and Wemple, S.H., "Steady-State Junction-Current Distributions In Thin Resistive Films On Semiconductor Junctions," *Journal Of Applied Physics*, vol. 41, no. 9, 3818-30, Aug. 1970.

[16] Wada, H., Babić, D.I., Ishikawa, M., and Bowers, J.E., "Effects Of Nonuniform Current Injection In GaInAsP/InP Vertical-Cavity Lasers," *Applied Physics Letters*, vol. 60, no. 24, 2974-2976, Jun 15 1992.

[17] Tell, B., Brown-goebeler, K.F., Leibenguth, R.E., Baez, F.M., and Lee, Y.H., "Temperature Dependence Of GaAs-AlGaAs Vertical Cavity Surface Emitting Lasers," *Applied Physics Letters*, vol. 60, no. 6, 683-5, 10 Feb. 1992.

[18] Kubota, S., Koyama, F., and Iga, K., "Low-Threshold GaInAsP/InP Transmission-Type Surface Emitting Laser," *Japanese Journal Of Applied Physics, Part 2 (Letters)*, vol. 31, no. 2B, L175-6, 15 Feb. 1992.

[19] Young, D.B., Scott, J.W., Peters, F.H., Thibeault, B.J., Corzine, S.W., Peters, M.G., Lee, S.L., and Coldren, L.A., "High-Power Temperature-Insensitive Gain-Offset InGaAs/GaAs Vertical-Cavity Surface-Emitting Lasers," *IEEE Photonic Technology Letters*, vol. 5, 129-32, Feb. 1993.

## Chapter 6
# Summary and Future Research

### 6.1 Introduction

The realization of practical long wavelength VCSELs has been an arduous and formidable task over the past several years. The purpose of this thesis has been to significantly advance the state of the art by introducing a novel method for the design and fabrication of long wavelength VCSELs. This method of integrating InGaAsP active regions with high reflectivity GaAs/AlAs mirrors is one of the most promising approaches for the transformation of long wavelength VCSELs from a laboratory curiosity into a commercially viable product. Through the use of wafer fused devices, the goals of a cheap, easily manufactured, and single frequency source at 1.3 and 1.55 μm may soon be achieved. Refinement of the device design presented in this dissertation should readily lead to room temperature, CW operation with threshold currents less than 5 mA.

In this chapter, I will discuss future directions for research on wafer fused VCSELs which should lead to the performance level stated above. I will also look

at other directions for research involving wafer fusing, including the study of the band structure of various heterostructures which cannot be grown epitaxially and the development of three-color displays. Before discussing future research, however, I will summarize the work which has been presented in this dissertation, suggest refinements in the device design to achieve higher temperature CW operation, and describe how the work of this dissertation has influenced other researchers at UCSB.

## 6.2 Summary

The most prominent achievements in this work have been the design, demonstration, and understanding of electrically injected, wafer fused VCSELs. Using the technique of wafer fusion, I demonstrated a unique approach in the design of long wavelength VCSELs: the use of non-lattice matched GaAs/AlAs multilayer structures to form an electrically and thermally conductive high reflectivity mirror. This design addressed several important issues in the realization of practical long wavelength VCSELs.

### Design Issues and Implementation

The most fundamental method to achieve lower threshold currents in a semiconductor laser is to increase the mirror reflectivity. In Chapter 2, I showed that the plane-wave reflectivities of GaAs-based mirrors are significantly higher than those of InP-based mirrors. At 1.3 $\mu$m wavelength, the amount of material necessary to achieve high reflectivities is too much to make InP mirrors practical. In addition to improved plane wave reflectivities, the smaller refractive index ratio

in GaAs mirrors leads to decreased diffraction loss and reduced penetration depths compared to InP mirrors.

By injecting current through the GaAs/AlAs mirror, the problem of non-uniform current injection was reduced compared to previous etched well devices. The use of the GaAs mirror led to devices with lower thermal resistances than devices which utilize two deposited mirrors or a combination of one InP/InGaAsP and one deposited mirror. Because of the large, temperature sensitive Auger recombination coefficient in the InGaAsP material system, the threshold current can increase rapidly with temperature in a long wavelength VCSEL, as discussed in Chapter 5. Thus, the design of devices with decreased thermal resistances is important to increase the range of temperatures and input powers over which these devices can operate CW. The fused VCSEL has improved thermal properties because the GaAs mirror has more than three times the thermal conductivity of an InP mirror and more than ten times the thermal conductivity of most insulating mirrors.

The design of the wafer fused VCSELs made possible improvements in the thermal properties of long wavelength VCSELs, minimization in current crowding, and higher plane-wave and modal reflectivities. Because of these improvements in the design, these wafer fused VCSELs displayed significant improvements in performance over previous long wavelength VCSELs. The wafer fused VCSELs demonstrated the lowest threshold current (9 mA) and lowest threshold current density (9 kA/cm$^2$) at room temperature to date of any long wavelength VCSEL. Room temperature, CW operation was not achieved, however, due to the large

mismatch of the cavity mode and gain peak at room temperature. This is an important issue which I will address in the next subsection.

To better understand the physics and to demonstrate the feasibility of a fused VCSEL, the first fused VCSEL which I made was optically pumped. This was the first demonstration of a long wavelength VCSEL which utilized GaAs/AlAs mirrors and was a clear indication that there was reason to be optimistic that an electrically injected device would work. The optically pumped laser operated at temperatures as high as 144 °C, the highest operation temperature reported to date for any long wavelength VCSEL. The laser also had pulse widths as short as 34 psec, the shortest pulses reported for a long wavelength VCSEL at room temperature[1].

The key to the success of these devices was the underlying wafer fusion technology. An important issue which was addressed initially was the ability to inject current through the fused interface and the degradation in device performance due to the high bonding temperatures. These issues were addressed through the demonstration of fused in-plane lasers in which the current flowed through the fused interface. The device characteristics of the fused in-plane lasers were as good as in a non-fused sample made from the same material.

*Possible Limitations*

The use of GaAs mirrors in the wafer fused VCSELs has shown dramatic improvements over previous VCSEL designs. However, in achieving these improvements some possible limitations have been uncovered. In order to integrate the GaAs/AlAs mirror with the InP double heterostructure, the samples are heated to over 600 °C for 30 minutes or longer. This may lead to dopant diffusion in the

semiconductors, especially close to the fused interface. Because of the lattice mismatch between the two materials and the difference in thermal expansion coefficients, there is strain near the fused interface. This strain combined with the high temperatures of fusing may lead to enhanced dopant diffusion close to the fused interface. Away from the fused interface, the high temperatures of fusing may still cause dopant diffusion. Matt Peters has shown[2] that the Be dopant used in p-type GaAs/AlAs mirrors tends to diffuse during epitaxial growth at 600 °C. The use of C for the acceptor in the GaAs mirrors, however, should lead to reduced diffusion problems. It is not clear how the high temperatures affect the diffusion of Zn. Zinc is known to diffuse readily from a solid source into InP[3,4,5] and to diffuse within previously grown layers and from dimethylzinc during MOVPE growth of InP[6]. Further study is needed to understand the phenomenon and severity of fusion-enhanced diffusion.

The combination of GaAs and InP creates another hetero-interface across which a voltage will drop during device operation. Hiroshi Wada[7] has measured the increase in voltage due to an n-InP/n-GaAs junction to be 0.4 V, but the data on p-InP/p-GaAs and p-n junctions still needs to be determined. It is advantageous for the VCSEL operation to have as small of a voltage drop as possible to reduce the power dissipation (and hence the temperature increase) in the device. The possible band lineups between InP and GaAs will be discussed in more detail in the next section of this chapter.

Also, more work needs to be done to look at the effects of the fused interface on the long term degradation of the fused VCSEL. Cross-sectional TEM studies by S. J. Rosner (Chapter 3) have shown that the strain induced by the lattice mismatch

is taken up by edge dislocations which have Burger's vectors perpendicular to the dislocation. This is the most mechanically stable dislocation and is not expected to propagate. However, further work needs to be done to see what effect the fused interface has on the lifetimes of the VCSELs.

In order to implement the fused VCSELs in a manufacturing environment, the fusing process needs to be scaled up in size so that 2" wafers can be bonded. The largest fused sample which has been reported in the literature[8] is 3 cm$^2$ in area, while we routinely fuse samples of approximately 1 cm$^2$ area. For production efforts, however, it is important to have the capability to fuse entire wafers. This will require special care in achieving uniform pressure to ensure complete bonding across the entire wafer.

*Directions for Achieving Room Temperature, CW Operation*

The major obstacle which prevented the devices reported on in this dissertation from achieving room temperature, CW operation was the alignment of the gain peak and cavity mode (Chapter 5). Future work to achieve this is important. The spectra of the mirror should be measured before fusing, as should the PL spectra of the active region. After fusing, the reflectance and/or transmission spectra should be measured again to determine the location of the Fabry-Perot mode. Because the active layer will be lossy at the wavelength of interest, the Fabry-Perot mode should be observable. If there were no loss in the active layer, the Fabry-Perot mode would be difficult to detect because of the low reflectivity of the InP/air interface which makes the top mirror of the resonator after fusing.

After the location of the resonance is determined, the top layer of the cavity can be etched back until the desired resonance is achieved. To achieve matching of the gain peak and cavity mode when the device is operating CW at room temperature requires a knowledge of the active region temperature under these conditions. This can be found through an estimation of the power dissipated in the device and knowledge of the thermal resistance from calculations such as those discussed in Chapter 2. The cavity mode should then be aligned such that the gain peak coincides with it when the active region reaches the calculated temperature above room temperature.

Besides the matching of the gain peak and cavity mode, further improvement in these devices can be made by lowering the contact resistance and decreasing the voltage drop across the GaAs/AlAs mirror. The contact resistance should be decreased to approximately 1 $\Omega$ through the use of a graded bandgap InGaAs contact and the prevention of the contact layer undercutting, as discussed in Chapter 5. Since the work on the fused VCSELs began, large improvements in the electrical design of GaAs/AlAs mirrors have been made by groups at UCSB[9,10,11] and at Sandia National Laboratories[12,13]. Through the implementation of a more advanced GaAs mirror design and the reduction of the number of mirror periods, the voltage drop across these mirrors should decrease to less than 2 V.

Finally, to achieve the best possible performance will require improved device design from the thermal viewpoint. One major improvement will be to replace the polyimide current blocking layers with more thermally conductive proton implanted or semi-insulating regrown layers. As shown in Chapter 2, the use of a proton

implanted current blocking layer should reduce the thermal resistance (hence the active region temperature) by 35 %. Another improvement to the thermal design can be made by replacing the insulating mirror with a second GaAs/AlAs mirror. This will reduce the thermal resistance by an additional 40 % from a single fused device. This double-fused VCSEL will be discussed in the next section.

*Influence of This Work on Other Research*

The combination of the GaAs/AlAs mirror with the InGaAsP active region was made possible through the development of wafer fusion at UCSB. The possibilities afforded by this technique were utilized in the research of others at UCSB after the successful demonstration of the optically pumped VCSELs. Further improvement in the understanding and technique of fusing occurred after our group at UCSB began collaborations with Hewlett-Packard Laboratories. Rajeev Ram did important work as a summer student at HP Labs resulting in better understanding of the fused interface and improved reproducibility of fusing[8]. Less than two years after that, the Optoelectronics Division of Hewlett-Packard introduced a new AlInGaP LED structure using fused transparent GaP substrates to double the brightness of the LEDs[14].

Dubravko Babić is currently working at UCSB on an all-epitaxial VCSEL in which a GaAs/AlAs mirror is fused to an InGaAsP active layer with an InP/InGaAsP mirror on the bottom[15]. In this case, fusing allows the incorporation of the high reflectivity GaAs/AlAs mirror with the InP based structure. The all-epitaxial VCSEL should have improved current uniformity over previous long wavelength VCSELs and would allow simultaneous growth of both mirrors in

different growth chambers, reducing the fabrication time. It should also simplify the fabrication technique required to make the long wavelength VCSELs.

I-Tsing Tan is developing a high speed, resonant cavity enhanced photodetector at 1.3 µm using GaAs/AlAs mirrors[16]. Although the requirements for mirror reflectivity in resonant cavity detectors are not as stringent as they are in VCSELs, wafer fusion allows the use of the well-developed GaAs/AlAs mirror growth capability at UCSB and gives a larger optical bandwidth using GaAs/AlAs mirrors than in lattice matched InP/InGaAsP mirrors.

## 6.3 Future Directions

The successful creation of long wavelength VCSELs which utilize GaAs-based mirrors could not have occurred without the use of wafer fusion. Wafer fusion has removed constraints from the device designer in the realization of desired device properties by removing the need to use lattice matched materials. New combinations of material systems can be achieved to enhance device performance and create devices which could not have been made otherwise. This section of the chapter examines some of the possibilities created by wafer fusion. First, I will discuss possible improvements to the wafer fused VCSEL through the use of a double-fused design. Then I will suggest some experiments for better understanding of the interfaces between different semiconductors, with a particular focus on the InP and GaAs material systems. Finally, I will propose a three-color display using LEDs or VCSELs fused onto the same substrate.

*Double-fused VCSELs*

Although the single fused devices developed in this thesis operate well, an electrically and thermally insulating dielectric mirror is still required on one side of the laser. Because current cannot be injected through the dielectric mirrors, a ring contact must be employed. The carriers injected from the ring are unevenly distributed in the radial direction. This non-uniform current distribution causes higher order transverse modes to achieve threshold[17,18]. It is also more difficult to extract heat through the dielectric mirrors than it is through epitaxially grown mirrors, as discussed in Chapter 2. Although previous authors have reported extremely high thermal conductivity through such dielectric mirrors as $Si/MgO$[19], they have invariably used the values for the thermal conductivity of crystalline $Si$[20]. In actuality what is used in the mirrors is amorphous $Si$[21,22], which has a thermal conductivity more than two orders of magnitude lower than that of crystalline $Si$. The lower thermal conductivity of amorphous $Si$ limits the maximum thermal conductivity achievable in dielectric mirrors. The highest thermal conductivities are achieved through the use of epitaxially grown mirrors.

A device which employed two $GaAs/AlAs$ mirrors would have improved thermal, optical, and electrical properties compared to any previous long wavelength VCSEL. A promising extension of this thesis work is the development of *double fused* VCSELs, in which the InGaAsP active layer is surrounded by two $GaAs/AlAs$ mirrors (Fig. 6.1). These devices have several advantages. After the mirrors are fused to the active material, double fused VCSELs look very similar to their (In)GaAs counterparts. Thus, most of the results from the research on (In)GaAs VCSELs can be applied to these devices. The fabrication techniques

which have been developed for (In)GaAs VCSELs can be applied to the double fused VCSELs. This is a very important point in making these devices commercially viable. It means that the double fused VCSELs can be placed in pre-existing VCSEL manufacturing lines without devoting materials and human resources to the development of a new and separate fabrication procedure.
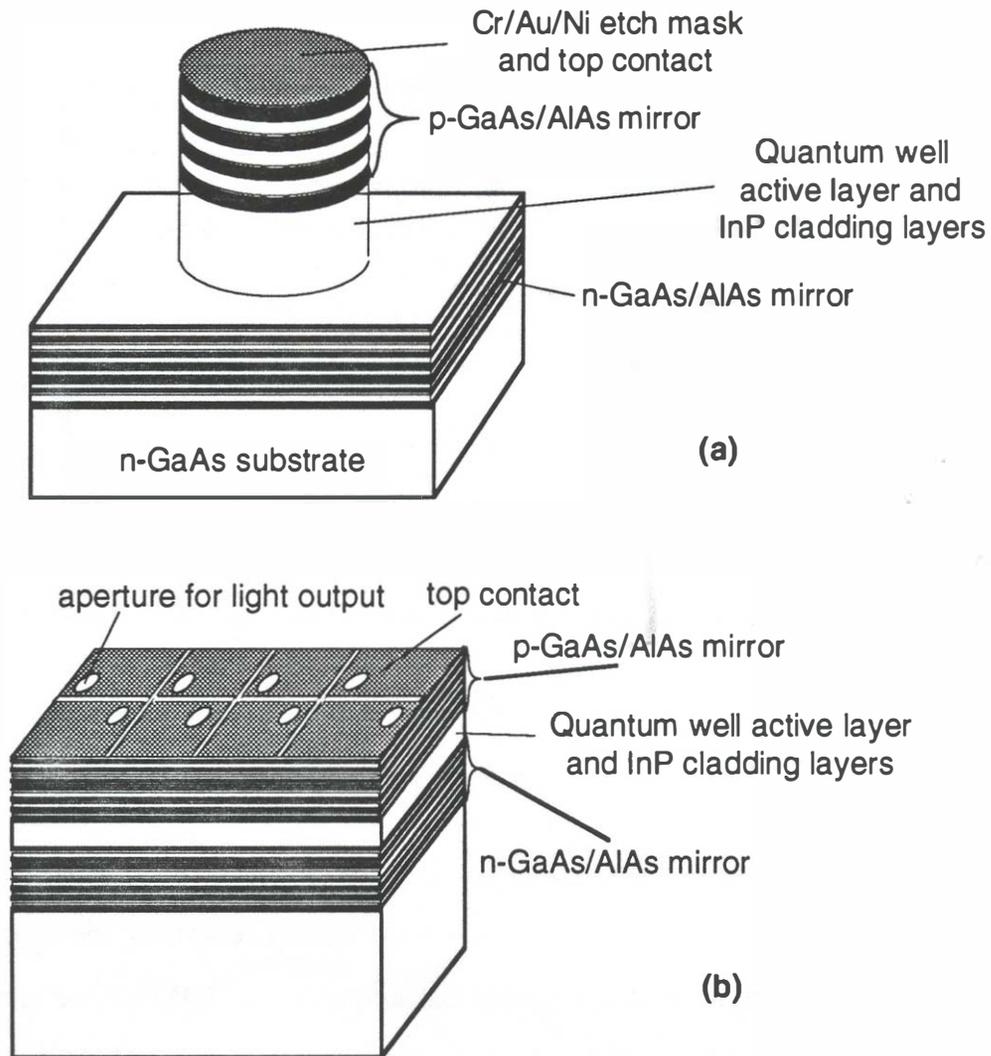


**Fig. 6.1** Schematic diagram of the proposed double fused VCSEL using (a) etched pillars and (b) proton implantation.

By employing a metal mirror as the top contact [Fig. 6.1(a)] or by including a current spreading layer in a top emitting structure [Fig. 6.1(b)], uniform current injection can be achieved. Proton implantation can be used to make a planar device as shown in Fig. 6.1(b). Mirror growth techniques which have led to threshold voltages less than 2 V in (In)GaAs VCSELs[9] can be used in these devices as well, lowering the heat dissipated and the resulting temperature rise in these devices.
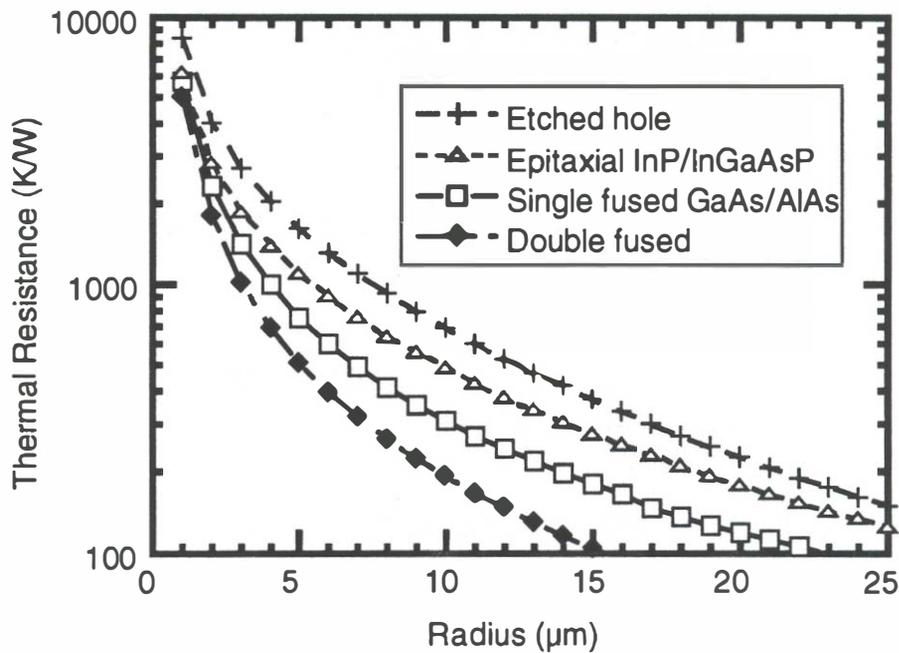


**Fig. 6.2** Thermal resistance of various long wavelength VCSEL structures.

Further improvement in the thermal characteristics should be achieved by going to a double fused structure. The results of a calculation comparing the thermal resistance of a conventional etched hole device, a conventional InP/InGaAsP mirror device, a single fused device and a double fused device are shown in Fig. 6.2. The thermal resistance of the single fused device is approximately 60 % lower than that

of the InP/InGaAsP mirror device, while the thermal resistance of the double fused device is only 40 % of the InP/InGaAsP mirror device. Thus, the double fused devices should have markedly better thermal properties than any of the previously demonstrated VCSEL designs.

The optical properties of the GaAs/AlAs mirrors are better than those of InP/InGaAsP mirrors and any of the dielectric mirrors except for $Ti_2O_3/SiO_2$. In addition to the higher plane wave reflectivity and larger optical bandwidth of GaAs/AlAs mirrors compared to InP/InGaAsP mirrors, the diffraction loss in the all-binary mirrors is lower as well[23]. While the desire for single transverse mode operation and minimum heating of the active region necessitate the use of small devices, practical devices using InP/InGaAsP mirrors cannot be made with diameters smaller than 10 $\mu$m due to the diffraction losses. Because of the decreased diffraction loss in GaAs/AlAs mirrors, however, devices with diameters on the order of 5 $\mu$m can be readily achieved. In comparing GaAs/AlAs mirrors with $Ti_2O_3/SiO_2$ mirrors, the maximum theoretical reflectivity which can be achieved with the $Ti_2O_3/SiO_2$ mirrors is greater. However, practical problems with stress in the deposited films must be addressed before the maximum reflectivity can be achieved, while the GaAs/AlAs mirror growth is a well-developed technology. Also, the benefits of being able to inject current through the epitaxially grown mirror outweighs the slight disadvantage in reflectivity.

The fabrication procedure for the double fused VCSEL begins with the fusing of the InP double heterostructure to the n-type GaAs/AlAs mirror. After the p-InP substrate is removed, the p-type GaAs/AlAs mirror is fused to the once-fused sample and the GaAs substrate is removed using an AlAs mirror layer as the etch

stop layer in a pH balanced $NH_4OH:H_2O_2$ spray etch[24,25]. Contact dots with Ni

on the top are formed by e-beam evaporation and standard lift-off techniques.

Mesas are etched through the p-GaAs/AlAs mirror with $Cl_2$ RIE using the contact

dots as a self-aligned etch mask. Finally, a bottom contact is evaporated on one

side of the n-GaAs substrate. A scanning electron micrograph of a finished double

fused device is shown in Fig. 6.3.
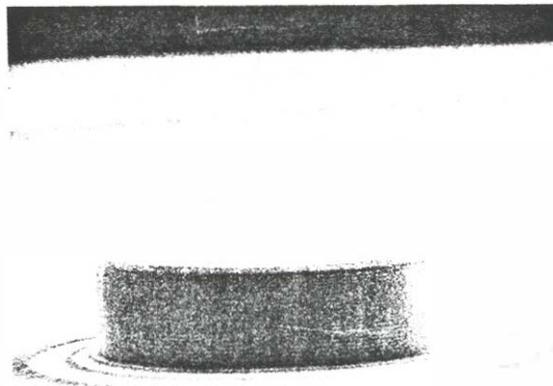


**Fig. 6.3** Scanning electron micrograph of a first-generation double fused VCSEL structure.

Because the fabrication procedure is straightforward and fast, I attempted to

make a double fused VCSEL using existing GaAs/AlAs mirrors centered near

1300 nm. Both the p-type mirror used in the optical pumping experiments

(Chapter 4) and the n-type mirror used in the single fused VCSEL (Chapter 5)

consisted of 27 periods of GaAs/AlAs pairs. Attempts were made to achieve a

more optimal design for the double fused VCSEL mirrors with a 22 period $n$-mirror

and an 18 period $p$-mirror (incorporating a phase matching layer to boost the reflectivity using the top contact), but the center wavelengths of the mirrors were far out of specification.

Two samples were fabricated, one with a 1.5 $\mu$m long cavity and a 360 nm thick InGaAsP ($\lambda_{gap}$ = 1.3 $\mu$m) active region, and one with a 0.8 $\mu$m long cavity and a 200 nm thick InGaAsP ($\lambda_{gap}$ = 1.3 $\mu$m) active region. Both samples were tested under pulsed (200 nsec, 10 kHz) and CW conditions at 15 °C. A typical CW light-current and current-voltage trace is shown in Fig. 6.4. Although there is a gradual turn-on in the L-I curve at 12 mA, the spectra remain very broad indicating that the device is not lasing. A strange kink also occurs in the L-I and I-V curves near 19 mA. This kink is reproduced when the current is decreased from above 19 mA to zero mA and is reproducible from device to device.

****** GRAPHICS PLOT ******
DF-VCSEL 221A C3L26
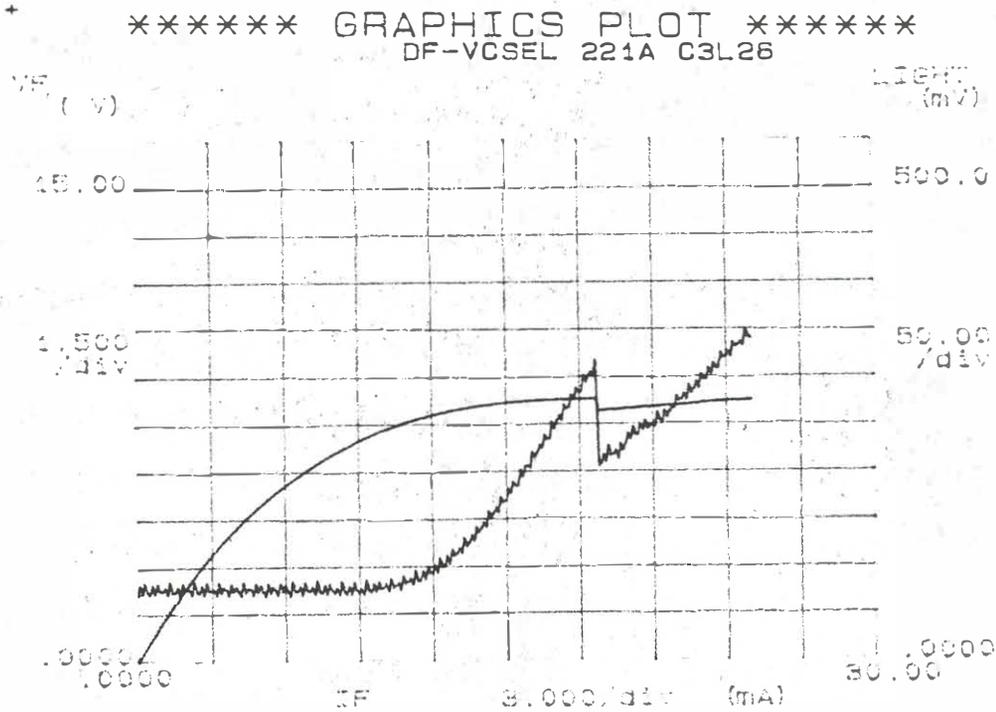
Fig. 6.4 Voltage (smooth curve) and light output (rough line) as a function of input current for the double fused VCSEL structure. Although there appears to be a threshold in the light-current characteristic, the spectra remains broad indicating that lasing does not take place.

Further research needs to be done to determine the feasibility of the double-fused VCSELs. It is promising that the first set of double fused devices display diode-like I-V characteristics and emit light. The devices are also fairly rugged, as they withstood testing at current levels as high as 350 mA and current densities as high as 32 kA/cm$^2$. Two areas in particular need to be explored further to better understand the physics in the double fused VCSEL.

The first is absorption in the p-type GaAs and AlAs. Intravalence band absorption is known to occur in highly doped p-GaAs[26]. No work has been published on absorption near 1.3 and 1.55 μm wavelengths, however, as there

have been no devices operating in this wavelength region using highly doped GaAs before the demonstration of the wafer fused VCSELs. Recent measurements by Babić[27] show that for GaAs wafers nominally doped at $N_A = 5 \times 10^{18}$ cm$^{-3}$, the absorption exceeds 100 cm$^{-1}$. More work is needed, however, to determine the absorption at values near those used in doping mirrors (typically $1 \times 10^{18}$ cm$^{-3}$). There is reason for optimism that the loss is noticeably lower there, as the dependence of intravalence band absorption on doping is non-linear and the two optically pumped wafer fused VCSELs which have been reported[1,15] both used $p$-GaAs/AlAs mirrors.
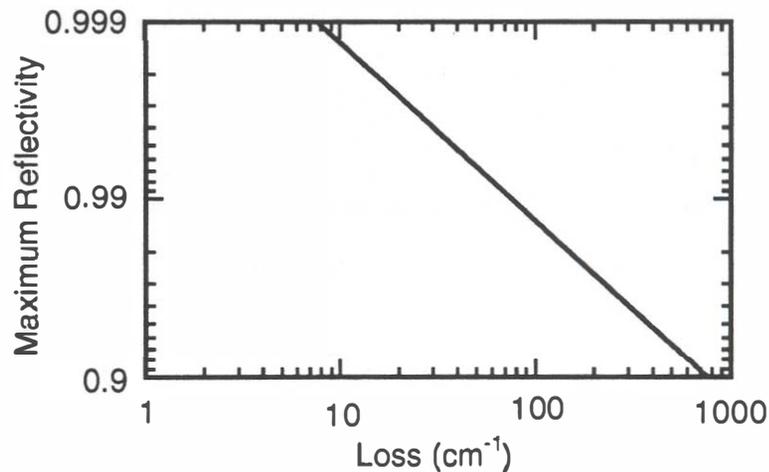


**Fig. 6.5** Maximum reflectivity achievable with GaAs/AlAs mirrors at 1.3 μm as a function of loss.

The effect of loss in $p$-doped GaAs/AlAs mirrors is shown in Fig. 6.5. This plot shows the maximum achievable reflectivity in a $p$-GaAs/AlAs mirror as a function of the absorption loss. Note that for losses greater than 700 cm$^{-1}$, the

maximum reflectivity is less than 90 %. The threshold current density in a device with a 90 % mirror and a 99.44 % mirror (achievable using a 21-period $n$-GaAs/AlAs mirror) should be less than 9 kA/cm$^2$ from the calculations shown in Fig. 5.2. The device modeled in that figure used a 4-period Si/SiO$_2$ mirror ($R = 99.44$ %) and a 15-period $n$-GaAs/AlAs mirror ($R = 89.1$ %) and had a highly lossy ($\alpha = 30$ cm$^{-1}$) 0.3 $\mu$m thick $p$-InGaAsP contact layer in the cavity. As the losses measured for $p$-GaAs have been less than 200 cm$^{-1}$ at high doping levels, the above analysis is overly pessimistic. The $p$-GaAs/AlAs mirror can also utilize a top Au layer to increase the reflectivity and reduce the drive voltage. Therefor, I think that operation of double-fused VCSELs should occur in the laboratory. However, the practical implementation of this device still requires careful design and understanding of the losses in $p$-GaAs.

The second area which needs to be explored more to fully exploit the possibility of making double-fused VCSELs is discussed in the following subsection.

*Physics at fused interfaces*

A complete description of the fused interface must include knowledge of the band offsets between the two fused materials. This affects the current transport properties in devices such as the double fused VCSEL proposed above, making it critical for the understanding of device operation. The use of wafer fusion to create abrupt, defect-free junctions between materials which could not be made by heteroepitaxy should also lead to the development of new classes of devices where the unique band lineups play critical roles in the device operation. Wafer fusion

also provides an empirical arena in which broad theories of heterojunction band lineups can be tested and refined until ultimately the physics at the semiconductor interfaces are better understood.

The remainder of this section will look at the junction between InP and GaAs. However, wafer fusion is not limited only to this set of materials. The field is rich with opportunities to explore combinations of other III-V compounds, combinations of II-VI compounds, and combinations of compound semiconductors with elemental semiconductors such as Si and Ge. In the particular case of InP joined to GaAs, previous research to combine the two material systems has focused on heteroepitaxial growth involving large buffer layers to relieve the thermal expansion and lattice mismatch induced strains. Thus, little is known about the band lineup in abrupt InP/GaAs junctions.

A first order approximation to the band offsets can be obtained by using the transition metal line-up principle[28,29]. Neglecting the effects of strain at the interface and looking at the energy positions of the 3d transition metal levels in InP and GaAs, it is predicted[30] that

$$\Delta E_c = E_c(\text{GaAs}) - E_c(\text{InP}) = 0.3 \text{ eV} \tag{6-1}$$

$$\Delta E_v = E_v(\text{GaAs}) - E_v(\text{InP}) = 0.2 \text{ eV} \tag{6-2}$$

Because of the positive signs for both offsets, this indicates a staggered band lineup or Type II heterostructure as shown in Fig. 6.6. The band diagram in Fig. 6.6 shows that the interface may allow spatially indirect transitions, an interesting area

for research on fused InP/GaAs interfaces independently proposed by R. Ram and J. Fouquet at HP Laboratories and D. Bimberg at the Technical University of Berlin.
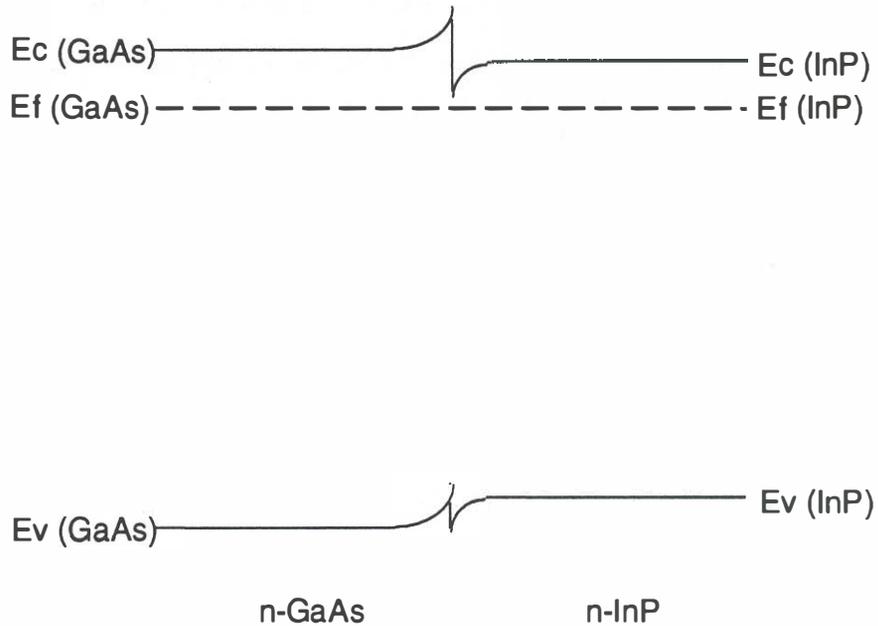


**Fig. 6.6** Proposed band diagram for the abrupt n-InP/n-GaAs interface.

Little work has been published to measure the offsets. Wada and co-workers[7] measured the I-V characteristics of wafer fused p-InP/p-GaAs and n-InP/n-GaAs junctions. The conduction band offset was fit to a simple thermionic emission model which gave an average $\Delta E_c$ of 0.41 eV. The actual value measured was found to be dependent on the fusing temperature used. Results using p-p junctions were more ambiguous, however. The p-p junctions did not fit the predicted I-V curves and the fit became worse as the fusing temperature increased. A possible reason for this is Zn diffusion at the interface between the two differently doped

materials ($2 \times 10^{19}$ for GaAs and $5 \times 10^{18}$ for InP) causing a non-abrupt interface to form.

As more work is done to measure the band lineups between different fused combinations, more opportunities will arise to use the unique properties of the fused junctions and a better understanding of the physics at heterostructure interfaces should arise. This improved understanding should lead to new and improved devices which utilize wafer fused materials.

### *Fused Color Displays*

The applications for light-weight, three-color displays are increasing. Portable computer screens, pager displays, flat panel television sets, large screen outdoor displays, and displays for automobiles and aviation are large current and potential markets for displays that do not have the bulk of CRT technology. Presently, thin film transistor LCD displays are used for the displays in many portable computers. However, these are expensive to manufacture and the manufactured yield of active-matrix LCD displays is only around 50 %[31]. While the LCD displays meet the criteria of being lightweight and flat, they cannot compete with CRTs for brightness.

With the recent improvements in visible LEDs to efficiencies meeting or exceeding those of standard incandescent light bulbs, it is now possible to integrate these into red-green-blue displays. However, the material systems used to make the LEDs (AlGaAs for red, AlInGaP for green, and GaN for blue) are not compatible with each other using standard epitaxial techniques. This is an area in

which wafer fusion can be used to integrate the various material systems to form bright, lightweight, and thin three-color displays.
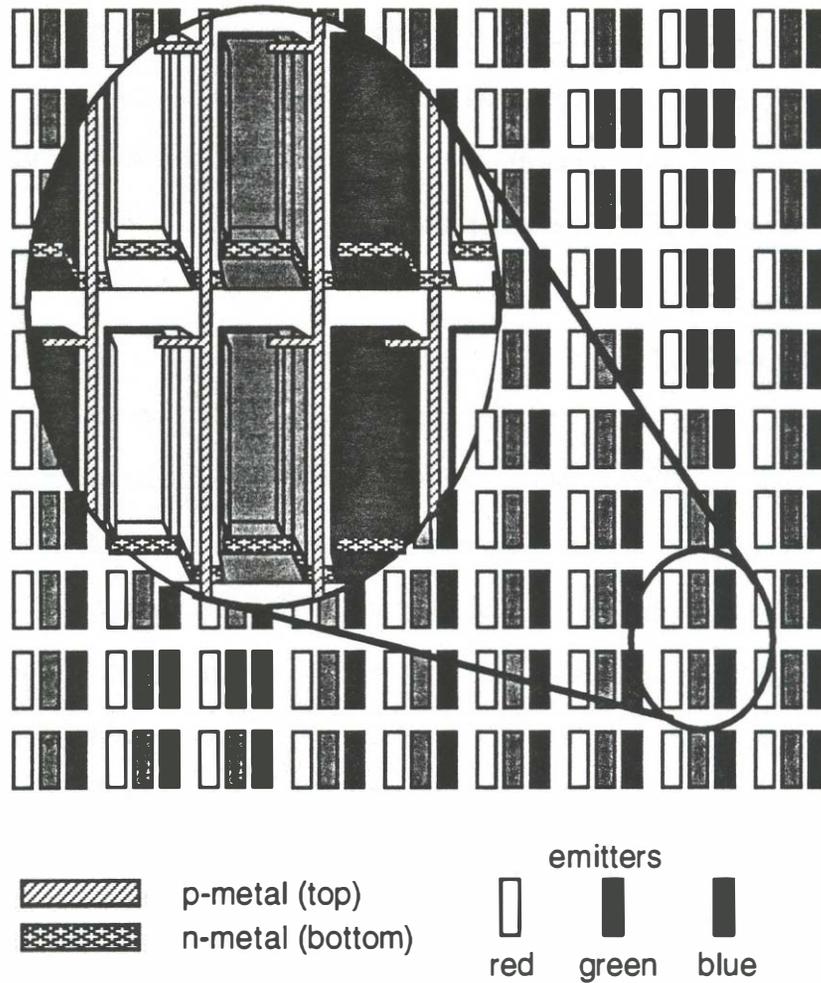


**Fig. 6.7** Schematic diagram of a three color display using fused LEDs or VCSELs.

A schematic of the proposed display is shown in Fig. 6.7. The interconnection metals which go across the rows of devices (shown in the blow up of Fig. 6.7) connect the $n$-type bottom half of the mesas. The interconnection metals for the

columns connect the *p*-type upper half of the mesas in this example of an
addressing scheme for the emitters. Note that the elements do not necessarily need
to be LEDs. They could also be lasers. However, visible LEDs are used in this
example because this technology is currently more mature than the visible laser
technology. Three individual epitaxial structures could be grown for all of the
colors. Before processing individual emitters, the 'red' wafer is fused to the
'green' wafer, followed by the etching of the 'green' wafer substrate. The 'blue'
wafer is then fused to the 'red-green' combination and the 'blue' substrate is
removed. The colors of the wafers indicate the color of the final emitter from that
material system. However, the order chosen here is arbitrary and not necessarily
the best choice for an actual design.



**(a)**                                    **(b)**
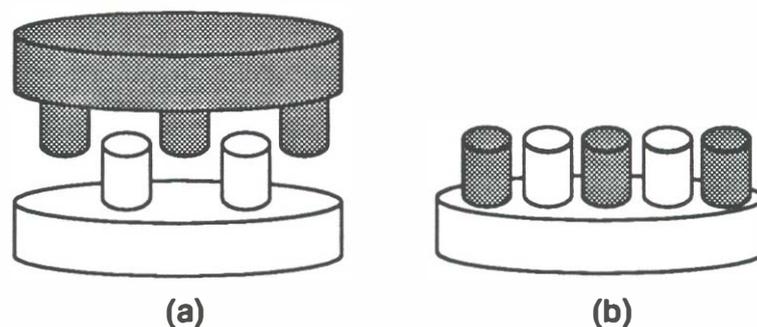
**Fig. 6.8** Method for self-alignment of different materials during fusing by
patterning the substrates prior to fusing.

A particularly advantageous method for fusing the different wafers together
which has been demonstrated at UCSB and at HP Labs is that of patterned fusing.
The idea is illustrated in Fig. 6.8. Before fusing, mesas are etched in each material
only where the desired final devices are to be located [Fig. 6.8(a)]. Alignment of
the wafers is aided by using the etched mesas as guides. After fusing, the top

substrate is removed, leaving mesas of two different materials on the bottom substrate [Fig. 6.8(b)]. The final processing step is then to deposit and define *p*- and *n*-type contacts. Finally, the three-color display would be packaged for viewing in a finished product, whether it be on a wrist watch, in an advanced calculator display, or on a full color, animated billboard.

## 6.4 Conclusions

The most visible result of this thesis has been the development of a new design for long wavelength VCSELs which takes advantage of the high reflectivity achievable in GaAs/AlAs mirrors. This design has solved some of the fundamental optical, thermal, and electrical problems in long wavelength VCSELs. The long-term impact of this work, however, will be much broader than that of the creation of a single device. Additionally, this work has demonstrated the versatility of the wafer fusion technique. This is the first work which has used wafer fusion in an application in which the fused interface plays an active role in both the electrical and optical properties of the device. Hopefully, this will lead to the invention of an entire generation of new and previously-impossible devices, while leading to a better understanding of solid state physics.

I have proposed in this chapter a direct extension to this thesis work, the development of the double fused VCSEL. It has the advantages of improved thermal, optical and electrical properties over previous long wavelength VCSELs. Much of the well-developed (In)GaAs VCSEL technology can be applied to the double fused VCSEL because of the similarities of the two structures.

Wafer fusion allows the opportunities to expand our knowledge of semiconductor physics. By creating abrupt, defect free junctions between materials that cannot be epitaxially grown, basic theories of electronic band lineups can be tested and improved. This will allow the invention of new device types while improving existing fused devices.

I also proposed in this chapter the creation of thin, bright three-color displays using fused LEDs or lasers. The high brightness available from current visible LEDs make these displays ideal for use in outdoor applications. Wafer fusion is ideal for integrating the various material systems used to make the different emitters as it does not require lattice matching of the materials.

Through the development of wafer fusion, this thesis work has solved many of the fundamental problems limiting the performance of long wavelength VCSELs. Material for several more Ph.D. dissertations remains to be found in the fields of long wavelength VCSELs and wafer fusion.

**References**

[1]   Dudley, J.J., Ishikawa, M., Babić, D.I., Miller, B.I., Mirin, R., Jiang, W.B., Bowers, J.E., and Hu, E.L., "144 °C Operation Of 1.3 μm InGaAsP Vertical Cavity Lasers On GaAs Substrates," *Applied Physics Letters*, vol. 61, no. 26, 3095-7, 28 Dec. 1992.

[2]   Peters, M.G., Thibeault, B.J., Young, D.B., Scott, J.W., Peters, F.H., Gossard, A.C., and Coldren, L.A., "Band-Gap Engineered Digital Alloy Interfaces For Lower Resistance Vertical-Cavity Surface-Emitting Lasers," *Applied Physics Letters*, vol. 63, no. 25, 3411-13, 20 Dec. 1993.

[3]   Wang, K., Parker, S.M., Cheng, C., and Long, J., "Diffusion In InP Using Evaporated $Zn_3P_2$ Film With Transient Annealing," *Journal Of Applied Physics*, vol. 63, no. 6, 2104-9, 15 March 1988.

[4]   VanGurp, G.J., Boudewijn, P.R., Kempeners, M.N.C., and Tjaden, D.L.A., "Zinc Diffusion In n-Type Indium Phosphide," *Journal Of Applied Physics*, vol. 61, no. 5, 1846-55, 1 March 1987.

[5]   Serreze, H.B. and Marek, H.S., "Zn Diffusion In InP: Effect Of Substrate Dopant Concentration," *Applied Physics Letters*, vol. 49, no. 4, 210-11, 28 July 1986.

[6]   Blaauw, C., Shepherd, F.R., and Eger, D., "Secondary Ion Mass Spectrometry And Electrical Characterization Of Zn Diffusion In n-Type InP," *Journal Of Applied Physics*, vol. 66, no. 2, 605-10, 15 July 1989.

[7]   Wada, H., Ogawa, Y., and Kamijoh, T., "Electrical Characteristics Of Directly-Bonded GaAs And InP," *Applied Physics Letters*, vol. 62, no. 7, 738-40, 15 Feb. 1993.

[8]   Ram, R.J., Yang, L., Nauka, K., Houng, Y.M., Ludowise, M., Mars, D.E., Dudley, J.J., and Wang, S.Y., "Analysis Of Wafer Fusing For 1.3 μm Vertical Cavity Surface Emitting Lasers," *Applied Physics Letters*, vol. 62, no. 20, 2474-76, 17 May 1993.

[9]   Peters, M.G., Thibeault, B.J., Young, D.B., Scott, J.W., Peters, F.H., Gossard, A.C., and Coldren, L.A., "Band-Gap Engineered Digital Alloy Interfaces for Lower Resistance Vertical-Cavity Surface-Emitting Lasers," *Applied Physics Letters*, vol. 63, no. 25, 3411-13, 20 Dec. 1993.

[10]  Peters, M.G., Young, D.B., Peters, F.H., Scott, J.W., Thibeault, B.J., and Coldren, L.A., "17.3% Peak Wall Plug Efficiency Vertical-Cavity Surface-Emitting Lasers Using Lower Barrier Mirrors," *IEEE Photonics Technology Letters*, vol. 6, no. 1, 31-3, Jan. 1994.

[11] Peters, M.G., Peters, F.H., Young, D.B., Scott, J.W., Thibeault, B.J., and Coldren, L.A., "High Wallplug Efficiency Vertical-Cavity Surface-Emitting Lasers Using Lower Barrier DBR Mirrors," *Electronics Letters*, vol. 29, no. 2, 170-2, 21 Jan. 1993.

[12] Lear, K.L., Chalmers, S.A., and Killeen, K.P., "Low Threshold Voltage Vertical Cavity Surface-Emitting Laser," *Electronics Letters*, vol. 29, no. 7, 584-6, 1 April 1993.

[13] Chalmers, S.A., Lear, K.L., and Killeen, K.P., "Low Resistance Wavelength-Reproducible p-Type (Al, Ga)As Distributed Bragg Reflectors Grown By Molecular Beam Epitaxy," *Applied Physics Letters*, vol. 62, no. 14, 1585-87, 5 April 1993.

[14] Kish, F.A., Steranka, F.M., Defevere, D.C., Vanderwater, D.A., Park, K.G., Kuo, C.P., Osentowski, T.D., Peanasky, M.J., Yu, J.G., Fletcher, R.M., Steigerwald, D.A., Craford, M.G., and Robbins, V.M., "Very High-Efficiency Semiconductor Wafer-Bonded Transparent-Substrate $(Al_xGa_{1-x})_{0.5}In_{0.5}P/GaP$ Light-Emitting Diodes," *Applied Physics Letters*, vol. 64, no. 21, 2839-2841, 23 May 1994.

[15] Babić, D.I., Dudley, J.J., Streubel, K., Mirin, R.P., Hu, E.L., and Bowers, J.E., "Optically Pumped All-Epitaxial Wafer-Fused 1.52 μm Vertical-Cavity Lasers," *Electronics Letters*, vol. 30, no. 9, 704-706, Apr 28 1994.

[16] T., I.T., Dudley, J.J., Babić, D.I., Cohen, D.A., Young, B.D., Hu, E.L., Bowers, J.E., Miller, B.I., and Young, M.G., "High Quantum Efficiency and Narrow Absorption Bandwidth of the Wafer-Fused Resonant InGaAs Photodetectors," *IEEE Photonics Technology Letters*, .

[17] Wada, H., Babić, D.I., Ishikawa, M., and Bowers, J.E., "Effects Of Nonuniform Current Injection In GaInAsP/InP Vertical-Cavity Lasers," *Applied Physics Letters*, vol. 60, no. 24, 2974-2976, Jun 15 1992.

[18] Dudley, J.J., Babić, D.I., Mirin, R., Yang, L., Miller, B.I., Ram, R.J., Reynolds, T., Hu, E.L., and Bowers, J.E., "Low Threshold, Wafer Fused Long Wavelength Vertical Cavity Lasers," *Applied Physics Letters*, vol. 64, no. 12, 1463-5, 21 March 1994.

[19] Baba, T., Yogo, Y., Suzuki, K., Iga, K., and Koyama, F., "GaInAsP/InP Low-Mesa CPBH Surface Emitting Laser With An Optimally Deposited MgO/Si Multilayer Laser Mirror," *Japanese Journal Of Applied Physics, Part 1 (Regular Papers & Short Notes)*, vol. 32, no. 6A, 2692-4, June 1993.

[20] Maycock, P.D., "Thermal Conductivity of Silicon, Germanium, III-V Compounds and III-V Alloys," *Solid-State Electronics*, vol. 10, 161-168, 1967.

[21] Cahill, D.G., Watson, S.K., and Pohl, R.O., "Lower Limit to the Thermal Conductivity of Disordered Crystals," *Physical Review B*, vol. 46, no. 10, 6131-6140, 1992.

[22] Goldsmid, H.J., Kaila, M.M., and Paul, G.L., "Thermal Conductivity of Amorphous Silicon," *phys. stat. sol. (a)*, vol. 76, K31-K33, 1983.

[23] Babić, D.I., Chung, Y., Dagli, N., and Bowers, J.E., "Modal Reflection of Quarter-Wave Mirrors in Vertical Cavity Lasers," *IEEE Journal of Quantum Electronics*, vol. 29, no. 6, 1950-62, June 1993.

[24] LePorc, J.J., "An Improved Technique for Selective Etching of GaAs and GaAlAs," *Journal of Applied Physics*, vol. 51, 6441-42, Dec. 1980.

[25] Babić, D.I., "Spray Etching System for Selective GaAs Substrate Removal," Sept. 1993, unpublished.

[26] Pankove, J.I., *Optical Processes in Semiconductors.* Dover, 1971.

[27] Babić, D., "Absortption in p-type GaAs and InP at Long Wavelengths," unpublished.

[28] Langer, J.M. and Heinrich, H., "Deep-Level Impurities: A Possible Guide to Prediction of Band-Edge Discontinuities in Semiconductor Heterojunctions," *Physical Review Letters*, vol. 55, no. 13, 1414-17, 23 Sept 1985.

[29] Langer, J.M., Delerue, C., Lannoo, M., and Heinrich, H., "Transition-Metal Impurities in Semiconductors and Heterojunction Band Lineups," *Physical Review B*, vol. 38, no. 11, 7723-39, 15 Oct 1988.

[30] Nolte, D.D., "Band Offsets For Pseudomorphic InP/GaAs," *Applied Physics Letters*, vol. 54, no. 3, 259-61, 16 Jan. 1989.

[31] Warner, K.I., "The Flat Panel's Future," *IEEE Spectrum*, 18-26, Nov 1993.