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UNIVERSITY OF CALIFORNIA
Santa Barbara

Fused Long-Wavelength Vertical-Cavity Lasers

A dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Materials Science

by

K. Alexis Black

Committee in charge:

Professor Evelyn L. Hu, Chairperson

Professor John E. Bowers, co-Chairperson

Professor Larry A. Coldren

Professor David Clarke

March 2000

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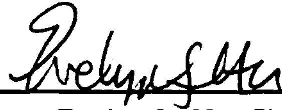

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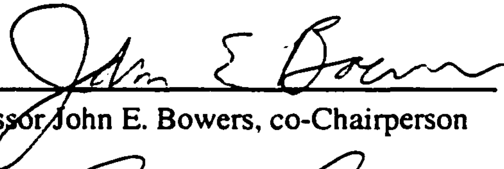

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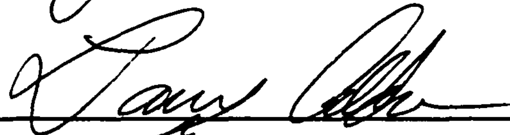

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This dissertation is dedicated to
the inventor of *i*,
my father

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Abstract

The need for low cost, high speed telecommunication and datacom sources demands the maturation of long wavelength vertical cavity lasers (VCLs). Long wavelength emission is desirable, as it is compatible with existing single mode fiber dispersion and loss minima. In order for long wavelength VCSELs to establish a cost advantage over uncooled distributed feedback lasers (DFBs), VCSELs must operate reliably over a wide temperature range. The difficulty in achieving suitable thermal behavior in long wavelength systems is manifested in low characteristic temperatures, and attributed to the high Auger recombination and intra-valence band absorption characteristic of low energy gap materials. A second major obstacle is the problem of finding a lattice matched mirror system capable of achieving the high reflectivities necessary for VCSEL design. This places stringent requirements on the design and optimization of the VCL structure. Wafer fusion has been used to combine the InP-based active region with high reflectivity GaAs-based mirrors, circumventing the problem of lattice matching. With this technology, the tradition of high performance LW-VCLs at UCSB was founded. At some point, however, the technology that enabled these devices also became their greatest limitation: the fused junction. This thesis is an in depth examination of an interface: its formation, its properties, and ultimately its role in the creation of state of the art VCSEL technology. The chemistry and microstructure of the fused interface are examined in order to determine the mechanism of fusion and optimize the structure of the interface. The electrical and optical impact of the fusion process and resultant interface on device performance is explored. In addition, two major additions to the device design were made capitalizing on the 3D design freedom afforded by the fusion process. The first attempts to incorporate a defect blocking superlattice at the fused interface to improve the gain of the active material. The second is the development and incorporation of selective area fusion for both current and carrier confinement into the device design. A deeper understanding of the nature of the fused interface allows the device designer to at once embrace the technology and work within its limitations. In conclusion, the state of the art device performance is presented, including record low threshold (0.8mA), high temperature (74°C), and small signal modulation bandwidth (7GHz) for LW-VCLs.

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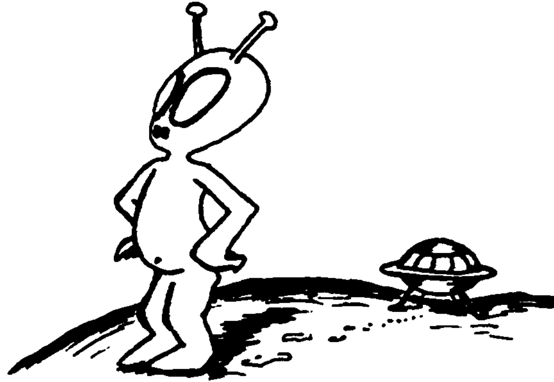

Chapter 1

Introduction to Long Wavelength Vertical Cavity Lasers

The emergence of a high speed, low threshold, long wavelength vertical cavity surface emitting laser (LW-VCSEL) source is much anticipated. VCSELs operating at 1.3 and 1.55 μm wavelength have long been heralded as the ultimate low cost solution for optical sources for gigabit ethernet links and fiber to the home (FTTH). Long wavelength emission is desirable, as it is compatible with existing single mode fiber dispersion and loss minima. Some inherent advantages of a vertical-cavity rather than an in-plane laser are efficient fiber coupling, on-wafer testing, and the potential for high bandwidth, directly-modulated devices with minimal power consumption. Despite the widespread acceptance of GaAs based (850 nm) VCSELs by industry, the development of their long wavelength counterparts has been hampered by the temperature performance of long wavelength material systems. In order for long wavelength VCSELs to establish a cost advantage over uncooled distributed feedback lasers (DFBs), VCSELs must operate reliably over a wide

temperature range. Commercial standards require operating ranges from -40°C to 85°C for telecom, and between 0°C and 70°C for datacom applications. The difficulty in achieving suitable thermal behavior in long wavelength systems is manifested in low characteristic temperatures, and attributed to the high Auger recombination and intra-valence band absorption characteristic of low energy gap materials. A second major obstacle is the problem of finding a mirror system, lattice matched to the active region, capable of achieving the high reflectivities necessary for VCSEL operation. In addition to the temperature performance specifications, additional hurdles such as competitive packaging costs for high speed (>2.5Gb/s) operation, relatively high output powers (~0 dBm at 80°C), and reliability are important.

This thesis employs wafer fusion (direct wafer bonding) to overcome the lattice matching constraints of traditional material growth techniques to combine InP-based active regions with high reflectivity GaAs-based mirrors. The resulting VCSELs define the state of the art in the field. However, the wafer fusion process and the effects of the fused junction on device performance are at once subtle and complex. This thesis provides an in depth analysis of the fused interface, explores the interaction between the interface and the resultant device, and attempts to capitalize on the freedom afforded by the fusion process to innovate new device architectures.

In this chapter, we will first review the possible material systems that can be used for both long wavelength laser active regions and mirror systems. The second section will focus on design issues relevant to attaining a thermally stable long wavelength VCSEL source, and the third section will discuss the recent technological advances that define the state of the art in the field. To conclude the chapter, an overview of the history of long wavelength VCSEL research at UCSB will be given. Finally, the major contributions of this work will be outlined in the scope of this thesis.

1.01 Long Wavelength Materials Systems

1.01.1 Mirror Systems

Critical to achieve lasing is the condition that gain overcomes loss. For a vertical cavity structure, the overlap of the optical mode and the gain region is quite small, $\Gamma \sim 0.03$. Thus, in order for the lasing condition to be met, the loss in the structure must be absolutely minimized. This translates to very high reflectivity mirrors (R ~ 99 % and greater) coupled with short optical cavities. Many different mirror systems have been proposed and demonstrated for long-wavelength VCLs. The optical, thermal, and electrical properties of each system must be addressed. They can be classified into three main categories: epitaxially-grown (either lattice matched or pseudomorphic), dielectric-deposited, and wafer-fused. Epitaxially-grown mirrors have the obvious advantage that they are directly integrated with the device much like standard GaAs based VCLs. This allows for easy manufacturability and device

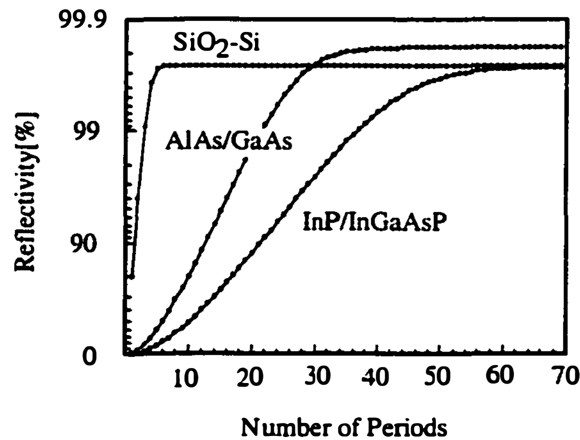

Figure 1.01 Plot of maximum mirror reflectivity versus number of periods for three different materials systems.

processing. The majority of the work on long wavelength epitaxial mirrors has been done in the InGaAsP/InP system. Unfortunately, the relatively small index contrast between InP and InGaAsP ($\Delta n \cong 0.31$) necessitates growth of a large number of mirror periods before reaching acceptable reflectivities. Figure 1.01 shows a typical plot of reflectivity (at 1.55 µm) of three different mirror systems versus the number of periods in the mirror. Table 1.1 compares important materials properties for typical long wavelength materials systems. Quoted values are representative of the materials systems and corresponding penetration depths of the optical mode for standard mirror designs. The need for long growths with good control over growth rates is even more pronounced when operating at 1.3 μm where the composition choice for the InGaAsP layer is even further constrained. The small index difference also results in large penetration depth of the optical field into the mirrors, increasing diffractive and absorptive losses. Furthermore, the thermal conductivity of InGaAsP material is very low due to alloy scattering of phonons from quaternary material. This results in a thick mirror (>10 μm) with a very low thermal conductivity. Heating in such a device is very pronounced and limits the maximum operating temperature.

There have recently been some promising results in antimonide-based mirrors lattice matched to InP[1]. The index contrast in Sb based mirrors is quite high, ($\Delta n \sim 0.48$). Unfortunately, this system suffers from poor thermal conductivity characteristic of ternary and quaternary materials. An optically pumped room temperature continuous wave operation of a 1.48 µm VCL was reported using one fused GaAs/AlGaAs mirror and one AlGaAsSb/AlAsSb mirror with an index contrast of 0.54[2]. All epitaxial, pulsed electrically pumped VCSELs using antimonide based mirrors have only recently been reported [3]. Despite the initial results using this system, considerable effort

must still be put forth in the areas of growth, dislocation control, and development of effective dopant grading schemes for low resistance mirrors.

Table.1.1 Comparison of material constants of long wavelength mirror systems.

Material ***Wavelength***	*GaAs/AlGaAs* 1.46eV **850 nm**	*InP/InGaAsP* 0.95 eV **1300 nm**	*InP/InGaAsP* 0.8 eV **1550 nm**
QW Auger recombination (cm^6/s)	3×10^{-30}	3×10^{-29}	1×10^{-28}
Free carrier absorption (p-type)	7 cm^{-1}	30 cm^{-1}	**60 cm^{-1}**
QW ΔE_c	0.3 eV	**0.16 eV**	0.23 eV
DBR thermal conductivity	0.6 W/cmK	**0.1 W/cmK**	**0.1 W/cmK**
DBR Δn	0.57	**0.25**	0.31
DBR ΔE_v	0.4 eV	0.2 eV	0.3 eV

The second type of mirror system developed for long-wavelength VCLs is the dielectric-deposited mirror. This mirror system typically consists of an oxide layer as one material and a semiconductor as the other, such as Si/SiO_2. Dielectric mirrors can have a very high index difference; less than eight periods are usually required to reach peak reflectivity. The small penetration depth reduces diffractive losses allowing for smaller devices to be fabricated. However, the poor thermal conductivity of amorphous oxide layers such as SiO_2 can result in excessive self-heating under continuous-wave operation. The loss associated with this mirror system is also great. Also, there is great difficulty in integrating such mirrors as the bottom mirror in a device.

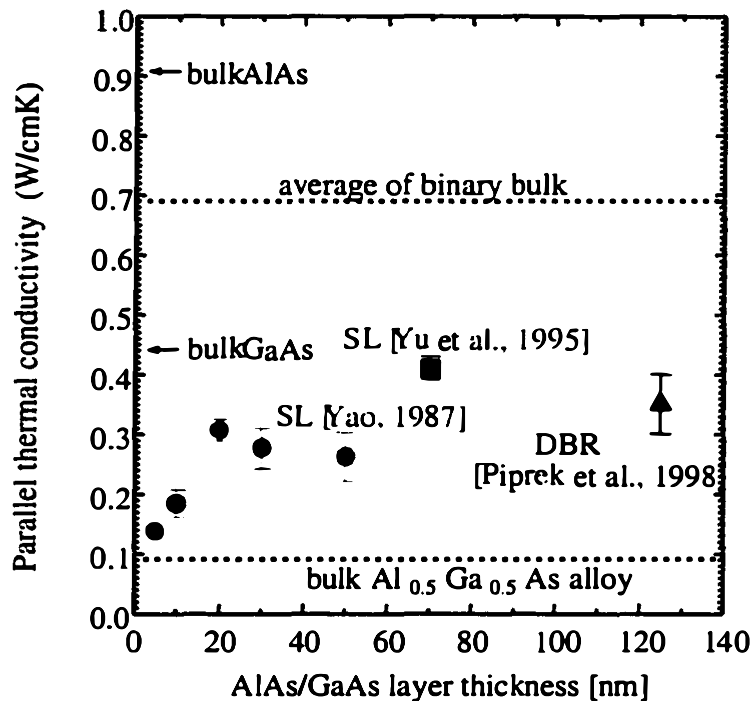

Figure 1.02 Thermal conductivity measurements from literature comparing bulk properties to that of superlattices (SL) and quarter wave DBRs. Figure by J. Piprek[4].

The final mirror system to produce working lasers is the AlAs/GaAs mirror. This material system has typically been fused to InP based active regions; however, recent work has demonstrated its use both as an epitaxially grown mirror on the lattice matched GaInNAs system[5, 6], and as a metamorphic mirror grown on InP[7]. Wafer fusion allows for the use of non-lattice matched materials such as InP and GaAs to be combined into a single device. Epitaxial wafers of each material are grown separately and combined under high temperature and pressure. The resultant interface is electrically conductive and optically transparent. GaAs/AlAs mirrors provide a high index contrast as well as the uniformity and reproducibility concomitant with epitaxial growth. Unfortunately, intra-valence band absorption in p-doped

GaAs becomes more pronounced at longer wavelengths, limiting the maximum reflectivity of the mirrors. This absorption is significantly worse at 1.55 μm than at 1.3 μm, but still allows for very high maximum reflectivities.

Despite the touted better thermal conductivity of binary systems due to an ordered lattice, Figure 1.02 contains results obtained from the literature demonstrating that the rewards of using a binary system is dependent on the thickness of the individual layers being used. In the best case scenario, the parallel bulk thermal conductivity of AlAs and GaAs are 0.9 and 0.45 W/cmK, respectively. A naive guess for the thermal conductivity of a layered structure containing 50 % AlAs and 50 % GaAs would be the average of the binary bulk data. For the case of a quarter wave stack in a GaAs/AlAs DBR, the layer thicknesses are on the order of 110 and 130 nm, respectively. This is also on the order of the mean free path of a phonon at room temperature in these systems. Consequently, the phonons can scatter off the interfaces of the quarter wave layers, contributing to a reduced thermal conductivity. The measured values for thermal conductivity of an AlAs/GaAs DBR at 1.55μm is 0.35 W/cmK[8]. This is a factor of four higher than the value for $Al_{0.5}Ga_{0.5}As$ due to the ordering in the individual layers as opposed to the disorder in the ternary compound ($Al_{0.5}Ga_{0.5}As$ is the worst case scenario for ordering). At increased temperatures, however, when the mean free path of the phonon is reduced, the effects of interface scattering may be minimized, and the benefits of an ordered binary system will prevail.

1.01.2 Active region material and design

Due to high Auger coefficients and smaller conduction band discontinuities, high temperature InP-based active regions have proven more difficult to achieve than those based on GaAs. Fortunately, much groundwork

has been laid for high temperature designs through progress in InP based edge emitters. These lasers employ strained quantum wells to reduce the effects of Auger recombination. Strain limits the number of QWs that can be grown without inducing an unacceptably high density of misfit dislocations. In order to incorporate many wells for the high gain requirements of VCLs, strain compensation techniques have been developed to reduce the net strain in the active region. Thus far, the best reported high temperature results employ strain compensated InGaAsP/InGaAsP active regions[9].

Table 1.2 Reported results on LW-VCL systems. Results for InGaAsP/InP and AlInGaAs/InP systems are given for CW RT results only.

Active region	Mirror system	Λ (μm)	Performance	Group
InGaAsP:InP	Double fused Al(Ga)As/GaAs	1.55	**74 °C,** 1 mW at 15°C, I_{th}= 0.8mA, V_{th} = 2.1V oxide aperture	UCSB
	Metamorphic Al(Ga)As/GaAs InGaAsP/InP	1.55	**45 °C,** J_{th}= 3kA/cm^2, V_{th} = <3V H+ implantation, cavity tuned	Alcatel
	Si/Al2O3 Si/SiO2	1.3	**36°C,** To = 50 K, I_{th}= 2.4mA Buried heterostructure	Furukawa
	SiO2/TiO2+ InGaAsP/InP Fused AlGaAs/AlAs+ InGaAsP/InP	1.55	**27 °C,** 7 μW at RT, J_{th}= 1.8kA/cm^2, V_{th} = 2.1V cavity tuned	NTT
AlGaInAs:InP	Fused Al(Ga)As/GaAs ZnSe/MgF	1.3	**40 °C,** 0.5 mW at RT, I_{th}= 0.8mA, V_{th} = 2.1V O implantation	Cornell
GaInNAs:GaAs	AlGaAs/GaAs SiO2/TiO2	1.25	RT cw photo-pumped Electrically pulsed at shorter wavelengths	Hitachi
InGaAs quantum dots	MgF/ZnSe AlGaAs/GaAs	1.15	J_{th} = 640 A/cm^2	UT Austin

In order to provide stronger electron confinement and prevent carrier overflow out of the MQW region at elevated temperatures, other material systems have been investigated. A considerable amount of work has been done in the AlGaInAs system lattice matched to InP. Theoretically, this system compares

favorably to the more traditional InGaAsP system, predicting slightly higher material gain and maximum critical temperatures. The conduction band offset is considerably higher in the (Al)GaInAs/Al(Ga)InAs ($\Delta E_c = 0.72\,\Delta E_g$) compared with the InGaAs(P)/InGaAsP system ($\Delta E_c = 0.4\,\Delta E_g$), leading to increased hole transport in the active layer and enhanced differential gain in edge-emitting lasers[10]. AlGaInAs active regions have been used to demonstrate cw lasing in a double fused oxide implanted VCL design operating up to 40°C[11].

Another attractive material system for active region design is GaInNAs lattice matched to GaAs. The extremely large bandgap bowing of the GaAsN system makes it possible to decrease the bandgap energy of the As rich ternary from 1.42 eV to 0 eV (semi-metal) simply by increasing the N content. However, there is a miscibility gap in this system that limits the amount of N that can be incorporated. In addition, it has been reported that the valence band lineup in the GaAs-GaInNAs is considered to be a staggered (type II) line-up[12]. By increasing the indium content and minimizing the nitrogen content, demonstration of type-I hetero-structures with emission wavelengths as long as 1.3 μm have been successful. More research into the growth of this material system is necessary to demonstrate efficient emission at longer wavelengths. Continuous-wave room-temperature photo-pumped laser oscillation has been demonstrated in vertical cavity laser designs employing single or multiple GaInNAs quantum wells, with lasing wavelengths as long as 1.256 μm[5, 6]. Electrically-injected devices have achieved pulsed operation at room temperature.

Work has also been done on InGaAs quantum dots[13], and in InGaP/InAsP systems to produce long wavelength active regions. Another interesting approach has been the development of InGaAs ternary substrates to

produce extremely high temperature operating in-plane lasers[14], although no VCLs have been demonstrated to date.

1.02 Device Design

In addition to the choices of materials for both active region and mirrors, there are numerous other design issues for the optimized performance of a long wavelength VCSEL. Only recently have many different research groups achieved room temperature continuous wave operation. Table 1 summarizes some of the recent technological advances in the field, ranging from all epitaxial structures to single and double fused structures, to quantum dot VCSELs. To date, the highest temperature VCSELs have been made using the process described in this thesis.

Aside from the choice of material system for both active region and mirror system, perhaps the most important attributes of the device design are the method of current constriction, the ability to tune the cavity, and the ability to scale devices down to small dimensions. Two particularly interesting and promising designs are those recently developed by Alcatel and CNET, a metamorphic device and a selective area fused VCL, respectively[15-17].

Alcatel's design is shown in Figure 1.03, and is comprised of an all epitaxial structure involving the metamorphic growth of an AlGaAs/GaAs

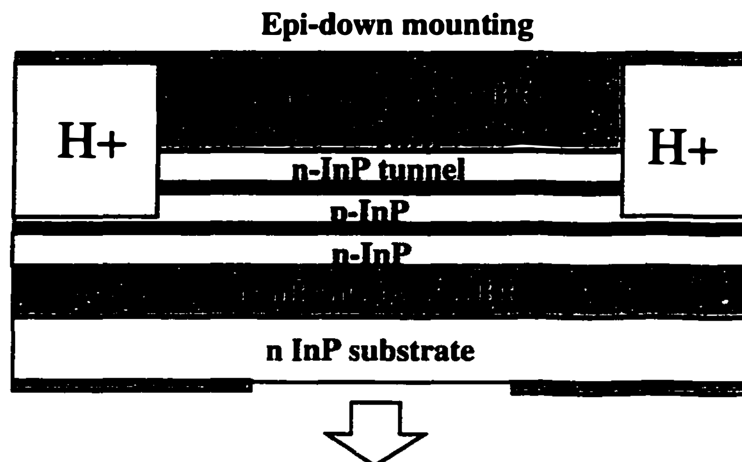

Figure 1.03 Schematic of Alcatel metamorphic Esaki junction design.

mirror on top of an InP/InGaAsP active region that has been grown on an InP/InGaAsP DBR. This structure uses H+ ion implantation for current restriction, which limits the smallest possible device diameter and lends itself to a gain guided device. Both top and bottom mirrors are n-type, minimizing the absorption loss concomitant with p-type dopants in GaAs. The diode is achieved with an Esaki junction in the upper cladding of the active region. A small (~0.3V) drop is associated with this tunnel junction. The biggest drawback of this particular device design is the metamorphic mirror. It is believed that lattice mismatched epilayers such as this top DBR are strain relaxed via plastic deformation, i.e. through the introduction of dislocations to the material at the growth surface[18]. Such dislocations are termed threading dislocations as they are inclined (usually 60°) to the strained interface and are mobile in the materials. It is interesting to note that the Matthews Blakesley limit for strained growth of GaAs on InP is less than three unit cells. This mirror reportedly has a dislocation density on the order of $10^6/cm^2$, much higher than the tolerance level for actual devices. However, Alcatel reports that the TEMs indicate the dislocations are entirely contained in the GaAs side

of the device, posing no threat to the active layers[7]. Dislocation motion, however, can only be monitored through reliability testing, which has yet to be done. The device is able to lase at RT and up to 45°C when epi-down mounted to a copper heat sink, demonstrating the second best high temperature

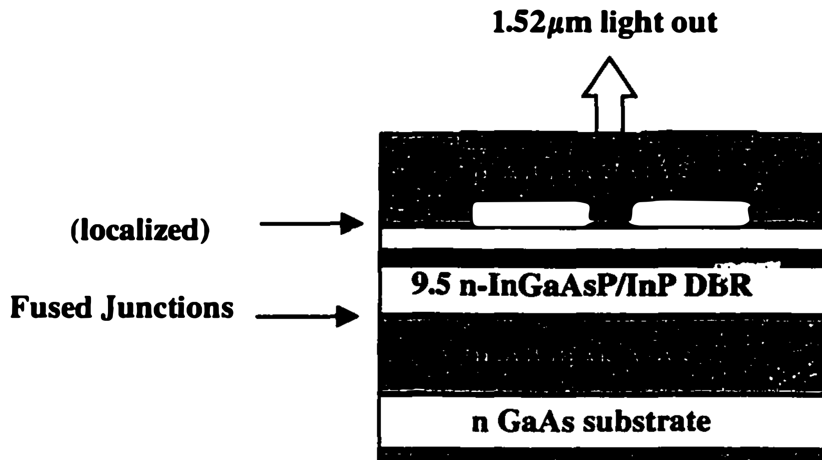

Figure 1.04 Schematic of the CNET double fused device utilizing localized wafer fusion as a current restriction technique.

performance of any electrically pumped LW-VCL.

The recent results from CNET are also quite interesting. The CNET device is a double fused structure, with the first 9.5 periods of the bottom mirror integrated with the active region via lattice matched epitaxial growth. The reason for these InP/InGaAsP mirror periods is for wavelength tuning of the cavity mode, which turns out to be a very important parameter to be able to control. They use a technique called localized fusion to constrict current. A schematic of their device is shown in Figure 1.04. They etch square pits into the GaAs mirror before fusion, thereby restricting the current to the fused areas. This etched area may also provide some index guiding to their device if

the etched aperture is smaller than the optical mode. With this structure, they have achieved 30°C CW operation[17].

All lasers that have achieved room temperature CW lasing have been demonstrated through the integration of GaAs based mirrors and InP/InGaAsP or AlInGaAs/InP active regions; all except for Alcatel's metamorphic structure have integrated these materials via wafer fusion. In the next section, we will describe a particular VCSEL design that we have employed to achieve state of the art high-temperature performance, and relate the observed device characteristics to important design choices.

1.03 This thesis: state of the art performance

The highest performance long wavelength VCSEL has consistently been achieved through wafer fusing[19]. Using the best performing electrically pumped device as an example, we will highlight the state of the art performance as well as focus on the areas that need to be further addressed to commercialize LW-VCLs.

The device structure we employ consists of two Al(Ga)As/GaAs mirrors grown on GaAs substrates by molecular beam epitaxy (MBE) fused to an InGaAsP/InP active region grown on an InP substrate by metal organic chemical vapor deposition (MOCVD). A schematic of the device is shown in Figure 1.05. The top p-mirror consists of 25.5 quarter wave periods with a single 40nm $Al_{.98}Ga_{.02}As$ layer for selective lateral oxidation placed 145 nm from the GaAs/InP fused junction. The interfaces are parabolically graded with a pulsed doping of $3x10^{18}/cm^3$. Prior to fusion, a 30nm GaAs layer was re-grown with a Be doping of $8x10^{18}/cm^3$. The bottom mirror is an undoped 30 period GaAs/AlAs quarter wave stack.

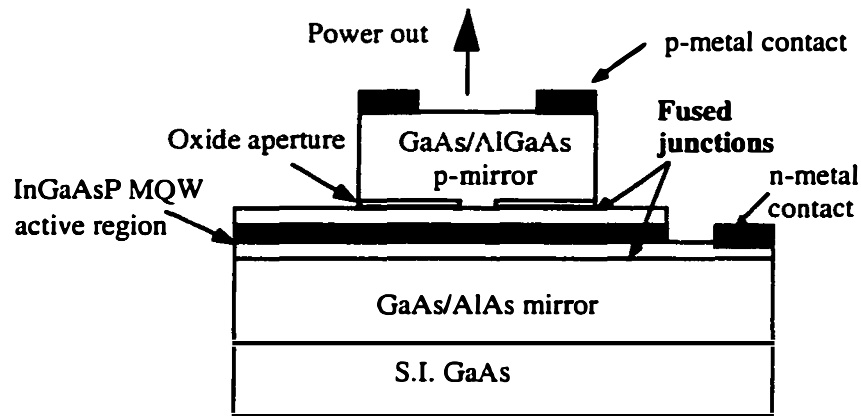

Figure 1.05 Schematic of a double fused VCSEL using an InGaAsP/InGaAsP MQW active region and two wafer fused GaAs/Al(Ga)As DBRs.

The active region incorporates two $In_{0.9}Ga_{0.1}P$ barrier layers on either side of the multiple quantum well region. The MQW region consists of six 7 nm 1%-strained quantum wells (QWs) with seven 7 nm thick barriers. The emission wavelength of the barriers is 1180 nm. On either side of the active region is a 300 nm InP cladding to form a $3/2\lambda$ cavity. The InGaP barriers serve both to compensate the compressive strain in the QWs and increase the confinement energy of the electrons in the active region by 30 meV relative to InP.

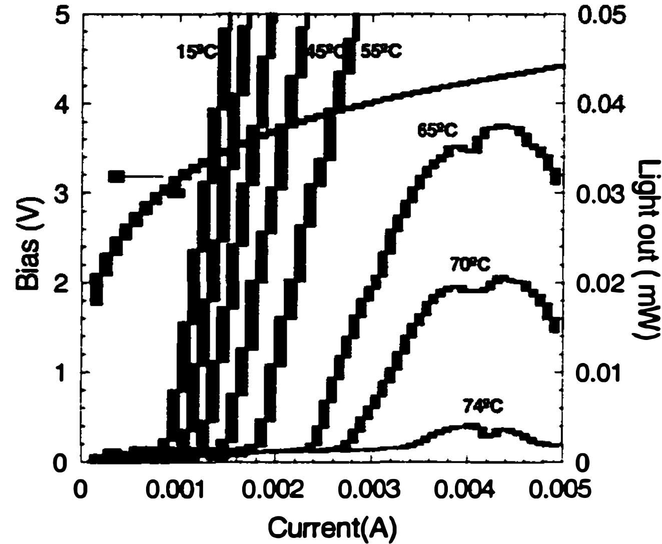

Figure 1.06 High temperature LIV curves from state of the art UCSB double fused LW-VCSEL.

The room temperature (RT) photoluminescence peak of the active region is at 1542 nm and the lasing mode is at 1515 nm. Figure 1.06 shows the high temperature L-I curves of a device with a 7 μm oxide opening. This is the first demonstration of a device operating CW up to 74°C. The threshold current at RT is 1 mA, and the threshold voltage is 3 V. The high temperature performance of this device cannot be attributed to the misalignment of the gain peak and optical mode at RT, as the gain-offset increases with temperature. The gain peak and mode wavelength shifts with temperature are 0.54 and 0.11 nm/K respectively[20]. The zero gain offset is calculated to be at -38°C and the optimum temperature for low threshold operation is expected at –108°C when the mode wavelength is 30 nm longer than the gain peak wavelength.

To further analyze the temperature sensitivity of the double fused VCSELs, the temperature sensitivity of the threshold current was measured from –190°C to 70°C, as shown in Figure 1.07. This analysis is performed on a

VCSEL from a previous run that demonstrated CW operation up to 71°C with threshold voltages of 2.1 V[21]. A record characteristic temperature of 132K is measured in the temperature range from -75°C to 35°C. This exceeds the best reported value of 95K for InGaAlAs/InP 1.55 μm Fabry-Perot lasers[22] and the more typical values reported for InGaAsP 1.55 μm lasers that fall in the 60 to 70 K range.

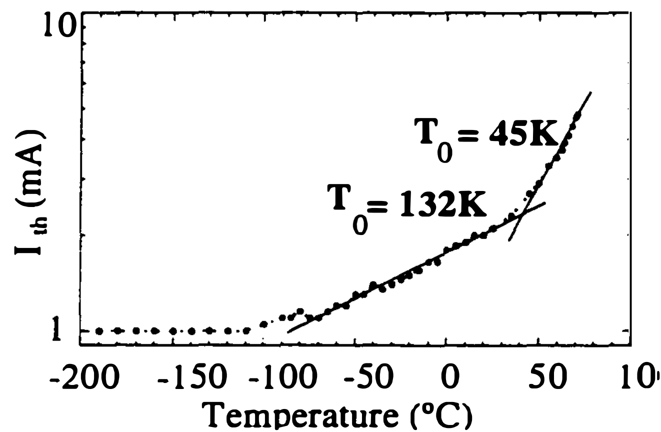

Figure 1.07 Temperature sensitivity of threshold current.

Many factors contribute to the high characteristic temperature measured. The high thermal conductivity of the AlAs/GaAs mirror allows for improved heat dissipation away from the active region. The parabolic doping profile and band structure of the p-mirror ensure high reflectivity and low electrical resistance across the mirror; subsequent re-growth on the p-mirror enabled a lowered voltage drop across the p-fused junction. The placement of strain compensating layers outside the active region allows for the QW barriers to be almost unstrained. Compared to previously used barriers with large tensile strains, a larger valence band offset results, decreasing both the hole concentration in the barriers and intra-valence band absorption, which is the

largest contributor to internal absorptive losses. The combination of these improvements result in device operation at lower threshold current densities and far from the gain saturation regime. This minimizes the carrier density increase necessary to maintain constant gain at elevated temperatures.

1.04 Critical Issues for Long Wavelength VCSELs

Despite the great success of LW VCSELs, there are many problems yet to be overcome. Critical for run to run reliability is the ability to tune the cavity mode. Although this is difficult in a double fused structure, successful tuning has been demonstrated by a number of groups using both all epitaxial structures[23] and single fused structures[24]. Current constriction has always been a problem in long wavelength VCLs. One advantage to using the GaAs-based mirror system is the ability to use high Al content layers for selective lateral oxidation. Only recently have successful techniques for oxide apertures in InP based systems been demonstrated, specifically, using AlAs/AlInAs superlattice layers[25]. Although oxidation can occur at reasonable temperatures (~500°C), the oxidation rate is very slow, requiring times on the order of 30 to 120 minutes for an oxidation depth of 5 to 18 µm. Another demonstrated technique for current constriction is ion implantation[26]. Although the resultant current confinement is good, there are oftentimes problems with poor optical guiding in these devices, as well as a difficulty with scaling down to small dimensions with minimal damage.

Finally, in order to achieve high temperature performance VCLs, the series resistance of the device must be minimized. Specific to fused devices is the problem of a high voltage drop across the fused GaAs-InP p-p junction. The excess voltage drop at this interface is typically on the order of 1 volt at current densities necessary for lasing. In order to circumvent this problem,

results have been presented utilizing localized fusion[16] as well as by using an n-n junction coupled with a tunnel junction active region[27]. An entirely different approach has been to avoid current injection altogether, using optically pumped double fused structures. This approach was first

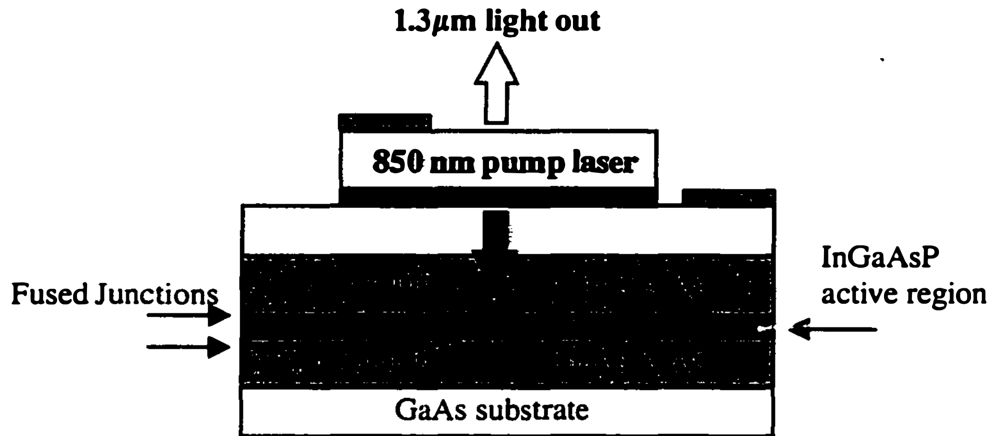

Figure 1.08 Gore Photonics VCL. Optically pumped by an integrated electrically pumped 850 nm diode VCL.

demonstrated by monolithically integrating an 850 nm bottom emitting VCL on top of the double fused structure[28]. A device schematic is shown in Figure 1.08. In addition to avoiding the voltage drop associated with the p-p junction, this approach allows for the use of an undoped structure, eliminating all excess loss. Since the 850 nmVCL is electrically pumped, the laser is then limited by the performance of the short wavelength pump. This structure has demonstrated operation up to 80°C, and output powers as high as 1.3 mW at room temperature.

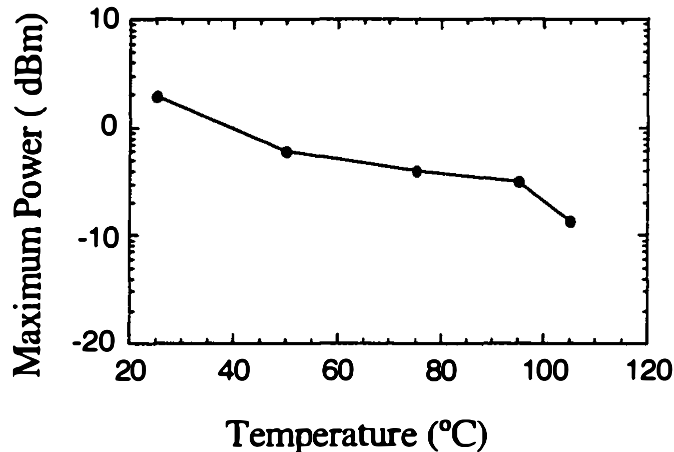

Figure 1.09 High temperature, high power operation of optically pumped double fused VCSEL.

We have since demonstrated a similar optically pumped structure using a commercially available 980 nm in-plane pump laser[29]. This work has demonstrated record high output powers and operating temperatures, as summarized in Figure 1.09. Fiber coupled output powers as high as 2 mW and operation up to 105°C are reported.

1.05 History of Long Wavelength VCSELs at UCSB

There has been great progress in the field of long wavelength VCLs in recent years. Figure 1.10 shows a roadmap of progress made since 1993. The original work on long wavelength VCSELs at UCSB was pioneered by Jim Dudley and Dubravko Babic in the mid-1990s. Dudley demonstrated the first fused VCSEL[30] and Babic demonstrated the first room temperature CW operating electrically pumped VCSEL in 1994[31]. Continuing this work was Near Margalit, who introduced the oxide aperture to the device and developed high temperature operating devices[32], as well as the first transmission experiments with LW-VCSELs in collaboration with Sheng Zhang[33].

However, at that time, a roadblock was met in the continuing development of better performing VCSELs. The fused junction that had enabled the device also became its limitation.

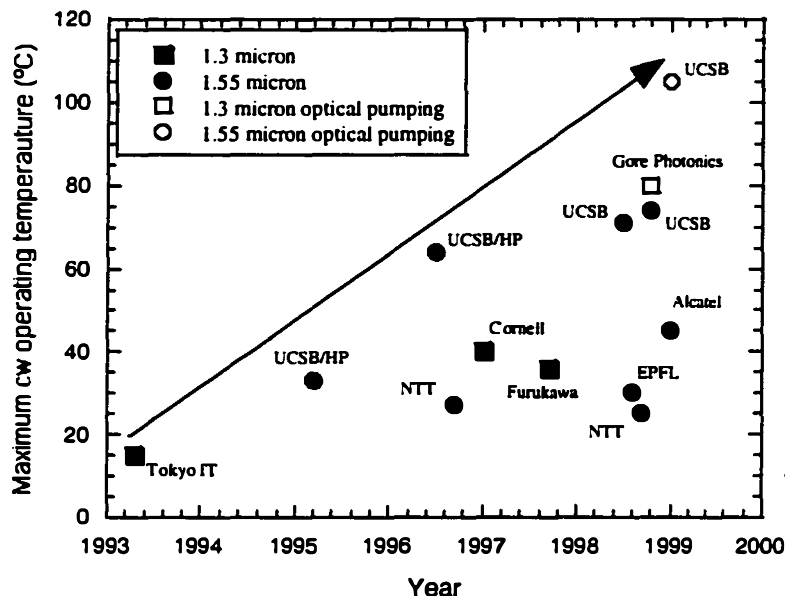

Figure 1.10 Progress in Long Wavelength VCSELs.

To date, the high temperature performance has been limited by a number of factors, difficulty with cavity tuning, current spreading, and joule heating among the most prominent. The ultimate design would allow for a monolithically grown device, preferably on a GaAs substrate to take advantage of the low cost, large diameter bulk crystal as well as the superior mirror systems available. The prospect for 1.3 μm VCSELs grown on GaAs using InGaAsN active layers is good, but it remains questionable whether this system is physically capable of reaching longer wavelengths. This will become important if tunability over the entire 1.3 μm to 1.55 μm range is required in the future. Although the optically pumped structures have shown improved

performance, to maintain cost and performance advantages in the future, an electrically pumped long wavelength VCSEL source is the ultimate goal. To this end, the best reported LW-VCSELs have been achieved through wafer fusion. Double fused, electrically pumped VCLs have demonstrated record high output powers and operating temperatures, and utilize a versatile technology that can be used to achieve lasers throughout the telecommunications frequency band

1.06 Scope of Thesis

This thesis is an in depth examination of an interface; its formation, its properties, and ultimately its role in the creation of state of the art VCSEL technology. It is precisely the GaAs/InP wafer fused interface that has enabled continuous record breaking device performance for the past 7 years at UCSB. Currently, it is also the wafer fused interface that limits the performance of next generation devices. This thesis examines the fused junction in close detail, and attempts to understand the fusing process in order to improve the overall performance of the VCSEL.

Chapter 1 is intended to review the state of the art in the field, and make known the existing problems in LW-VCSEL technology. Chapter 2 introduces the fusion process and examines the structure and chemistry of the fused junction. Chapter 3 reveals the electrical and optical implications of the fused junction critical to device performance. Chapter 4 discusses device design, and for the first time attempts to capitalize on the freedom afforded by the fusion process to create novel device structures. Chapter 5 delves into the specifics of LW-VCSEL processing, and how the fused material affects the processing sequence and tolerances. Chapter 6 examines a number of device generations in terms of static as well as dynamic performance. Finally, in

Chapter 7, this thesis concludes with a summary of device results and suggestion for future direction of LW-VCSEL technology.

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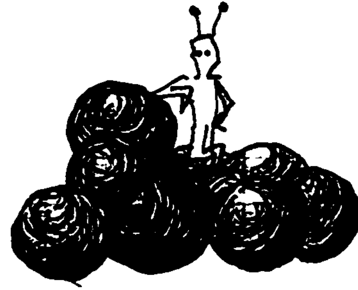

Chapter 2

Chemistry and Structure of the Wafer Fused Interface

2.01 Introduction to Wafer Fusion

High performance semiconductor-based electronic and optoelectronic devices benefit greatly from heterogeneous integration. An effective integration method has remained a challenge due to lattice constant mismatch between semiconductor systems. Monolithic techniques have addressed the issue of lattice mismatched growth with little success. Conventional techniques, e.g. molecular beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD) are limited to strained layer or pseudomorphic growth. During MBE and MOCVD growth of lattice mismatched materials, dislocations form to relax the strain energy as soon as the layer thickness exceeds a critical value, known as the critical thickness[1]. It is energetically preferred for dislocations to nucleate on the surface of the growing layer[2], and glide down through the strained film towards the strained interface. In diamond crystals such as InP and GaAs, the slip plane for dislocation glide are

the family of {111} planes. Portions of the dislocation line will reach the plane of the interface and act as edge type dislocations, relieving strain. However, much of the dislocation line will be present in the film, from nucleation point down to the interface, as a threading dislocation. In the case of GaAs/InP, where the lattice mismatch is 3.7%, the critical thickness of strained layer growth is on the order of 1nm (per Matthews-Blakesly criterion). Beyond this critical thickness, a high density of threading dislocations will be introduced to the lattice mismatched film, and is incompatible with optoelectronic device applications.

The past few years have seen exciting progress in the integration of disparate materials to optimize device performance through a process termed "wafer fusion". Wafer fusion is a special case of direct bonding in which chemical bonds are established directly between two materials at their hetero-interface in the absence of an intermediate layer. For fusion bonding to occur in semiconductors, two (oxide and contaminant-free) crystals are directly bonded and then annealed to yield a crystalline junction. Contrary to monolithic growth of lattice mismatched materials, the difference in lattice constants of the materials being fused is ideally accommodated entirely in the plane of the interface in the form of edge-type or misfit dislocations. Misfit dislocations are not mobile and pose no threat to device reliability. In many cases, devices achieving record performances have been demonstrated as a result of using fusion to eliminate the limitations imposed by lattice matched epitaxy.

This chapter focuses specifically on the GaAs/InP wafer fused interface that has been critical to the realization of long wavelength vertical cavity lasers. Section 2.02 outlines the wafer fusion process and overviews the parameter space available in which to optimize the quality of the fused interface. Sections 2.03 and 2.04 discuss the importance of surface quality

before fusion in terms of surface roughness, defect density, and surface chemistry. A structural analysis of the resulting fused interface is presented in Section 2.05 by way of optical, scanning electron, and transmission electron microscopy (TEM). Section 2.06 details the current view on the GaAs/InP fusion mechanism. To conclude the chapter, an overview of the process parameters and how they interrelate as well as some insight into the most important parameters to control will be given.

2.02 Wafer Fusion Process Overview

The technique of fusion bonding consists of three steps: surface preparation, placement of the substrates into contact with each other, and an elevated temperature anneal while the substrates are in contact under directly applied pressure. The surface preparation steps include removal of oxides and organic contaminants, as well as chemical activation of the surface for interfacial bonding. Bonding by Van der Waals forces occurs when two such clean and smooth macroscopic bodies are placed in contact, while chemical reactions and re-crystallization takes place during the elevated temperature anneal[3].

There are a number of techniques used for surface preparation and placing substrates in intimate contact. Bonding may be classified as "wet" or "dry". In wet bonding, the samples are put together and pressure is applied while the samples are still immersed in an oxide-removing or passivating wet chemical medium. In the dry-bonding technique, the oxides are removed using a suitable chemical, and the samples are placed in contact after the surfaces have been dried. Surface oxidation must be prevented when using the latter technique. Surface preparation may also be carried out in an environment with reduced oxygen partial pressure.

In both wet and dry bonding, it is necessary to allow the chemicals adsorbed at the surface to escape before the bonding occurs. One way of achieving this is to etch escape channels into the substrate. This technique has been successfully used in a number of InP/GaAs fusion experiments [4] and in silicon direct bonding[5]. If the surface is not patterned, and if the channel pitch is too long, the trapped liquids and gases produce large-scale bubbles (size ~ 100 μm)[6], and a large density of microscopic voids (size ~ 1 μm). We have found that an appropriate channel pitch for GaAs/InP bonding is on the order of 200 μm in *both* directions across the sample. The depth of the channels is less important: channel depths of 100 Å suffice, as do channel widths of 3 μm.

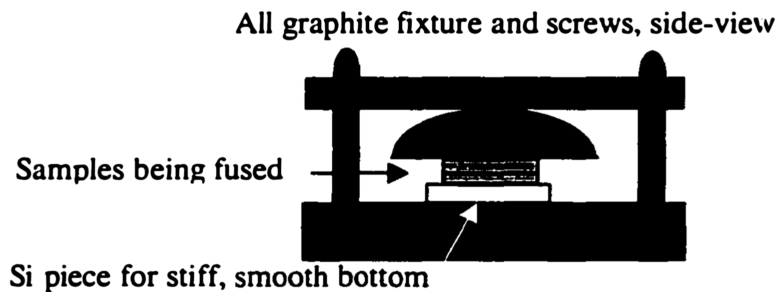

Figure 2.01 Schematic of the fusion fixture with samples in place for fusion. All pieces, including top and bottom plates, hemisphere for uniform load application, and screws are made of graphite. A cleaved piece of silicon is placed between the bottom graphite plate and the samples being fused. The purpose of the Si piece is to provide a stiff, flat surface on which to place the samples, as the graphite plates can bow at high applied pressure.

After channel etching, the surface preparation typically consists of a solvent clean followed by sequential oxidation and oxide removal steps. The surface may be oxidized by oxygen plasma, UV-ozone oxidation[7], or wet chemical oxidation (hydrogen peroxide). The oxide removal may be achieved

using various acids and bases[8]. The exact fusion process used to form LW-VCLs for this thesis is outlined in Appendix A. All devices processed in this thesis were fused with channels under "wet" conditions, meaning the samples were brought into contact in a reducing liquid (typically NH_4OH) or a passivating solvent.

The fusion anneal of GaAs/InP junctions is performed under directly applied pressure and elevated temperature in specially designed graphite fixtures. A schematic of the fusion fixture used for the studies in this thesis is shown in Figure 2.1. After the samples are placed into contact, they are immediately placed into the graphite fixture for the direct application of bond pressure. It has been found that this step is time critical: all movements must be swift to ensure a good bond. The sample sizes used in experiments vary from less than 1 cm^2 to full 2" wafers[9]. The fusion pressure reported in the literature varies over a wide range, from relatively small pressures of 3 kPa[8] 30 kPa, 100 kPa[10], to ~ 3 MPa[11]. The essential factor in the effective application of the force on the samples is its uniformity. It is for this reason that we use a hemisphere of graphite beneath the top plate- to evenly distribute a point source of force over area. The fixture with the samples secured within is then placed into the fusion furnace, and the temperature is ramped to the fusion temperature as shown in Figure 2.02. The fusion furnace is simply a converted LPE furnace: a quartz tube with a three stage IR heater. We have the capability to flow either house Nitrogen or pure hydrogen through the furnace during fusion. Pure (>99.9999%) hydrogen is obtained by using a commercially available palladium membrane hydrogen purifier. Neither gas has been shown to have a significant advantage over the other. The fusion temperatures for GaAs/InP fusion range between 500°C and 650°C, with peak temperatures usually held for less than 30 minutes. Higher pressures result in the ability to carry out lower temperature fusing.

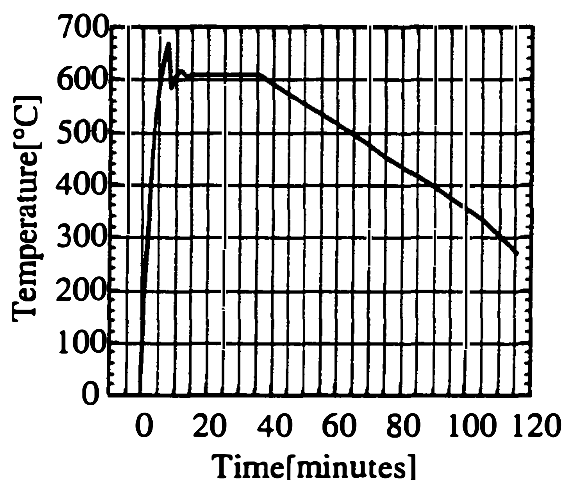

Figure 2.02 Ramp rate and temperature profile of the fusion furnace. A long cool down time is allowed to prevent cracking of the substrate due to difference in thermal expansion coefficients.

The process of fusion bonding of GaAs and InP (or other Ga/In/As/P materials) is not fully understood, but is believed to rely on the proximity annealing of InP with a GaAs cap. It is proposed that as phosphorus desorbs from the InP surface and fills the gaps in the fused junction, indium diffuses laterally and fills the voids, ultimately reacting with the phosphorus to form an InGaAsP alloy[11]. Whereas it was once believed that phosphorus and indium were the primary mobile species during fusion bonding of GaAs and InP, we now have reason to believe that depending upon the bonding temperature, all four chemical species (i.e. Ga, As, In, and P) are mobile[12]. The pressure maintained on the two wafers to be bonded helps to even out the surface non-uniformities.

Upon completion of the heat treatment, one of the substrates is removed via wet chemical etching until a stop etch layer is reached. This layer is best designed to be at least 1000Å thick. All InP structures in this thesis used either an InGaAs or an InGaAsP etch stop layer. The InP substrates were

removed in a 3:1 HCl : H_2O solution with an approximate etch rate of 15 μm/min. This solution can also be heated to 60°C to increase the etch rate to 50 μm/min. Removal of the GaAs substrate has proven to be a bit more difficult. This substrate removal can be done using a spray-etch set-up developed by Babic in a 30:1 H_2O_2 : NH_4OH solution[13]. This method has at times posed problems as the force of the spray is not uniform over a large area. Because the etch is diffusion limited, it is proportional to the supply of etchant species. Once a portion of the sample is finished etching, the spray remains on that portion of the sample as the substrate removal on the rest of the sample finishes. This process can last 30 minutes. Meanwhile, any microscopic poorly fused areas will grow under the spray. To combat this, the sample can be turned around; the vapor generated by the spray is enough to uniformly remove the substrate in a benign manner. We have found that the etch selectivity is greatly enhanced if the etch stop layer is nominally p-doped. Any type of GaAs substrate may be etched using the above described method, but the etch of Al containing compounds seems to be an electron assisted process. P-type doping of the stop etch reduces the electron density at the surface, and thereby enhances the selectivity. Stop etch layers with as little as 67% Al have proven effective. Once the substrate has been removed, the fusion process is complete.

2.03 Materials: surface roughness and epilayer quality

A critical factor in determining the outcome of a fusion is the surface quality of the materials to be fused. An assessment of the surfaces includes an analysis of defect density, surface micro-roughness, and crystal orientation.

2.03.1 MBE grown material

Tolerable defect density

Figure 2.03 Examples of good and poor epilayer quality for fusion. Both images are of 26 period Al_9Ga_1As mirrors (~6 μm growth).

The defect density not only affects the active (electrical and optical) integrity of the material, but also can contribute to problems with morphology as well as substrate removal. Rough surfaces will not fuse: surface aberrations are well correlated with un-fused areas. Figure 2.03 shows a comparison by optical microscopy of good and poor quality MBE grown mirrors. The two major sources of surface defects in the MBE grown material are oval defects and particulate contamination on the epi-ready wafers. Examples of such defects are shown in Figure 2.04. Oval defects arise from sputtering of the Ga source leading to Ga clusters on the growth surface. Particulate contamination, on the other hand, can be avoided by proper surface preparation prior to epi-layer growth. The defect density on the poor mirror is greater than $2000/cm^2$, a number that is unacceptable for device processing. For an epilayer to be considered good enough for fusion and subsequent device processing the defect density must be well below $100/cm^2/\mu m$ growth; for mirrors, this corresponds to 600 defects/ cm^2. Although MOCVD grown materials usually have a much better surface morphology, the thickness of the active layers

grown by MBE is easier to control due to *in situ* growth monitoring techniques (RHEED), an equally important parameter to control in fused LW-VCSELs.

Figure 2.04 Examples of oval defects (left) and particle-induced defects (right) on the growth surfaces of mirrors.

Since defects are preferentially etched due to higher dangling bond densities, high dislocation densities cannot be tolerated in the transferred epilayers. The effects of highly dislocated materials on substrate removal is shown in Figure 2.05. The rectangular etch pits can be directly correlated with surface defect density prior to fusion. The area for active devices has been significantly reduced due to the presence of these defects.

Figure 2:05 Etch pits on surface of mirror after substrate removal. The nature of surface defect is easily identifiable from its shape.

In addition to optical inspection of the materials prior to fusion, much can be learned from atomic force microscopy (AFM). An epi-ready GaAs

wafer has a root mean square (RMS) roughness of 0.3 nm. After cleaning (depending on the cleaning procedure), the RMS roughness can be as high as 1.5 nm. A typical (~6μm thick) solid source carbon doped DBR has a RMS roughness of 4 nm. Doping with gas source carbon leads to wonderfully smooth DBR surfaces, with RMS roughnesses on the order of 0.7 nm. Much of these differences have to do with surface preparation of the wafers before growth, growth temperatures, and dopant levels. In depth analysis of MBE growth conditions is beyond the scope of this thesis.

2.03.2 MOCVD grown material

The most common substrate orientation used for fusion bonding is (001), but many other combinations have been explored[14]. As indicated in the previous section, smooth surface morphology of epitaxially grown layers is critical for successful fusing. This may in turn dictate growth on substrates slightly misoriented from (001). Abraham found this to be true in MOCVD growth of InP-based materials for fusing[15]. The MOCVD growths employ trimethylindium (TMI), trimethylggallium (TMG), tertiarybutylarsine (TBA) and tertiarybutylphosphine (TBP), using growth temperatures ranging from 610°C to 650°C, at either atmospheric pressure or 350 Torr. More details about the growth conditions can be found in reference[11]. Tear-drop-like hillock defects can result in the grown material, resulting from preferential nucleation on the screw dislocations emerging at the surface of the crystal. A misorientation of the crystal surface with respect to the exact (100) orientation creates monatomic steps that are also preferential adsorption sites, making it possible for the growth to proceed without the formation of hillock defects. However, too high a misorientation can give rise to step bunching, also creating surface roughness. The optimum misorientation will produce smooth surface morphology; this depends on growth parameters that influence the

diffusion length of the atomic species at the surface: temperature, growth rate and V/III ratio[16]. Abraham chose a misorientation of 0.2° from (001). Figure 2.06 shows the X ray diffraction spectra of two samples consisting of three compressively strained InGaAsP QWs with unstrained InGaAsP barriers. One sample is grown on a 2° off the (100) substrate whereas the other one is grown on a 0.2° off (100) substrate. The comparison of the two spectra clearly shows that the crystallographic quality of the 2°-off sample is not as good as that of the 0.2° sample. Moreover, the full width at half maximum (FWHM) of the photoluminescence (PL) peak of the 2°-off sample is larger (about double) than that of the 0.2° off sample. This results from the rougher surface of the former sample, with attendant thickness variations that increase the widths of the luminescence peaks.

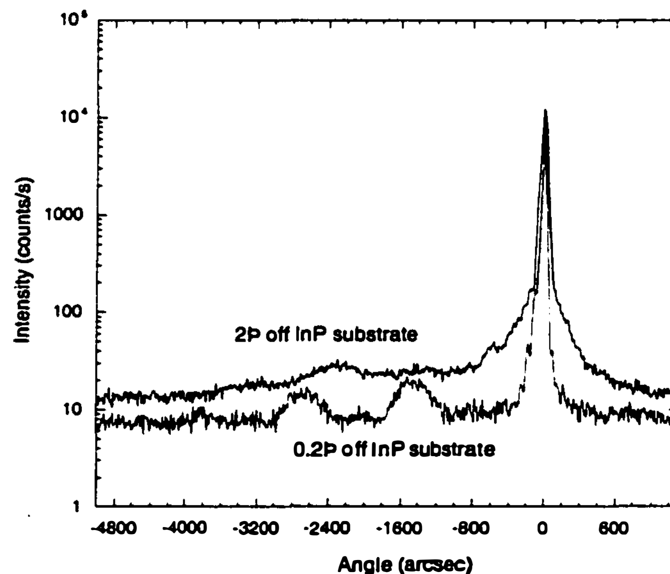

Figure 2.06 X ray diffraction spectra of two samples consisting of three compressively strained InGaAsP QWs with unstrained InGaAsP barriers. One sample is grown on a 2°-off (100) InP substrate whereas the other one is grown on a 0.2°-off (100) substrate. Figure by P. Abraham.

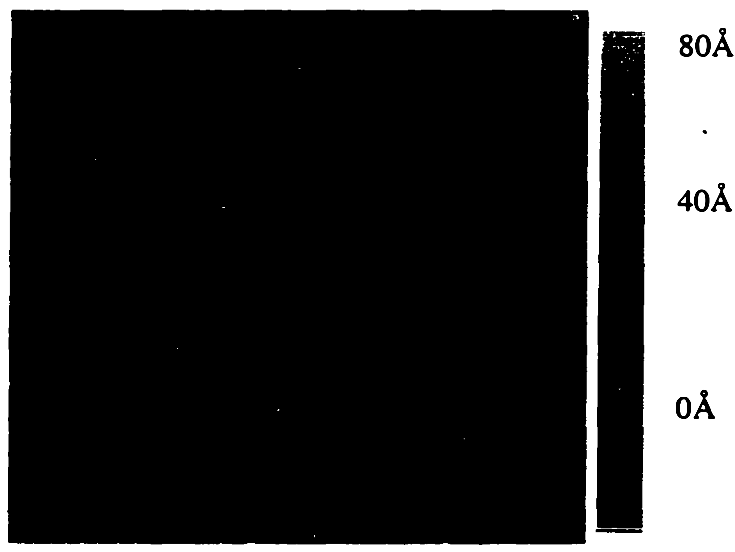

Figure 2.07 AFM image of an InP wafer after surface preparation for fusion. The last step is a 5 minute dip in NH_4OH.

Optical micrograph of MOCVD grown active regions show virtually defect free material. Any surface aberrations are too faint to make out in the quality of this printing, although some surface morphology can be seen using a Nomarski microscope. The RMS surface micro-roughness of a 0.2° miscut InP wafer with active region grown on it is 1 nm.

Although the growth surface is quite smooth, the InP surface is very sensitive to surface preparation. Figure 2.07 is an AFM image of an InP surface treated in NH_4OH, and Figure 2.08 is an AFM image of an InP surface treated with HCl. Both these chemicals have been used as the last step before wafer fusion. Whereas the HCl treated surface maintains its surface quality, the chemical leaves the surface hydrophobically terminated, which will be shown in the next section to adversely affect the fusion quality. The surface treated with NH_4OH, on the other hand, degrades in smoothness, but leaves the surface hydrophillically terminated, and has lead to the best overall uniformity of fusion. Determination of hydrophilic and hydrophobic termination was

done in a primitive way: simply by immersing the treated surface in water and noting the affinity of the water to the surface. In fact, the surface structure seen in Figure 2.07 may directly contribute to the excellent fusion quality. It is known that when reducing the InP surface in NH_4OH, phosphorous is preferentially desorbed, leaving behind indium rich islands along the <1-10> crystallographic directions[17]. This is directly correlated with the structure seen in the AFM image. The 80Å spikes seen in the image are most likely In-rich islands. Since we believe that mobile indium at the fusing interface is crucial to forming the junction, such indium rich islands may aid in the fusion process.

In general, smooth surface morphology is better for initial Van der Waals bonding between two clean surfaces, and roughness resulting from defects is always undesired. However, in the case of InP, where surface roughness may be related to surface chemistry, the benefits of an indium rich hydrophilic surface may outweigh the detriment caused by increased surface roughness in an NH_4OH reducing last step.

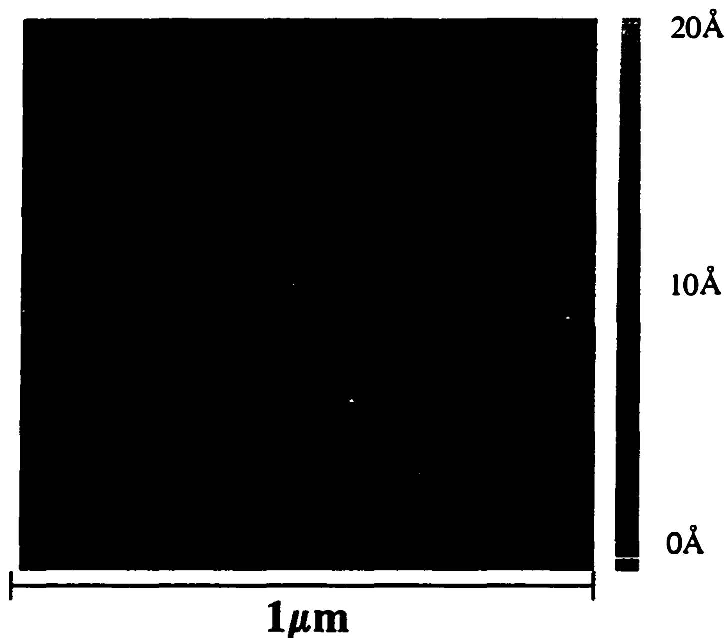

Figure 2.08 AFM image of an InP surface treated with HCl before fusion.

2.04 Surface preparation and interface chemistry

Equally important to the quality of fusion is the bond termination of the two samples being fused. Surface chemistry and passivation have been shown to affect both surface morphology and activation. The wafer fusion process involves many steps to rid the surfaces of both inorganic and organic contaminants. The primary goal of the last surface treatment before fusion is oxide removal. This section investigates the chemical nature of the fused interface, and describes the steps we have taken to both optimize and understand the chemistry of the interface.

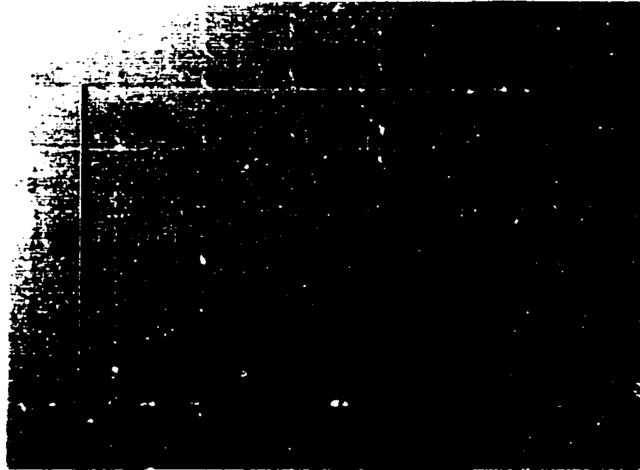

Figure 2.09 Example of a hydrophilically terminated bond, as seen after InP substrate removal. A "blanket" of InP covers the surface- the grid-like channels can be seen with the Nomarski microscope, indicating bowing or depression of the transferred epilayer.

2.04.1 Hydrophobic vs. hydrophilic termination

On a macroscopic level, a clear difference is noted between the quality of bonds using hydrophobic vs. hydrophilic termination of the fusing surfaces. Despite the "better" surface morphology of the HCl treated sample, the overall bond quality is diminished due to the hydrophobic nature of the surface. Optical micrographs of hydrophilic and hydrophobic bonds are shown in Figures 2.09 and 2.10 respectively. Whereas the hydrophilic termination results in uniform bonding, the hydrophobic termination results in a large quantity of macroscopic voids, presumably formed due to trapped gas at the interface. Indeed, in Silicon bonding, hydrophobic surfaces are bonded to form pressure sensors in a similar fashion[18].

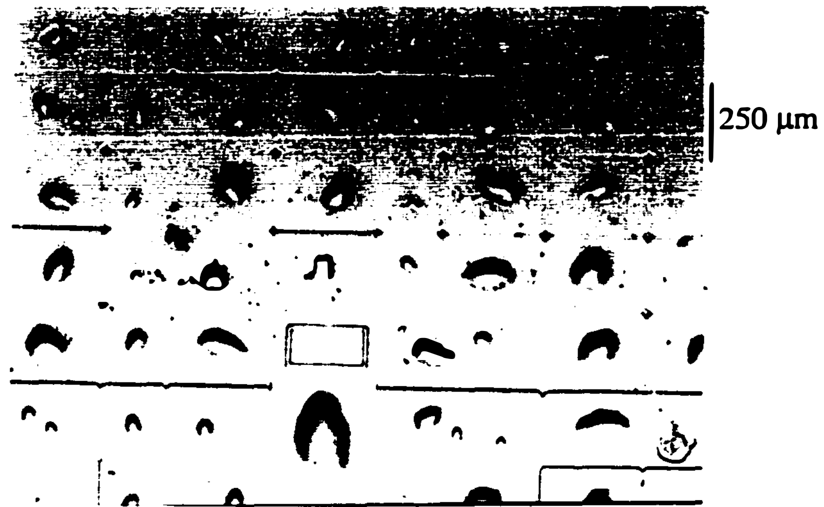

Figure 2.10 Example of a hydrophobically terminated (HCl treated) bond. Between the channels are macroscopic bubbles in the transferred epilayer, presumably holding trapped gas.

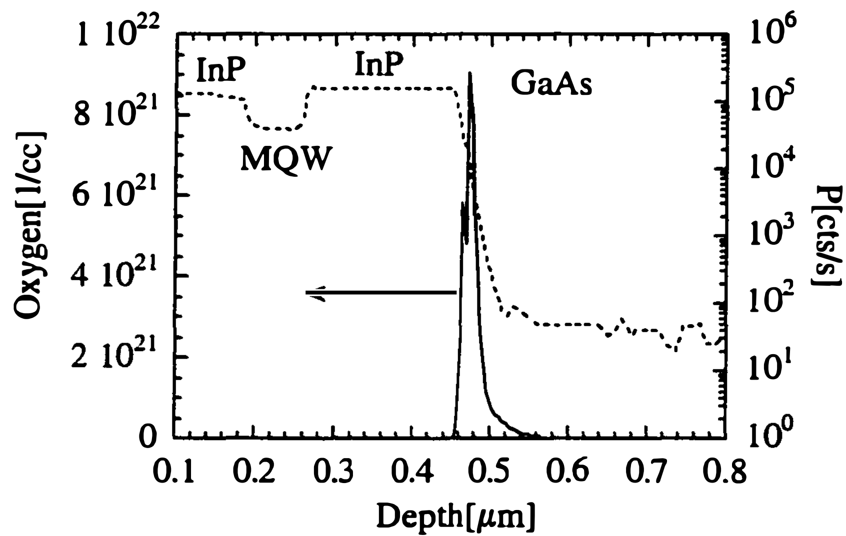

Figure 2.11 SIMS profile of oxygen accumulation at the fused interface. Phosphorous is used as a marker.

2.04.2 Chemistry of the fused interface

Despite all efforts to bring together two macroscopically clean, smooth, and oxide free surfaces to form the fused junction, the wafer fused interface remains highly contaminated. Secondary Ion Mass Spectroscopy (SIMS) performed at Charles Evans Associates has revealed oxygen to be the major contaminant, in addition to high concentrations of carbon and hydrogen at the fused interface. A SIMS profile is shown in Figure 2.11. High levels of oxygen may be a result of our sample preparation procedures, resulting in high O_2 incorporation at the surface. Although the oxide is nominally removed prior to sample transfer to the fusing fixture, a ~ 1 nm thick native may nevertheless form before the onset of the fusing process itself. Indeed, broad area SIMS (within its lateral resolution) reveals uniform coverage of oxygen at the fused interface, as shown in Figure 2.12.

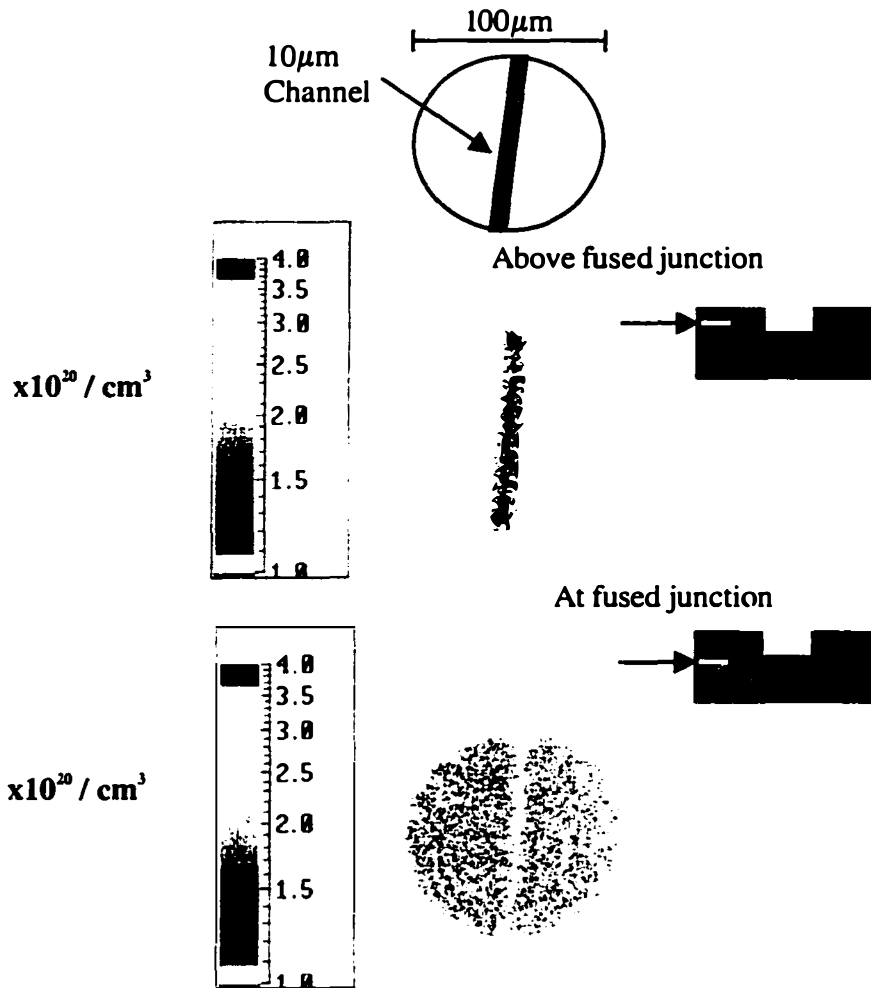

Figure 2.12 Broad area SIMS, performed at Charles Evans Associates, indicating uniform oxygen coverage at the interface.

Many different passivation and oxide removal techniques have been incorporated in an attempt to improve the interface quality. Pre-fusion passivation techniques have included HF, buffered HF, HCl, H_2O, NH_4OH, NH_4S_x, Methanol, and Isopropanol as last step solutions. Although SIMS measurements have indicated orders of magnitude improvement of interface contamination, corresponding electrical tests have shown but nominal

improvement. Table 2.1 is a summary of all surface passivation chemistries attempted, and corresponding levels of organic contamination.

Table 2.1 SIMS results from surface passivation experiments.

Passivation Chemistry	Oxygen Level (atoms/cc)	Carbon levels (atoms/cc)
NH_4OH	$2(10)^{22}$	$3(10)^{18}$
NH_4OH/Methanol	$1.5(10)^{21}$	$1(10)^{20}$
NH_4OH/Isopropanol	$1(10)^{22}$	$1.5(10)^{18}$
HF	$7.5(10)^{20}$	$8(10)^{19}$
Buffered HF	$9(10)^{20}$	$9(10)^{20}$
HF + N_2 Ambient	$8(10)^{19}$	$2(10)^{21}$
HCl	$8(10)^{21}$	$5(10)^{18}$

The best wet surface passivation method in terms of SIMS counts has been the combination of HF acid and pre-fusion handling of the substrate in a glove box with flowing N_2. Concomitant with HF cleans, the carbon content at the interface is also higher[19]. Despite orders of magnitude difference in organic contamination levels at the interface, the overall properties of the fusion remained the same, as will be elaborated on in Chapter 3. The conclusions that can be drawn from these wet chemical passivation experiments are that either the minimal exposure to ambient air during placement in the fusion furnace is enough to form native oxides on the samples, or that the vast accumulation of oxygen at the interface is a result of oxygen diffusing from either the bulk or the wafer-growth interface. Because all liquid fusions were carried out in aqueous solutions, it is not surprising that native oxides would form. An alternative approach would be to fuse under liquid in a non-aqueous solution such as benzene. In addition, the level of oxygen at the start-growth interface is known to be very high, consistently on the order of $8(10)^{19}$ atoms of oxygen per cubic centimeter. Such high levels of contamination at the growth interface indicate that more care needs to be taken

to appropriately blow off the native oxide on the wafers received from the manufacturer. A possible experiment to test this hypothesis would be to fuse an epilayer with a superlattice (SL) at the wafer-growth interface to see if the SL would trap diffusing oxygen species.

In addition to wet chemistry, dry passivation through capping has been attempted, as well as fusing in low oxygen environments, such as N_2 glove boxes, and vacuum fusion environments. Capping of the MBE grown material was done in situ with both arsenic and antimonide; sulfur capping was achieved through wet chemical treatment in NH_4S_x. The arsenic and antimonide capped samples were then transferred to the MOCVD growth chamber that is attached to a N_2 glovebox. The caps were blown off at elevated temperatures (500°C) in the MOCVD chamber under arsenic overpressure and the samples were placed into intimate contact with just grown InP material. Fusion of the sulfur capped material progressed in a similar manner, except in this case, both GaAs and InP samples were capped. All samples were placed in to the fusion fixture and transferred to the fusion furnace in a vacuum suitcase.

None of the dry passivation schemes worked: after fusion at elevated pressures and temperatures, the two respective GaAs and InP samples simply slid off one another. This indicates that the passivation techniques probably left the surfaces of the samples unactivated. In the case of the As and Sb capping, simple capping of the GaAs sample was enough to prevent fusion. In the case of S capping of both InP and GaAs, it is known that blowing off the excess S at 400°C will leave a monolayer of S-terminated bonds on each sample, once again enough to prevent *both* fusion and surface degradation at the elevated fusion temperatures (~630°C). It is important to note that the fusion temperature is higher than the growth temperature of either material

being fused, so the good surface quality is a testament to the fine passivation of the surfaces.

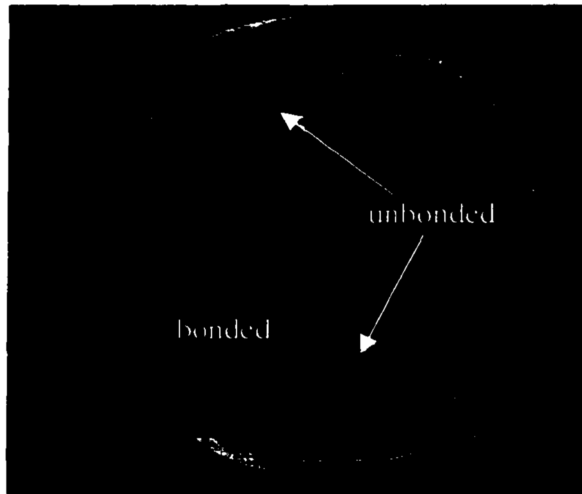

Figure 2.13 Infrared image of 2" UHV wafer bond showing macroscopic uniformity. Bonding by MPI, Halle.

In another effort to optimize the fusion conditions, samples were sent to Goesele's lab at the Max Planck Institute for Microstructural Physics in Halle. The 2 inch GaAs and InP wafers were fused in an ultra high vacuum fusion

Figure 2.14 Optical micrograph of mini voids in the transferred film fused under UHV conditions in Halle. No channels were used.

bonding system[20]. The samples were first heated to 350°C and cleaned with atomic hydrogen. The samples were than placed into contact and bonded at 100°C *without* the application of pressure. An infrared image of the large scale bond is shown in 2.13. Good overall uniformity is achieved, with only a few visible defects.

Upon substrate removal, however, a multitude of microscopic bubbles became apparent, as seen in Figure 2.14. These defects, on the order of 1 μm in size and $5000/cm^2$, are most likely the result of trapped gas at the interface, since no channels were etched into the samples before fusion. A SIMS profile of this interface is shown in Figure 2.15. Again, high oxygen contamination is revealed at the fused interface, with levels as high as $2.5(10)^{20}/cm^3$.

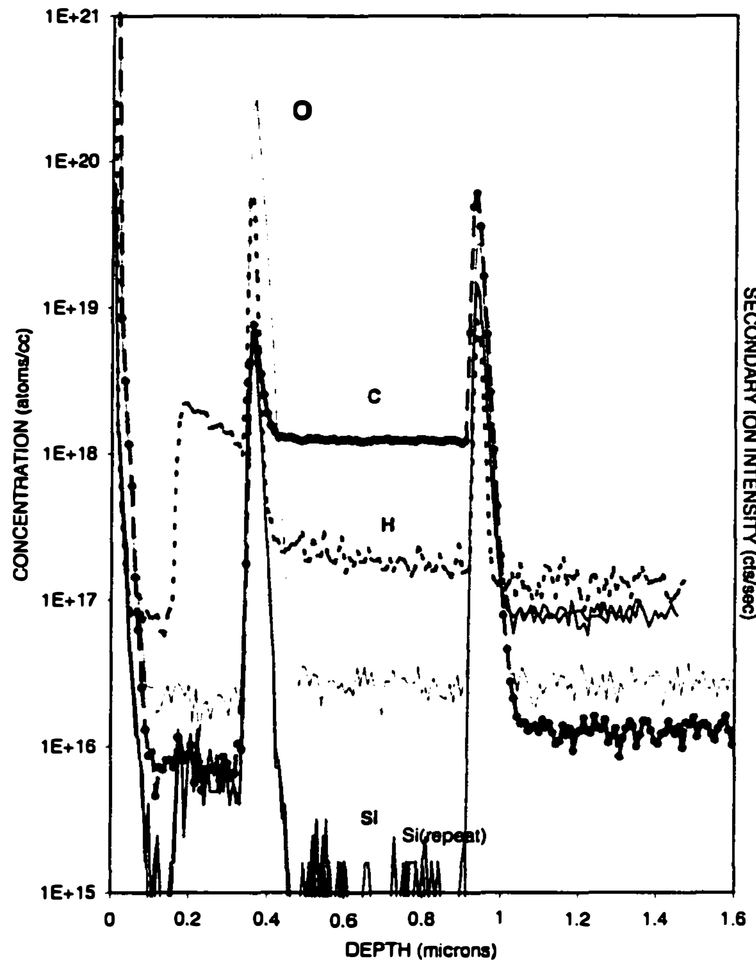

Figure 2.15 SIMS of vacuum fusion performed in Halle showing comparable contamination at the fused interface to normal (non-UHV) conditions.

Conclusions to be drawn from this experiment are that either the *in situ* surface clean was not potent enough to remove the oxygen from the fusing surfaces, or the oxygen at the interface has diffused from the bulk or the epi-growth interfaces. An excellent experiment here would be to heat the samples up enough to desorb the native oxide on the surface before fusion. This would require temperatures on the order of 500°C. However, unless a phosphorous overpressure is available, the InP surface would degrade. An alternate

approach would be to prepare the surfaces in a reducing solution before loading into the UHV bonding system. With the appropriate pre-cleaning process (a HF dip would be optimal), the atomic hydrogen may be potent enough to rid the surfaces of oxygen before fusion.

In addition to organic contamination at the fused interface, mobile dopant species are also present in abundance. Figure 2.16 is a SIMS profile of an InP-based active region fused to a GaAs epilayer. In this case, Phosphorous was used as the marker element to locate the p-p junction. Both Zn, the p-type dopant in InP and Be, the GaAs p-type dopant accumulate at the junction. It is interesting to note the depletion of Be next to the interface, whereas the Zn profile remains constant until close to the interface. Although it is clear that dopant species diffuse towards and accumulate at the fused junction, it is not yet clear to what extent the dopant species situated at the fused junction improve or impair the electrical characteristics.

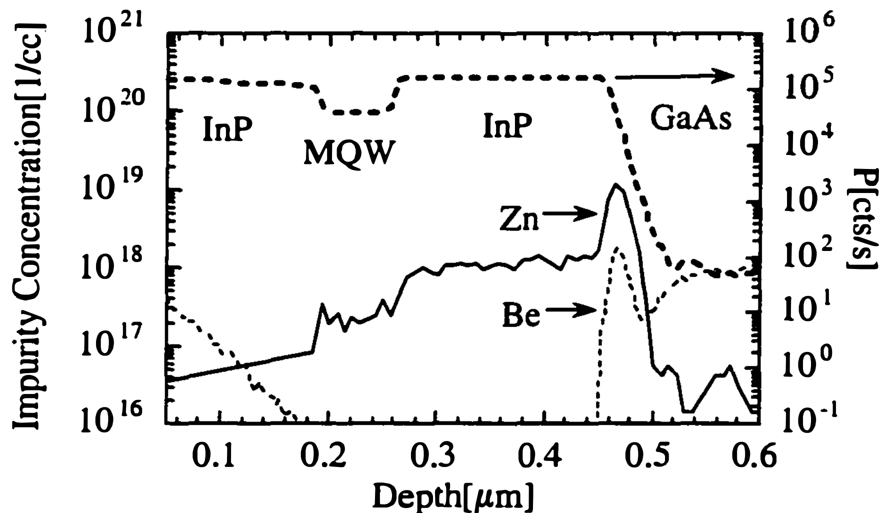

Figure 2.16 SIMS profile of an InP-based VCL active region fused to GaAs. Accumulation of dopant species at the interface is shown.

2.05 SEM and TEM analysis of the fused junction

An important consideration for commercial devices utilizing fused interfaces is the overall uniformity of the fusion, and its ability to be scaled to full wafer sized dimensions. Additionally, dislocations present in active layers of devices are a potential reliability and performance concern. The work done in the vacuum fusion section is a good indication that large scale fusion is readily achieved. Already, companies such as Hewlett-Packard and Gore Photonics have developed 2 inch bonding capability for commercialized devices[21, 22]. However, little attention has been paid to the actual structure of the fused interface. The previous section presented a detailed overview of the chemical nature of the GaAs/InP wafer fused interface; this next section looks at the uniformity and microstructure of the interface through a series of microscopy techniques.

2.05.1 Optical and Scanning Electron Microscopy

Visual inspection deems the quality of the fused interface to be surprisingly good. To date, we have been consistently achieving over 90% fused area over a $1 cm^2$ piece. Liu[23] has demonstrated perfect bonding over 4 cm^2 pieces of InP fused to InP using similar conditions and fixtures. The most important factor affecting large scale fusion uniformity is the smoothness of the fixture, the replacement of the stiff Silicon bottom piece, and the care it takes to apply pressure evenly over the three or four screw fixture.

Figure 2.09 is a fine example of a well-fused sample. However, a closer look under the Nomarski microscope reveals the presence of a cross hatch pattern over the entire sample area, as can be seen in Figure 2.17.

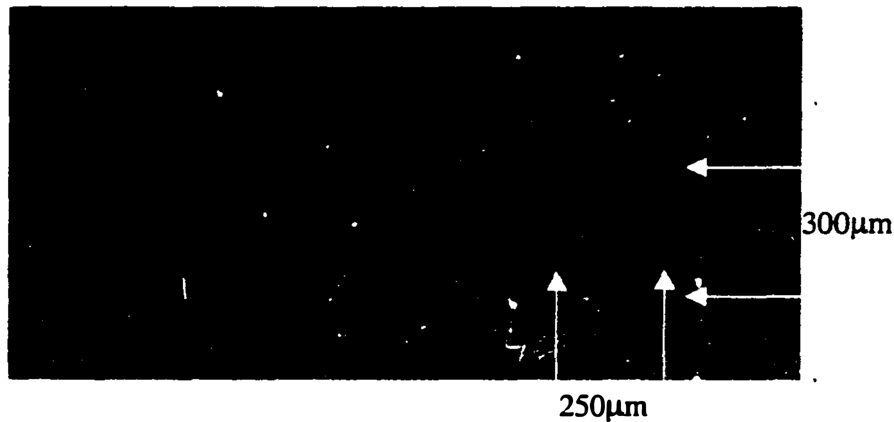

Figure 2.17 Nomarski image of crosshatch pattern on a double fused epilayer. Covered channels are indicated with overlaid arrows.

The cross hatch pattern becomes more pronounced with time, and penetrates deeply into the transferred epilayer. The pitch of the crosshatch is about 1μm, and runs along the [110] and [1-10] crystallographic directions. Similar patterns are seen in strained layer growth. We believe the crosshatch pattern to be a result of coefficient of thermal expansion mismatch between GaAs and InP. The difference in thermal expansion coefficients between InP and GaAs from room temperature to 650°C is 0.1%. Such dislocations are known as volume dislocations as they are not contained at the interface. The volume dislocation density is calculated to be 10^5 – 10^7/cm^2. This is reasonable dislocation density for device application as compared to the expected 10^{10}/cm^2 expected from pseudmorphic growth. Only this dislocation network has been shown to have an effect on the nonradiative recombination of minority carriers in the interface region. Using electron beam induced current microscopy (EBIC), Ram *et al.* uncovered a network of dark line defects at this interface that correspond to this exact spacing[11]. More studies would need to be done to confirm this association, however.

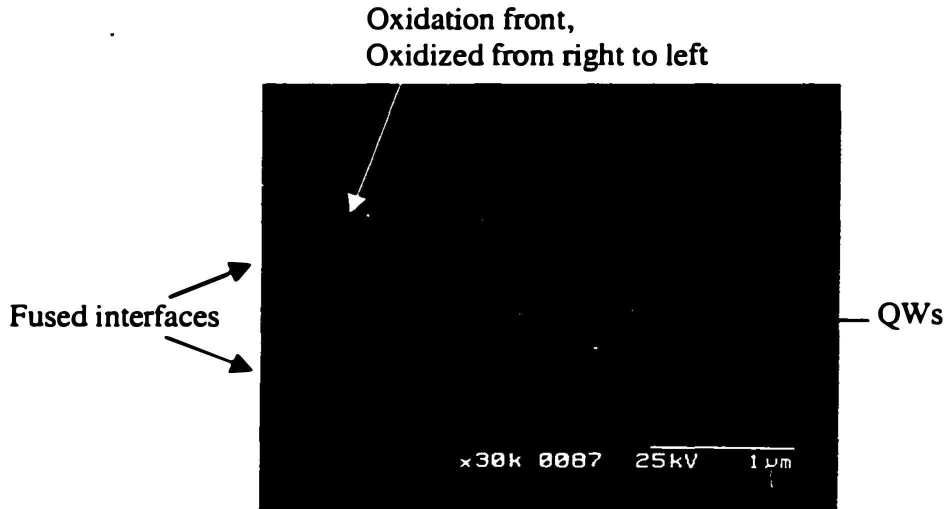

Figure 2.18 A double fused VCL structure. The interfaces are barely detectable. The current confining oxidation layer, partially oxidized, is also noted.

In most cases, scanning electron micrographs show a virtually undetectable fused interface. It is, in fact, very difficult to locate the interface without looking for the channels. An example of a well-fused double fusion is shown in Figure 2.18. On the rare occasion, however, we have seen fused interfaces that indicate the presence of voids. Figure 2.19 shows such an example of a double fused laser structure that did not lase. An interesting experiment here would be to run current through this interface to note the effect of high current densities on these microscopic voids.

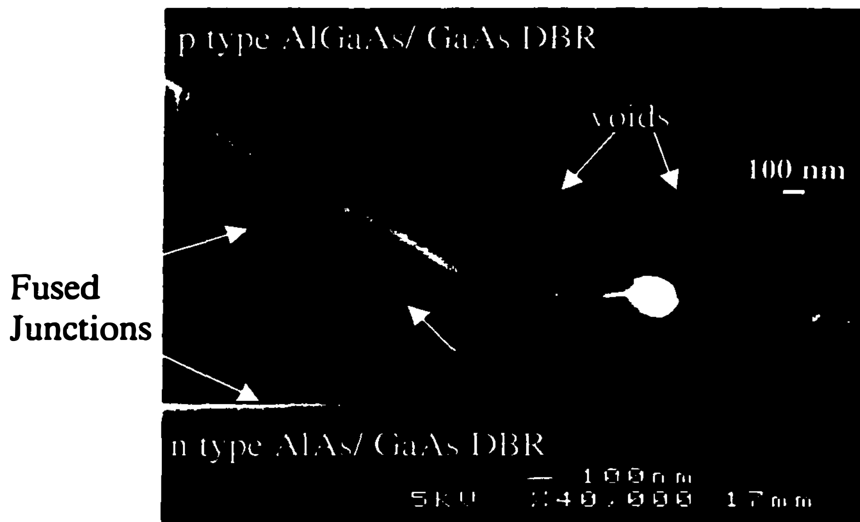

Figure 2.19 Scanning electron micrograph of double fused laser structure that did not lase, presumable due to the poor fusion quality. Cleave damage cuts diagonally across the image from top left to bottom right.

2.05.2 Transmission Electron Microscopy (TEM) Analysis

Optical microscopy tells us that we have a very uniform and reliable fusion process over relatively large size pieces. Cross-sectional SEMs tell us that the macroscopic uniformity is also quite good. SIMS scans give us an idea about the contamination levels of the interface. Perhaps the most important characterization technique to evaluate the quality of the fused junction is transmission electron microscopy. TEM analysis gives us an idea of the actual microstructure and chemical make up of the interface and insight into the fusion mechanism itself. This section will overview both plan view and cross-sectional analysis of the GaAs/InP fused junction, however, for two impeccable resources, the reader is referred to references[12, 24]: two independent groups with whom we have collaborated closely.

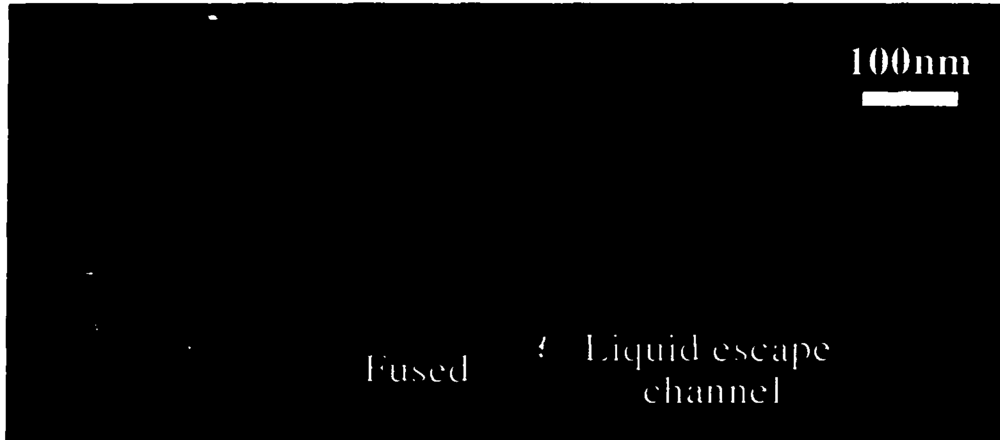

Figure 2.20 Plan view dark field TEM of the fused interface. TEM by Mathis, UCSB.

2.05.3 Plan view TEM Analysis

Initial plan view TEMs of our fused junctions were done by Mathis at UCSB. The sample structure was simple: a transferred epilayer of InP fused onto a GaAs substrate. The sample preparation was done using wedge polishing followed by a bromine etch and Ar+ sputtering. Figure 2.20 is a plan view TEM of a 25 nm InP film transferred to a GaAs substrate. The interesting feature is the presence of many light areas in the TEM that correspond well with the AFM of the NH_4OH cleaned samples prior to fusion. Surface features resulting from the pre fusion clean are preserved through the fusion process, resulting in small islands of a possible In-rich compound at the interface. These features are seen only in the fused area, and not in the channel regions where fusion does not occur. The presence of these features is also noted by other groups doing TEM analysis of both UCSB and other group's fusions[10]. Subsequent EDX analysis by the two aforementioned groups have revealed these "cavities" to be either In-rich (Sagalowicz)[24] or In-depleted (Jin Phillipp) [12].

In addition to large (~20 nm) interface species such as these, the dislocation network at the interface has been more carefully analyzed to reveal the presence of four distinct dislocation networks situated at or nearby the fused interface. The four dislocation networks accommodate respectively the lattice mismatch, the tilt misorientation, the axis misorientation, and the thermal mismatch between GaAs and InP. Ideally, the first network, resulting simply from lattice mismatch, would be a network of edge-type dislocations with 11 nm spacing in both the <110> and <1-10> crystallographic directions. This would correspond perfectly with the 3.7% lattice mismatch in the GaAs-InP systems, assuming bonding at 630°C. In diamond structures perfect dislocations have Burgers vectors of $a/2\langle 110\rangle$, and glide on $\{111\}$ planes. Misfit dislocations relax the lattice misfit most efficiently. In order to accommodate the lattice mismatch between the two lattices of the wafers, interface dislocations form at bonding temperature, T_{bond}, when the atomic bonds across the two wafers are constructed. The calculated distance, *d*, between misfit dislocations is found by the relation:

$$d = b/\varepsilon$$

where $b = a/2^{1/2}$ and is the Burgers vector of an edge-type dislocation, a is the lattice constant, and ε the lattice mismatch, both at the bonding temperature. Using this simple formalism, Jin-Phillip's analysis of our fused junctions reveal the presence of a network of edge type dislocations with an average spacing of 10.5 nm, rather than 11 nm, indicating that bonding may take place at a lower temperature than the fusion annealing temperature of 630°C. Indeed, calculations using Vegard's law and the coefficients of thermal expansion of GaAs and InP suggest that bonding may occur at temperatures as low as 550°C.

The second and third networks arise from the tilt of the fused surfaces, and the slight misorientation of the crystals during fusion. As alluded to

before, we do not use perfect (001) crystals for fusion; typically we use 0.2° offcut samples for MOCVD grown InP. Because of the offcut, steps are present on the surface of the InP sample. Sagalowicz has identified an array of dislocations with a burger's vector perpendicular to the interface that can be attributed to the presence of these steps. The third network comes about because we just visually align the cleavage planes of the samples before fusion, and at times are as much as 3° off normal. These two networks of dislocations are *not* contained in the plane of the fused interface and do indeed have a component of tilt to them. Finally, the fourth network of dislocations is that which arises from difference in thermal expansion, as described. This network could be minimized by fusing at lower temperatures such as at 100°C as was demonstrated by the bond in UHV fusion system at MPI, Halle.

Another interesting TEM image is the one that shows the presence of a

Figure 2.21 Bright field plan view TEM image of an InP to GaAs fusion. Crystal orientation is indicated with an arrow.

second phase "cavity" region or intermixed region of material aligned along the <110> directions, shown in Figure 2.21. These features can possible be attributed to enhanced diffusion of species at the fused interface along the steps originating from the InP crystal miscut. Further analysis is clearly necessary to substantiate this hypothesis.

2.05.4 Cross-sectional TEM analysis

Cross-sectional and high-resolution microscopy of the fused interface reveals that most of the fused area is not crystalline across the junction. In fact, we typically see a 6-8 nm amorphous layer that is the interface. This, according to standard interface theory, is exactly what we expect. No interface can be atomically smooth. With our description of the fusion process, we actually expect a large degree of mobility at the fusion temperatures: 630°C is above the growth temperatures of either constituent material. Figure 2.22 shows a high-resolution image of the fused junction. We estimate that about 5% of the junction area is comprised "cavities" filled with a combination of native oxides and intermixed semiconductor. Within the amorphous region exist some areas of crystallinity. EDX analysis by Phillip has revealed the smaller crystalline regions to be comprised of either an α-Al_2O_3 or α-Ga_2O_3, possibly formed during the high temperature, high pressure fusion anneal of the amorphous native oxide region.

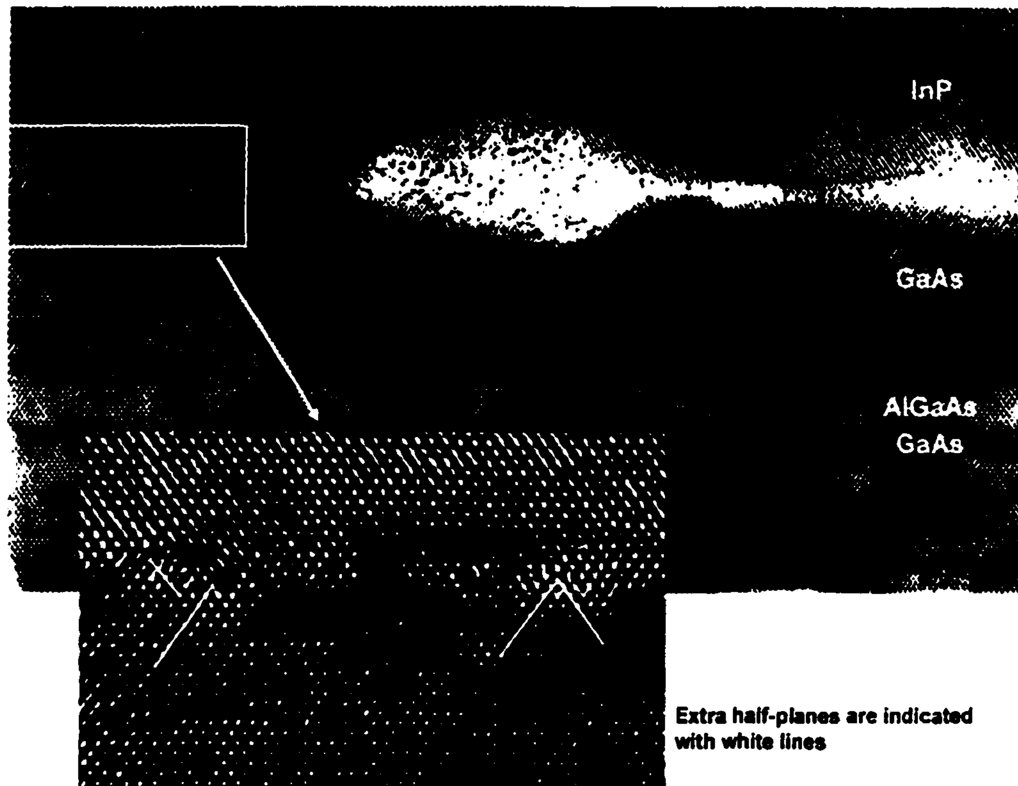

Figure 2.22 HR XTEM of the GaAs / InP fused junction courtesy of Jin-Phillip, MPI, Stuttgart.

2.06 Mechanism of GaAs/InP wafer fusion

In the past, the GaAs – InP fusion mechanism has simplistically been described as a combination of P desorption from the InP surface and In mobility at the junction. Indeed, it is considerably easier (lower temperatures, pressures, and better fusion uniformity) to fuse In-based materials than materials without In. However, our experiments indicate that the fusion mechanism is much more complex. Depending on the actual bonding and annealing temperatures, differences in thermal expansion coefficients will cause varying amounts of plastic and elastic strain at the forming interface. This will affect both the dislocation networks that form as well as the amount

of intermixing that occurs at the fused interface. It has previously also been shown that the high temperature and applied pressure of the fusion process affect not only the interfacial area, but areas far removed from the interface as well. Severe intermixing of quantum wells placed in the vicinity of the junction is directly related to the fusion process, as will be presented in detail in Chapter 3.

The fusion mechanism is described as follows: networks of edge-type dislocations accommodating lattice mismatch form at T_{bond}, as do the networks of dislocations that accommodate wafer tilt and rotation misalignment. Any surface contamination is sealed at the interface within an amorphous layer. The fourth dislocation network is comprised of volume dislocations, and arises from the strain resulting from coefficient of thermal expansion mismatch. This network forms during cooling of the fused sample. However, the difference in thermal expansion coefficients plays a greater role in the definition of the fused interface, specifically in relation to the chemistry of the forming interface.

The chemical nature of the fused interface is affected by the interdiffusion of constituent species at the forming interface. If the bonding takes place at T_{bond}, the interdiffusion of the four elements is driven by concentration gradients, chemical interaction, and thermal strain. In order to quantify the diffusion of constituent species at the fusing interface, EDS analysis was performed by Jin-Phillip in a dedicated STEM with a resolution of ~3 nm. She has demonstrated interdiffusion of all four chemical species across the fused interface. It is proposed that as the annealing temperature is raised above T_{bond}, where the structural bridge between the two materials is formed, any increase in temperature results in "a thermal misfit between the two wafers which dilates the InP lattice and compresses the GaAs lattice. An interdiffusion of group-V elements would compensate this misfit. During cooling down the thermal misfit causes the InP lattice to be compressed, and

the GaAs lattice to be dilated. Interdiffusion of group-III elements enables a compensation of the thermal misfit." Upon cooling below the bonding temperature, the samples experience the opposite sign of stress, and interdiffusion in the opposite direction occurs. Because of the ~0.09% difference in coefficient of thermal expansion between room temperature and T_{bond}, there is still considerable thermal stress between the materials, resulting in the formation of the fourth dislocation network between T_{bond} and 400°C below which temperature dislocations become relatively immobile. This network lies in the <110> directions, is not situated in the plane of the interface, and is potentially hazardous to device applications.

2.07 Summary of fused junction characteristics

The fusion process and fused junction are complicated and still not fully understood. Since the fusion mechanism is materials system dependent, we focussed specifically on the GaAs – InP system. This chapter highlighted some of the critical factors to control in practical wafer fusion, namely, epilayer and surface quality, surface cleaning procedures, and passivation. The importance of surface activation as well as the presence of channels was stressed. We also looked at the interface microstructure. The presence of four individual dislocation networks was revealed, as well as an interface thickness of ~7 nm and the presence of many "cavities" of a second phase of material, constituting about 5% of the interfacial area. The collaboration of UCSB with expert microscopy groups in both France and Germany has lead to a deeper understanding of the mechanism of fusion, especially through the careful analysis of interdiffusion at the interface and extrapolations of the bonding temperature through dislocation spacing and analysis. It will be shown in the next chapters that the microstructure of the interface does indeed affect the

macroscopic electrical and optical properties of devices to be made with wafer fusion, and ultimately, will be their limitation.

2.08 References

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Chapter 3

Electrical and Optical Analysis of the Fused Junction

Most important to the integrity of vertical cavity lasers is how the fused junction will affect the electrical and optical properties of the device. As known, the quality of epilayers is crucial to device performance and reliability. This chapter looks in depth at how the nature of the fused interface affects parameters critical to device performance. Section 3.1 looks at the electrical characteristics of the GaAs-InP fused junction through a series of I-V characteristics. The bonding conditions were varied in an attempt to reduce the resistance of the fused junction. Approaches included surface passivation and orientation as well as bulk parameters such as doping and applied pressure. Section 3.2 is an in depth analysis of the effect the fused junction has on the optical quality of the adjacent materials. Both room temperature and low temperature photoluminescence (PL) studies were performed. Additionally, an intermediary superlattice was introduced to better mediate the effects of the fusion process on the optical quality of the fused material.

3.01 Electrical Characterization

3.01.1 Current – Voltage Characteristics

The electrical characteristics of fused junctions have been made primarily through I-V measurements made across the fused junctions. Several parameters are known to influence the character of the junctions. The I-V characteristics critically depend on the presence of potential barriers arising from discontinuous energy-band lineups and interface charge. Theoretical considerations predict a staggered band lineup between strained GaAs/InP with the GaAs valence band several hundred meV above that of InP[1]. However, no agreement between theoretical and experimental values of band offset has yet been reported. The cleanliness of the surfaces before bonding, namely, trapping of contaminants at the junctions, will have an adverse effect on the conduction of carriers. Potential barriers at fused junctions can originate from thin oxide layers or a high concentration of surface charge introduced by surface contamination before bonding. In the previous chapter, Oxygen has been found to be the major contaminant, in addition to high concentrations of carbon and hydrogen at the fused surface. Although the oxide is nominally removed prior to sample transfer to the fusing fixture, a ~ 1 nm thick native oxide may nevertheless form before the onset of the fusing process itself. Surface oxide layers and charge affect both electron and hole flow, but because of the lower electron effective mass this has a greater impact on the holes. For this reason, among others, n-n-junctions perform better than p-p-junctions. Indeed, ohmic conduction across n-n junctions has been demonstrated[2].

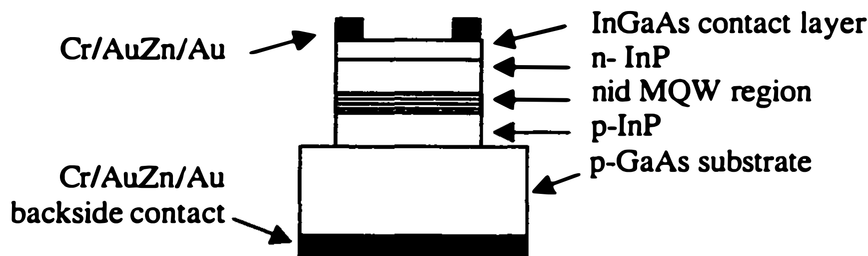


Figure 3.01 Schematic of I-V test structure. An active region fused to a GaAs epilayer.

The primary focus of our studies has been conduction across the p-p fused interface. It is the transport across this interface that is important to consider in fused LW-VCLs. In particular, we inject current through a pp junction precisely because of the lower mobility of holes, leading to better current constriction in the layers beneath the oxide aperture. Of course, this advantage is meaningless if the voltage drop across the fused junction causes more current spreading than using an n-n interface. A more detailed description of device design considerations is given in Chapter 4. The structure used for testing the voltage drop across the fused junction is shown in Figure 3.01. Typically, an active region is fused to a GaAs epilayer grown on a p-doped substrate. Such a structure affords us much information. One can both fuse actual device structures and ohmically contact the n-doped InGaAs etch stop layer, minimizing contact resistance. In addition, the same structures can be evaluated for luminescence intensity from the MQW active region after fusion. A typical I-V curve across this structure is shown in Figure 3.02. The voltage across the pin active region diode is marked with a dashed line. The voltage across the fused junction is estimated to be 1.2-1.4 V, much in excess of the predicted band offset on the order of hundreds of meV. The voltage drop is a highly reproducible feature of the electrical performance of the fused junction and is significant to the performance of fused devices utilizing a p-p

fusion. The power dissipated at this junction severely limits the high temperature operation of our devices. In addition, large resistances at the fused junction will cause additional current spreading before the carriers pass through the junction, increasing threshold gain. The second feature on this I-V characteristic is a kink in the I-V. The ominous kink will be discussed in Section 3.01.2.

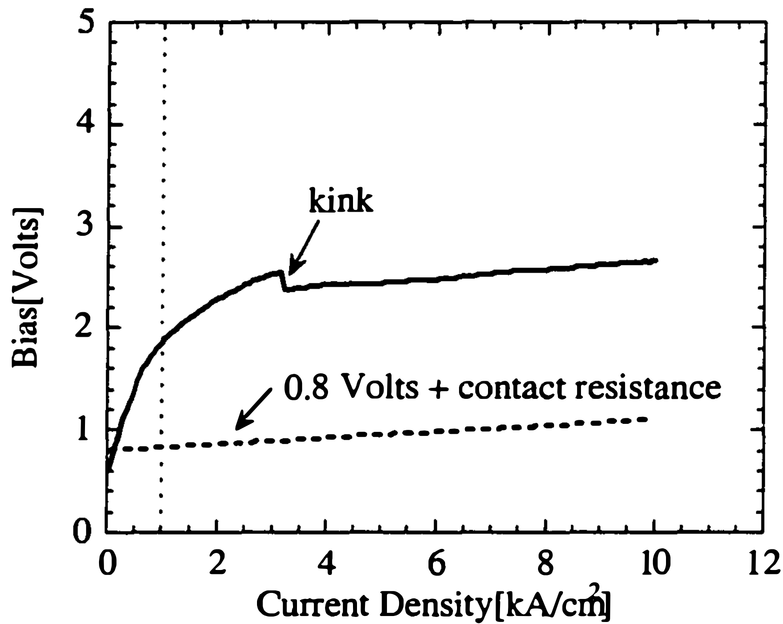


Figure 3.02 I-V characteristic of InP-GaAs fused junction. The diode voltage is marked by a dashed line. The voltage drop across the fused junction is estimated to be 1.2-1.4V.

Surface Passivation

In order to investigate the cause of the large voltage drop at the interface, many different passivation and oxide removal techniques have been incorporated in an attempt to improve the interface quality. Pre-fusion passivation techniques included HF, HCl, H_2O, NH_4OH, NH_4S_x, Methanol, and Isopropanol as last step solutions. Fusions were also done in a dry state in the

UHV system at MPI, Halle. Although SIMS measurements discussed in Chapter 2 indicated orders of magnitude differences in the amount of oxygen and other organics at the fused interface, the result of the electrical studies of these interfaces was not promising. A table of voltage drops across the fused junction at 1.5 kA/cm^2 is given in Table 3.1. Surprisingly, the voltage drops across the interface remain unaffected by the orders of magnitude difference in contamination levels between the passivation techniques. Although one remarkable result was obtained using buffered HF, it proved impossible to repeat this result. Even this result did not correspond with the lowest obtained oxygen concentration at the interface. Either the contamination levels at the fused interface are simply *all* above the concentration necessary to improve the characteristics, or the nature of the fused junction voltage drop is not a direct result of the fused interface contamination levels.

Table 3.1 Comparison of passivation technique, oxygen levels, and voltage drop at the fused interface. We report one hero result of 0.9V dropped at the interface, but were unable to reproduce it in 4 successive processing runs.

Passivation Chemistry	**Oxygen Level (atoms/cc)**	**Voltage drop at 1.5kA/cm^2**
NH_4OH	$2(10)^{22}$	1.2
NH_4OH/Methanol	$1.5(10)^{21}$	1.2
NH_4OH/Isopropanol	$1(10)^{22}$	1.3
HF	$7.5(10)^{20}$	1.2
Buffered HF	$9(10)^{20}$	**0.9 (hero)** **1.2**
HF + N_2 Ambient	$8(10)^{19}$	1.2
HCl	$8(10)^{21}$	1.35
UHV fusion with H+ clean	$2.5(10)^{20}$	1.2

Misorientation

In the absence of surface contamination, another parameter that can influence the electrical properties of the junction is the exact matching of the

bonds at fused junctions. Since the main reason for GaAs/InP fusion bonding is to transcend the lattice matching requirement, exact bond-for-bond matching of [100] substrates is not possible, but bonding off-axis cut substrates may help reduce the number of dangling bonds and dislocations. The bonding of off-axis substrates of GaInP on GaAs[3] has revealed that small deviations from on-axis bonding result in dramatic increases in junction resistance. GaAs/InP bonding between different substrate orientations also results in reduced junction conductivity[4]. Since the surfaces of different III-V compound semiconductors have different oxidation properties and terminations, certain surface preparations and procedures may produce different results for different materials. A good example is that of [011] GaP/[001] InGaP in which there is a large difference in the I-V characteristics between in-phase ([110] axis of top wafer *perpendicular* to the [110] axis of bottom wafer) and anti-phase bonding ([110] axis of top wafer *parallel* to the [110] axis of bottom wafer)[3]. In the case of (001) GaAs on (001) InP, the difference is hardly noticeable[5]. In general, we do not align our samples in-phase before fusion.

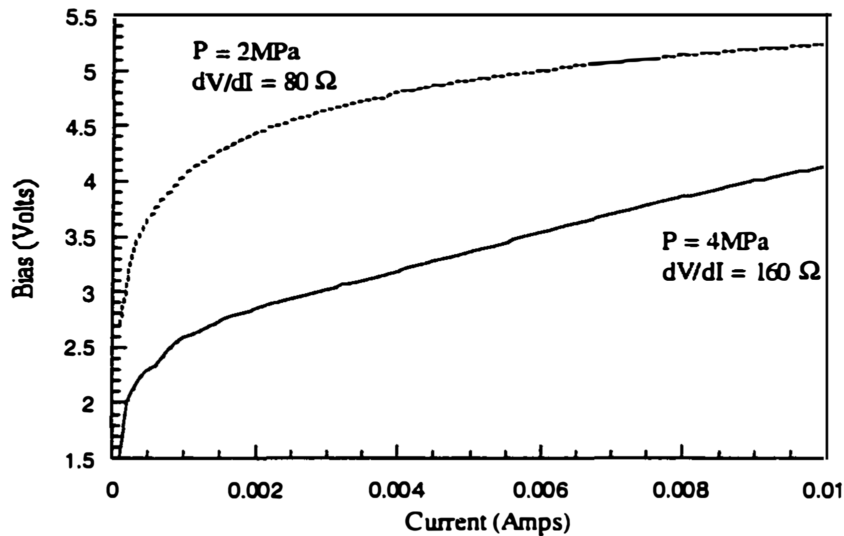


Figure 3.03 Pressure dependent fusion study. Higher applied pressure reduces the fusion voltage for a given set of materials.

One experiment we tried, however, was to calculate the miscut of GaAs wafer necessary to have equal numbers of dangling bonds on both the GaAs and InP wafers being fused. This angle was determined to be 21.9°. Two sets of offcut wafers were ordered and fused, offcut 21.9° towards the [110] and [111] directions, respectively. Doped epilayers were grown by MBE on the semi-insulating substrates to yield doping densities of $1(10)^{18}/cm^3$. The results of the fusions were voltage drops of 3-10 V across the interface, much higher than anything previously measured. The auspiciously high voltages could be attributed to surface morphology of the MBE growth. Adequate time for optimization of the growth and doping of such severely offcut crystals was not allotted. The passivation chemistry of the 21.9° offcut surface could be considerably different, also affecting the bond.

Pressure

The effect of varied pressures on the quality of the fusion was examined. Due to the enhanced diffusion coefficients with increased temperatures and pressures, it is thought that a larger degree of intermixing might improve the overall junction characteristics. We fused samples at applied room temperature pressures of 2MPa, 4MPa, and 6MPa. In order to assure that the pressure ratio was calibrated (temperature dependence of applied pressure varies with the geometry of the fixture), we simply changed the areas of the samples being fused. The resultant I-V characteristic is shown in Figure 3.03. Specifically, we found an improvement in electrical quality of the fused junction with pressure. However, the PL intensity from these active regions was degraded with increased pressure, probably due to increased intermixing in the quantum wells.

Doping

In all fused devices, the doping levels of the epilayers is of primary importance. Specific to LW-VCSELs, the single largest contributor to loss is free carrier absorption in the InP and GaAs p-doped layers. It was shown by Margalit [6] that higher zinc levels at the fused interface improve the electrical characteristics. Jin-Phillipp demonstrated[7] that higher levels of zinc in the fused epilayers contribute to a larger degree of intermixing at the junction. It is clear from the SIMS analysis in the previous chapter that dopant species diffuse towards and segregate at the fused junction. However, it remains in question to what extent the dopant species situated at the fused junction can improve the electrical characteristics. Similarly the ramifications of such doping levels on the optical properties of the device must equally be considered.

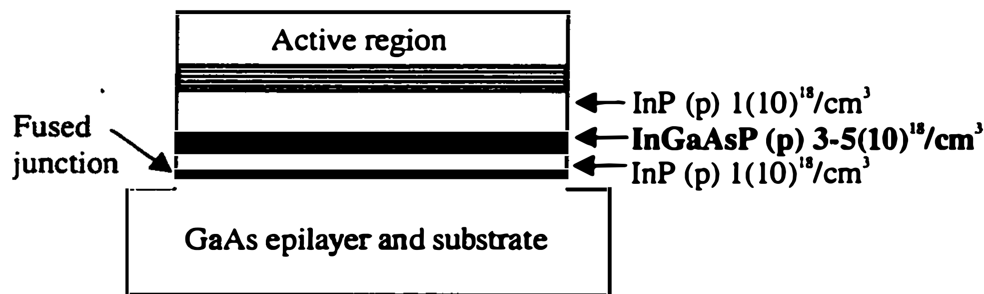


Figure 3.04 Schematic of structure for improved zinc incorporation at the fused junction. The InGaAsP layer is 75Å thick, as is the InP layer closest to the junction.

In order to reduce the fused junction resistance, one might try to increase both the doping and the intermixing at the fused interface as much as possible.. Drawing on the conclusions made from both the pressure dependent studies, the TEM analysis, and previous electrical characterization, zinc is targeted as the most important dopant to control. Unfortunately, zinc is also the most difficult dopant with which to achieve high doping levels. Reaction chemistry limits the amount of Zn incorporated into an InP film to a maximum of $1(10)^{18}/cm^3$ in the UCSB reactor. Studies with high delta doping of Zn at the interface produced no improvements in results. However, because it is possible to dope 1.2 μm InGaAsP to levels as high as $3\text{-}5(10)^{18}/cm^3$, we experimented with fusing a thin quaternary layer 7.5 nm removed from the fusing surface. A schematic of the fused film is shown in Figure 3.04. With this structure, the results were quite promising. The I-V characteristics are shown in Figure 3.05. When the diode voltage drop is neglected from the measurement (~0.8V), the remaining voltage from across the fused junction plus the contact resistance is found to be a couple hundred meV. Possible mechanisms for this are described in the next section.

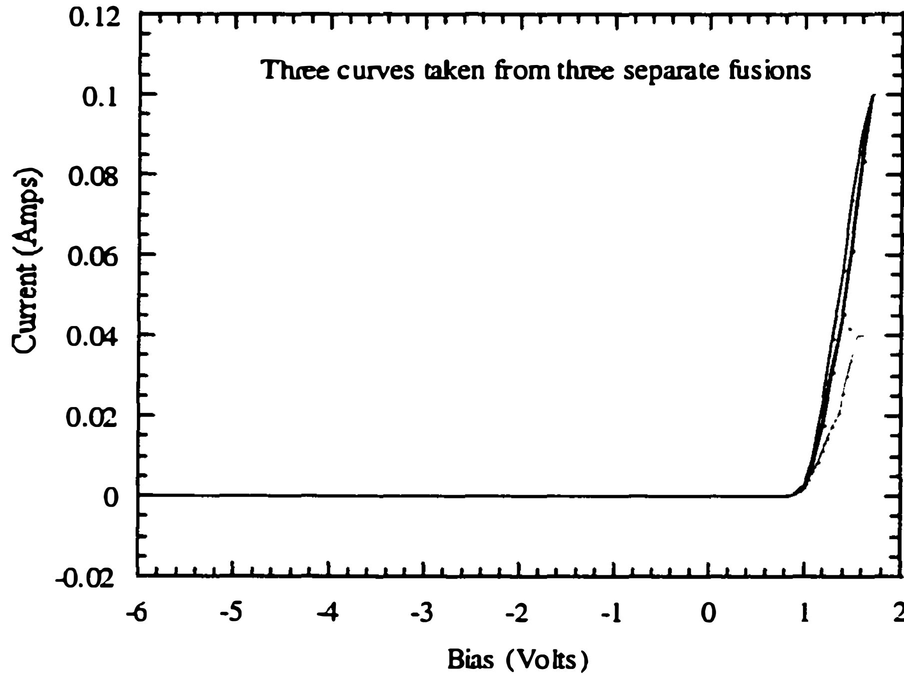


Figure 3.05 I-V characteristic from fusion with a dopant supplying InGaAsP layer 7.5 nm removed from the interface.

3.01.2 Thyristor type action at the p-p fused interface

Another feature notably absent from the I-V characteristic is the kink present in Figure 3.02. This kink is reminiscent of kinks that can be found in the characteristic curves of a npnp device known as a thyristor. Indeed, we believe the kink to be a result of n-type traps at the interface, forming a pnpn junction when an active region is fused to p material. In this way, the device structure is n/p/fused junction/p where the fused junction behaves as an n-type layer. Figure 3.06 shows a simulated fit to experimental data assuming an n-type trap density of $2\times10^{17}/cm^2$ situated at the fused interface. The program crashes at the exact point in our experimental data that the kink occurs, lending

credence to the thyristor theory. Further evidence of this is the absence of kinks in n-n fused junction I-V characteristics, where a thyristor type effect is no longer an issue. The effects of the kink are multifold and will be discussed in the section below.

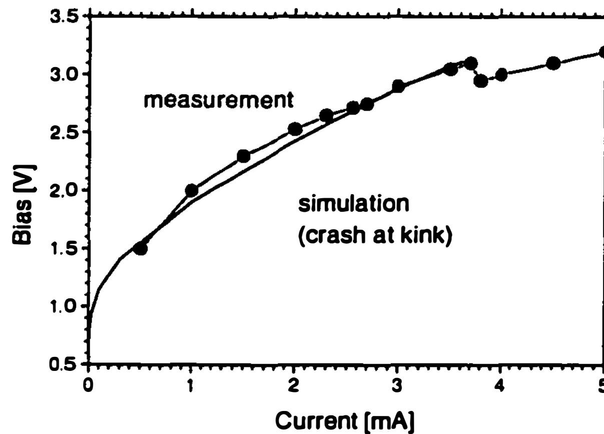


Figure 3.06 Measurement and simulation of kink in I-V due to the presence of n-type traps at the fused interface. Simulation by J. Piprek.

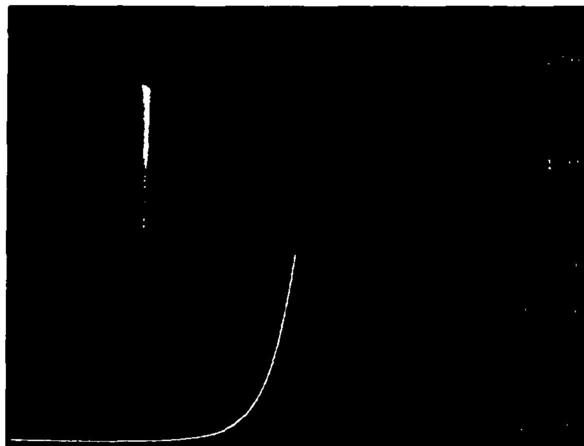


Figure 3.07. Curve tracer I-V characteristic in constant current mode showing a kink at 9mA with a magnitude of greater than 3V.

The kink exhibits hysterisis, both in constant current and voltage bias. A scanned image from a curve tracer is shown in Figure 3.07. A proposed

model ensues. The fused junction, an n-type layer sandwiched between two p-type regions of GaAs and InP, acts as a barrier to hole flow. Calculated band diagrams from an active region fused to a p-type mirror are shown in Figure 3.08 for both 0 mA and 3 mA applied bias.

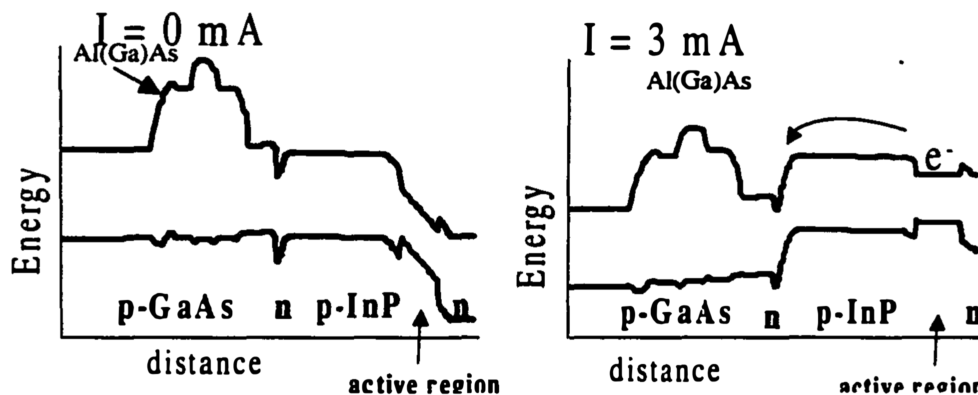


Figure 3.08 Calculated energy band diagrams for active region fused to a GaAs mirror period. N-type charge of the concentration $1.7(10)^{13}/cm^2$ is modeled at the interface. Calculation by J. Piprek.

Under forward bias, electrons are provided to the n-terminal on the n-side of the active region, and holes are provided to the GaAs substrate. There is an accumulation of positive charge at the fused interface due to n-type defects, posing a barrier to hole flow. At increasing bias, the fused junction begins to pass current and the active region diode is turned on. As the device is biased further above threshold, the bands bend, allowing electrons to leak out of the MQW active region towards the fused junction. Since there is no barrier to electron flow across the junction, the electrons may traverse the junction and recombine in the spacer layer. Figure 3.09 shows the optical luminescence spectrum from a double fused VCL in a wavelength region outside of both the gain spectrum and the optical pass band of the DBR. We see a developing luminescence peak at 980 nm. This luminescence peak may actually be at longer wavelength but is not detected due to the mirror stop band. At some

point, the resistance of the fused junction decreases, and any increase in applied bias is applied to the active region diode. The result is more leakage out to the active region, eventually leading to the creation of a shunt current path around the active region that is the kink in the I-V.

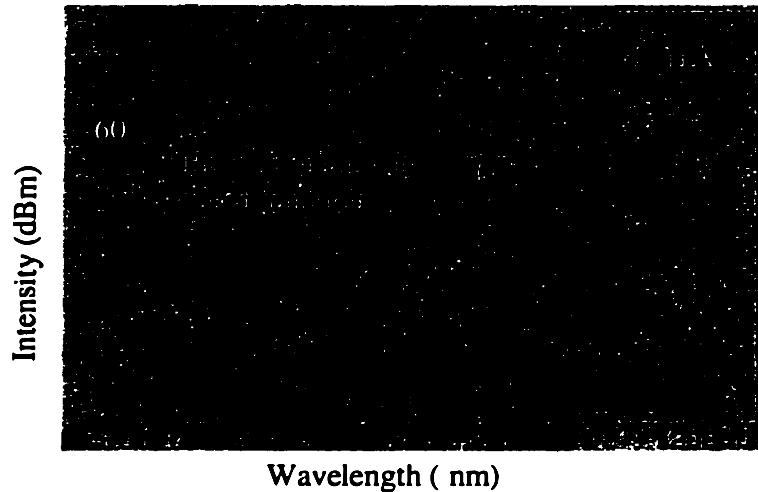


Figure 3.09 Optical spectrum from VCL biased at 8 mA. The peak at 950 nm may be attributed to recombination outside of the MQW active region. The intensity of this peak increases with applied bias, i.e. increases with additional leakage out of the active region.

The reason we see no kink in Figure 3.05 is that we have possibly supplied enough p-type dopant to the fused interface to compensate the n-type charge, eliminating the problems associated therewith. As indicated previously, however, the manifestations of the kink are many-fold. In many cases, multiple kinks plague the devices. Such behavior is indicative of capacitive charging and discharging. The kink also appears in the light-current relations and near field image of the lasing mode as will be discussed in Chapter 5. Clearly, a better understanding of the fused interface will contribute to a better understanding of the kink in our devices.

3.02 Optical Characterization of the Fused Interface

3.01.1 Low temperature Photoluminescence

In spite of evidence of organic contaminants, misfit dislocations, and higher than ideal voltage drops across the fused junctions, wafer fused technology has enabled the realization of high quality interfaces for optoelectronic design. In order to assess the extent over which the highly dislocated and contaminated interface impacts the optical quality of the surrounding material, multiple quantum well (MQW) photoluminescence (PL) studies have been performed. The premise of such experiments is simple; the MQW structure acts as a depth resolved probe to compare the luminescence efficiency of the material in the interface region before and after fusion.

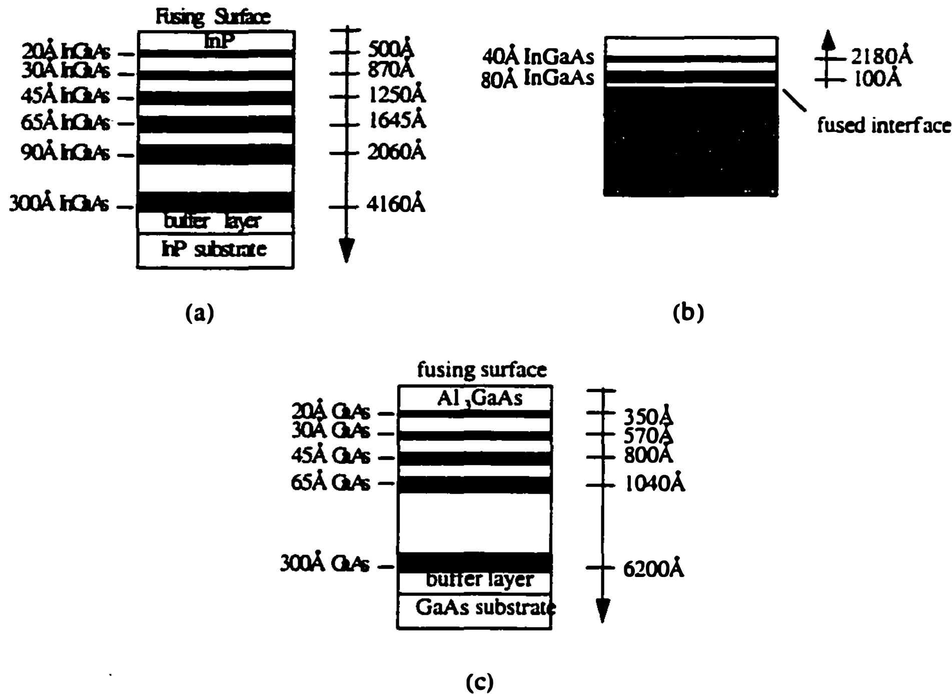


Figure 3.10 MQW structures for PL; excitation and luminescence detection taken from the top of all samples. (a) InP-based MQW structure consisting of In.53Ga.47As lattice matched wells with 300Å InP barriers. (b) InP-based strained layer sample. (c) GaAs-based MQW structure with 200Å Al.3Ga.7As barriers.

Lattice matched InP/InGaAs and AlGaAs/GaAs quantum wells of varying widths were strategically grown on InP and GaAs substrates by MOCVD and MBE, respectively, to probe the optical quality of the epilayer region before and after wafer fusion. The InP-based structures are shown in Figure 3.10 (a) and 3.10(b), and the GaAs structure in Figure 3.10(c). The GaAs structure was grown at 600°C whereas the InP-based structures were grown at 615°C. The order in which the quantum wells were grown was designed to allow photoluminescence (PL) studies to be performed on both the substrate material to which an epilayer is fused (Figure 3.10a), as well as on the thin, transferred epilayer (Figure 3.10b). In the MQW samples, reference

quantum wells were grown deep in each epilayer to facilitate accurate normalization of signal intensity. In all cases, care was taken to ensure that the luminescence from the wells would not be absorbed by the surrounding material before reaching the detector.

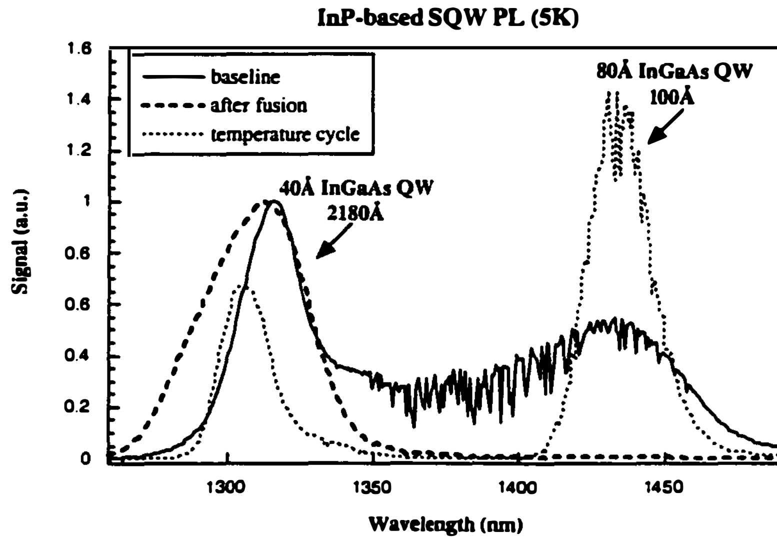


Figure 3.11 InP-based strained layer PL spectra. Markers indicate well thickness as well as distance from the fused interface in Angstroms. The three overlaid spectra provide a baseline spectra of an unfused sample for reference, fused spectra of a transferred film, and spectra of a thermally cycled sample.

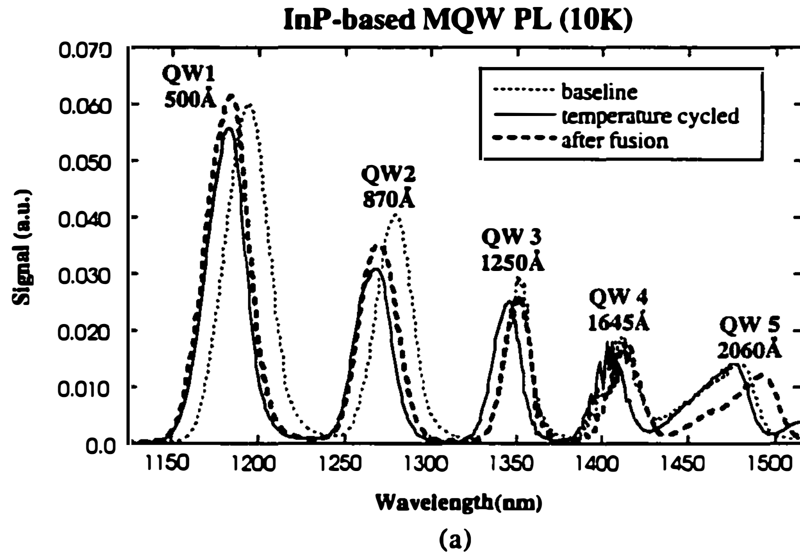
The surfaces of all epilayers were cleaned and passivated in methanol prior to fusion. Photoluminescence data was taken at 10K with a 514 nm Argon 5W laser at an optical power of 5 mW. Our analysis employs three photoluminescence data sets: (a) PL of the "as grown" material to provide a baseline, (b) after fusion and upon removal of either the substrate and etch-stop layer (for transferred films) or removal of both the substrate and transferred epilayer (for MQW samples receiving epilayers) by wet etching, and (c) after temperature cycling the "as grown" QW substrate under the fusing conditions

to decouple the effects of the thermal cycling employed in the fusion process with the effects of fusion itself. The thermally cycled samples were placed in the fusing fixture/furnace with a silicon cap to prevent surface degradation, and treated in a hydrogen ambient.

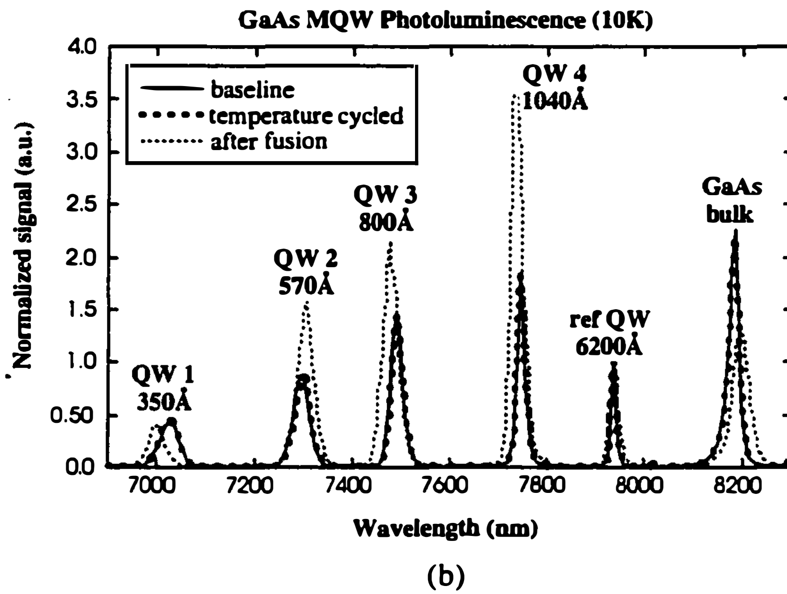
The InP-based single quantum well (SQW) structure was fused to an undoped GaAs substrate with a 500 nm epitaxial layer grown by MBE. Upon removal of both the InP substrate and stop-etch layer, PL was performed. The resulting PL spectra is shown in Figure 3.11. The PL spectra shows that whereas the luminescence from the quantum well 214 nm removed from the interface endures the fusion process, the luminescence from the well 10 nm away from the interface is degraded. The relative intensities of the 214 nm deep QW peaks before and after fusion cannot be compared since the spectra from the baseline and after fusion are taken with the incident excitation and subsequent luminescence collected from different sides of the QW structure (as is necessitated by substrate absorption). However, the increased PL signal intensity from the surface QW after temperature cycling as compared with the baseline is real, and indicates that thermal cycling alone does not degrade the luminescence, but can in fact improve it, perhaps by acting as a thermal anneal to drive out defects.

The InP MQW sample was fused to a 100 nm thick GaAs epilayer grown by MBE; the GaAs MQW sample was fused to a 300 nm thick InP epilayer grown by MOCVD. The resulting PL spectra are shown in Figure 3.12. Figure 3.12(a) shows the raw PL data taken on the InP MQW sample, including the baseline ("as grown"), the temperature cycled, and the fused spectra. Although we were unable to normalize the InP MQW spectra, as all peaks were affected by the fusion process, we clearly see no appreciable decrease in luminescence efficiency of the quantum wells as close as 50 nm from the fused interface. The same is true for the GaAs MQW structure as

seen in Figure 3.12(b). However, in this case, we were able to normalize to the reference peak and demonstrate what appears to be an increase in the luminescence efficiency of all the quantum wells, venturing as close as 35 nm to the fused interface. The increase in luminescence may result from gettering of defects during the fusion process, where the fused interface itself may provide a 'sink' for any defects present in the as grown epilayers. The integrity of the PL signal from quantum wells as close as 35 nm and 50 nm from the fused interface suggests that optically active regions can be placed in close proximity to the fused interface without suffering degradation of operation.



(a)



(b)

Figure 3.12 PL spectra from InP-based (a) and GaAs-based (b) MQW structures.

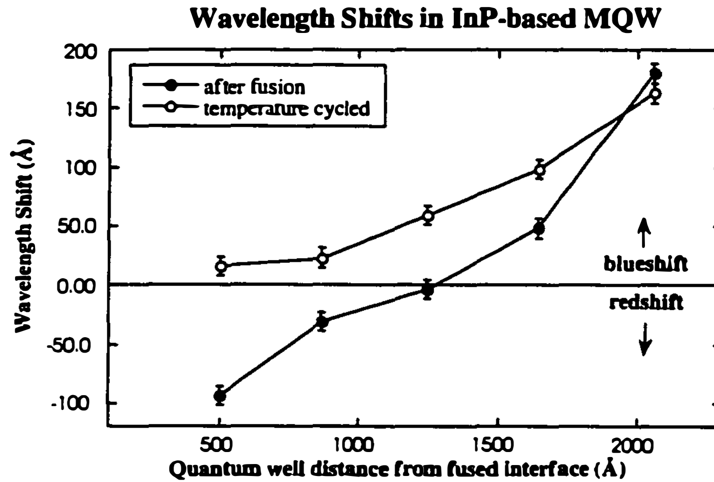


Figure 3.13 Peak wavelength shifts in the InP-based MQW structures. Shifts were measured relative to the baseline "as grown" structure. Open circles indicate shifts seen in the thermally-cycled piece; closed circles represent shifts in the fused piece after the transferred epilayer has been removed. Error bars were determined from MOCVD growth non-uniformity.

In addition to the peak intensity, the peak position of the MQW samples can provide information on the material changes effected during the fusion process. The peak wavelength shifts from the baseline for both the temperature cycled and fused GaAs samples are negligible (within error derived from MBE growth non-uniformity). However, there are notable shifts in the peak positions in the InP-based MQW, as detailed in Figure 3.13. The temperature-cycled sample displays a blue shift in all of the wells; the effect is increasingly pronounced as both the distance from the interface and thickness of the wells increases. Although the overall shift is of the same magnitude and nature at the deepest quantum well for both the thermally cycled and fused sample, QWs in the fused piece experience increasingly larger red-shifts with

proximity to the fused interface that counteract the blue-shifting seen in the temperature cycled spectrum.

Similar data have been reported elsewhere[8], and there is substantial literature available on diffusion/intermixing across quantum well boundaries[9]. In the well studied AlGaAs/GaAs system, diffusion of Al across the interface results in a more graded interface, a richer Al content in the quantum well region, and a consequent blue-shift in the peak position associated with the quantum well. The InGaAs/InP system presents an added degree of complexity, since diffusion of both the group III and group V elements is possible. In general, AlGaAs/GaAs quantum wells annealed under the same conditions are more stable to interdiffusion; one calculation has shown that the activation energy for interdiffusion to be more than twice that characteristic for InGaAs/InP heterostructures[10]. A number of previous studies have shown blue-shifts in thermally annealed multiple quantum well samples due to diffusion of P into the QW region[11]. Without further characterization of the nature of the QW interfaces and their compositional changes, we cannot give a definitive explanation of the variation of magnitudes of the shifts for different quantum wells. However, the following may have some bearing on the observed systematic increase in blue shift for QWs farther from the interface: Wong et al. have found that interdiffusion processes for the group V elements are related to point defect densities, which are in turn controlled by the nature of the substrates[12]. It is conceivable that defects in the substrate diffuse upwards into the epitaxial layers during the thermal cycling or the wafer fusion itself. In this regard, we note that the fusing temperature was larger than the growth temperature for all quantum well materials used. Those QWs closest to the substrate would be more sensitive to these point defects, displaying a larger P diffusion, and consequently a large blue-shift. Concomitantly, the creation of group III vacancies or defects at the

surface, even though capped, may provide a means of augmenting the group III interdiffusion. Indium diffusion into the quantum well, and consequent formation of an In-rich well would lead to an observed red-shift, whose magnitude would decrease with increasing distance from the interface.

This latter process is further augmented through the fusion process itself. It is believed that the crux of our fusing process depends on the rearrangement of material in the region of the interface, in particular, the indium; the actual evolution of material into pre-etched channels used in the fusing process supports this56. The redistribution of indium at the fused interface could subsequently enhance the diffusion of indium in the material closest to the interface, producing a red-shift in the QW PL spectrum that decreases with increasing distance form the interface. Indeed, this is consistent with the microscopy analysis presented in Chapter 2. There are of course many other factors, such as strain and doping that influence the diffusion constants of the group III and group V constituents involved in InP/InGaAs interdiffusion. The important results of these peak shift studies are that materials can be engineered to minimize either group III or group V diffusion in order to stabilize the critical peak positions during the fusing process.

The persistence of high intensity low temperature PL from quantum wells as close as 35 nm on the GaAs side and 50 nm on the InP side of the fused interface provides useful information for the design of device structures based on the wafer fusing process. Peak shifts observed in the more mobile InP-based materials represent the balance of diffusion processes producing blue-shifts and compensating processes leading to red-shifts. The proper understanding of the relative roles of those processes, and strategic engineering of substrate and quantum well composition can minimize the shifts observed. Low temperature PL is a sensitive probe of material quality that enables observations of subtle peak luminescence shifts that may otherwise be lost in

the broadened spectra characteristic of room temperature measurements. Actual devices, however, operate at room temperature and above, conditions under which the carrier diffusion lengths are considerably larger and may interact more with the fused interface.

3.01.2 Room Temperature Photoluminescence

A myriad of devices have been demonstrated using wafer fusion. Perhaps the most sensitive of these devices to the quality of the wafer fused interface are long wavelength vertical cavity lasers (VCL), as the wafer fused interface must at once be electrically conductive and optically transparent. Most importantly, the material being fused must be able to withstand the high temperature and pressure requirements of the fusion process itself. This section investigates the degradation of InP/InGaAsP multiple quantum well (MQW) laser active regions after fusion and demonstrates a superlattice defect blocking layer that improves the luminescence of the MQW active region through the fusion process.

In order to gage the effects of the fusion on actual devices, the luminescence properties of InP/InGaAsP multiple quantum well (MQW) laser active regions was investigated. Room temperature photoluminescence studies were performed on doped and undoped active regions before fusion, after fusion, after thermal cycling, and after rapid thermal annealing. We show that quantum well RT luminescence intensity degrades considerably after wafer fusion. The introduction of a superlattice defect blocking layer at the fusing surface of the MQW active region not only prevents degradation of the luminescence, but actually improves the luminescence of the MQW active region through the fusion process by a factor of four.

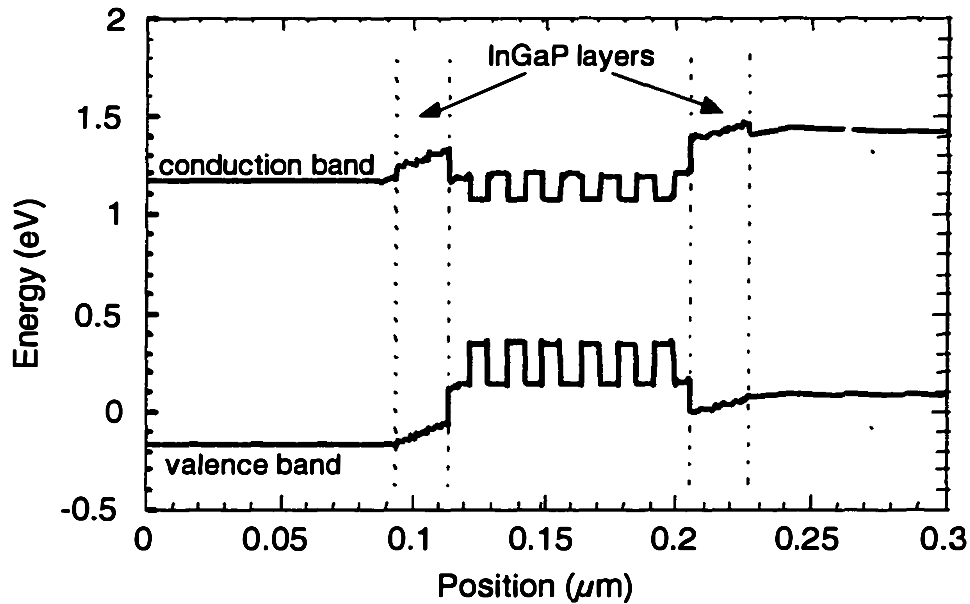


Figure 3.14 Calculated energy band diagram of active region comprised of six 7 nm QWs with 1% compressive strain. Two InGaP layers are designed into the cladding to increase the electron confinement in the active region by 30 meV and for modest strain compensation.

Three different MQW active regions were grown for this study; the energy band diagram is shown in Figure 3.14, and the fused structures are shown in Figure 3.15. Figure 3.15(a) shows the typical structure for a VCL active region grown by metal organic chemical vapor deposition (MOCVD) fused to a GaAs epilayer. The MQW region consists of six 7 nm thick 1% strain compensated InGaAsP QWs with seven 7.5 nm thick InGaAsP barriers. The emission wavelength of the barriers is 1180 nm. On either side of the active region is a strain compensating $In_{0.9}Ga_{0.1}P$ layer and a 300 nm InP cladding. The bottom cladding is n-doped with 10^{18} Si and the upper cladding is p-doped with 5×10^{17} Zn, set back from the QWs by 100 nm non-intentionally doped InP. Figure 3.15(b) shows the structure of an identical active region with a lattice matched InP/InGaAsP superlattice consisting of four repetitions

of a 7.5 nm InP/ 7.5nm InGaAsP period. This active region was grown both with the same doping profile as the typical active region and without intentional doping, to decouple the effects of Zn disordering of the active region and defect induced changes in the active region before and after fusing. Both structures were fused to Be-doped GaAs epilayers grown by molecular beam epitaxy (MBE). The InP substrates and InGaAs etch stop layers were removed by wet chemical etching.

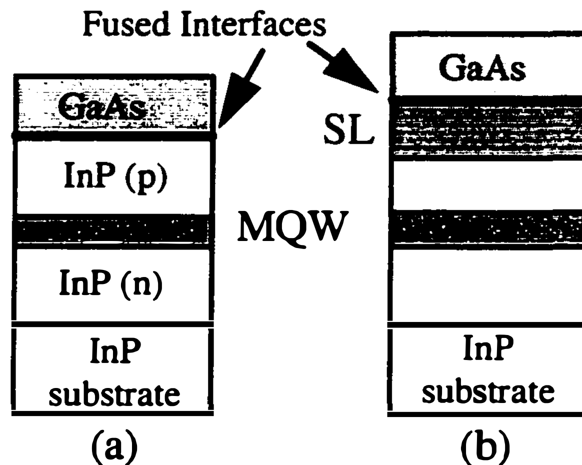


Figure 3.15: Structure of fused active regions. (a) typical active region, (b) active region with a superlattice barrier at the fused interface.

Photoluminescence data were taken at room temperature with a 780 nm diode laser pump. Our analysis employs four photoluminescence data sets: (a) PL of the "as grown" material to provide a baseline, (b) PL after fusion and upon removal of the substrate by wet etching, (c) PL after a rapid thermal anneal at 650°C for one minute, and (d) PL after temperature cycling the "as grown" active region at the fusing temperature. This allows us to decouple the effects of the thermal cycling employed in the fusion process from the effects of fusion itself. The thermally cycled samples were placed in the fusing

furnace with a GaAs cap to prevent surface degradation. Care was taken to prevent surface degradation during rapid thermal annealing by placing an InP cap over the surface of the samples.

The spectra from the regular active region fusion are shown in Figure 3.16. The PL signal from the MQWs is degraded by a factor of 10 upon fusion whereas the PL signal only degrades by a factor of 2 after thermal cycling. Therefore, it is not simply the elevated temperature of the fusing process that produces the degradation, but some additional process that occurs during the fusion itself. These results are readily explained through the following reasoning. Mass transport of material in the region of the interface, the indium in particular, is believed critical to fusion bonding. The evolution of material into pre-etched channels used in the fusing process supports this. Because the GaAs and InP surfaces are not perfectly flat, rearrangement of atoms at the two free surfaces during fusion is coupled with the generation of vacancies that may diffuse from the forming interface towards the active region. The application of pressure can also enhance the diffusivity of both dopants and defects in materials, further degrading the luminescence properties of the MQWs after fusion.

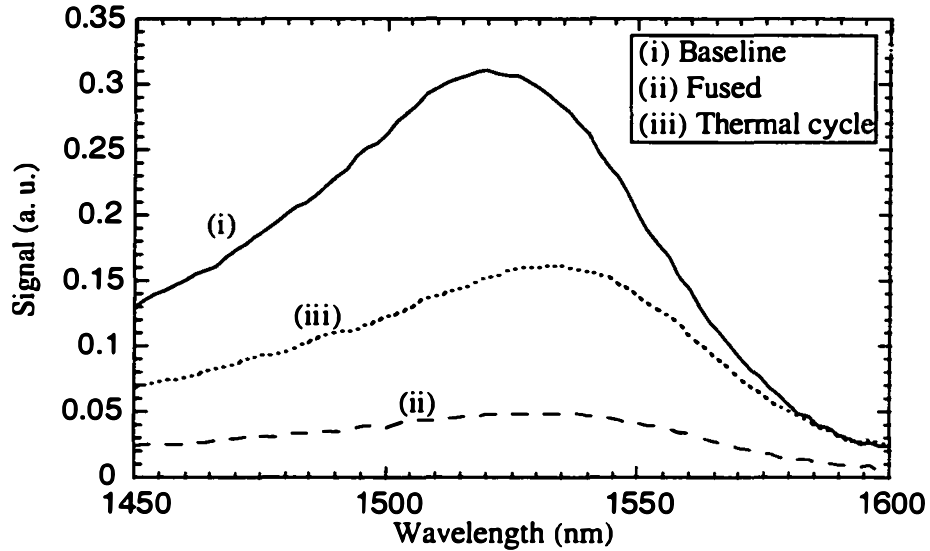


Figure 3.16 PL spectra from the original active region.

The addition of a superlattice barrier to the MQW active region provides a dramatic improvement in the photoluminescence characteristics, *even in comparison to the baseline measurements.* These results are summarized in Figure 3.17. Figure 3.17(a) shows the photoluminescence spectra from the non-intentionally doped superlattice sample; Figure 3.17(b) shows the spectra from the doped superlattice study. In dramatic contrast to the results obtained for the regular active region, the interposition of a superlattice results in a factor of 2 improvement in the after-fusion PL for the undoped case, and in a factor of 4 for the doped case. The superlattice is proposed to act as a defect-blocking layer, preventing the deeper propagation of defects formed through the fusing process.

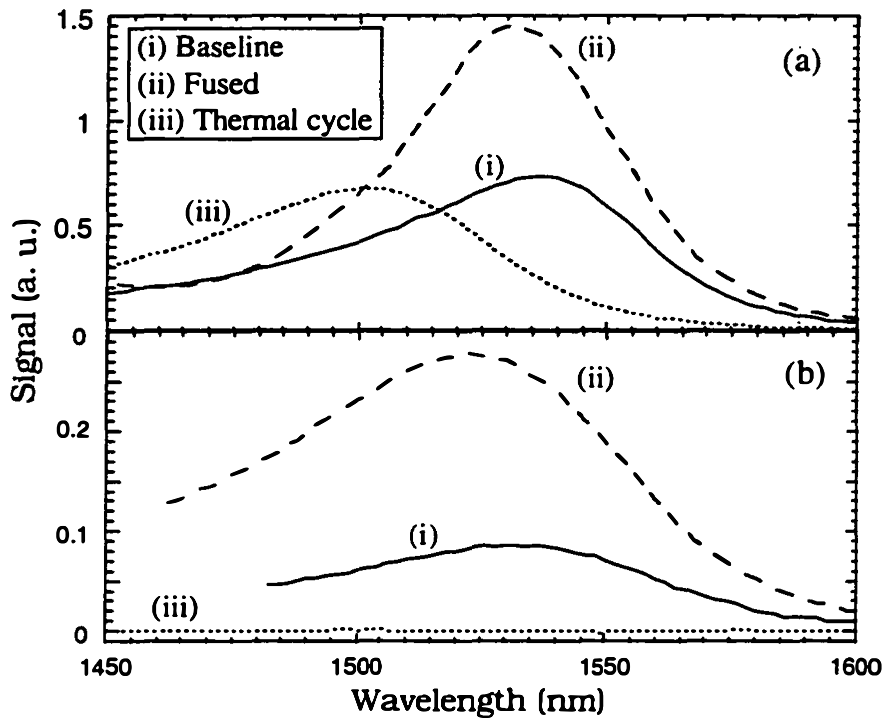


Figure 3.17 (a) PL spectra from the non-intentionally doped superlattice sample. (b) PL spectra from the doped superlattice sample.

The increase in PL signal after fusion can be explained by a combination of processes. There have been numerous demonstrations that a superlattice has the ability to block the propagation of defects from a 'source' to a critical active layer. Superlattices have been used as a buffer layer in crystal growth, preventing the migration of defects from the bulk into the epilayers[13]. This can account for the fact that the active layer PL signal is *not degraded* after the fusion process. However, the PL is actually *enhanced* after fusion, and this may result from the fused interface itself, in conjunction with the superlattice barrier.

Again, there is a dramatic difference in the PL spectra for samples that are simply thermally cycled, compared to those samples that are fused. In this case, with the superlattice barriers, the fused samples are substantially better than those that are only given the thermal treatment. In the case of the doped samples, the thermal cycling completely obliterates the MQW peak. This is shown in Figure 3.18, demonstrating the effect of a rapid thermal anneal on the doped superlattice sample. The un-annealed sample shows good photoluminescence both from the strained MQW region as well as from the lattice matched superlattice. Upon annealing, however, the PL from the superlattice remains intact whereas the PL signal from the MQW region is completely obliterated. Thermal cycling has the same effect. The effects of Zn diffusion through QWs are well established to be detrimental to the optical integrity of the material.[9] Defects, with elevated diffusion constants brought about by higher temperature processing, would be most readily accommodated by strained interfaces. In the purely thermal process, the strained interfaces of the MQW region provide the most favorable sink for defects and dopant aggregation, with a consequent reduction in the MQW PL.

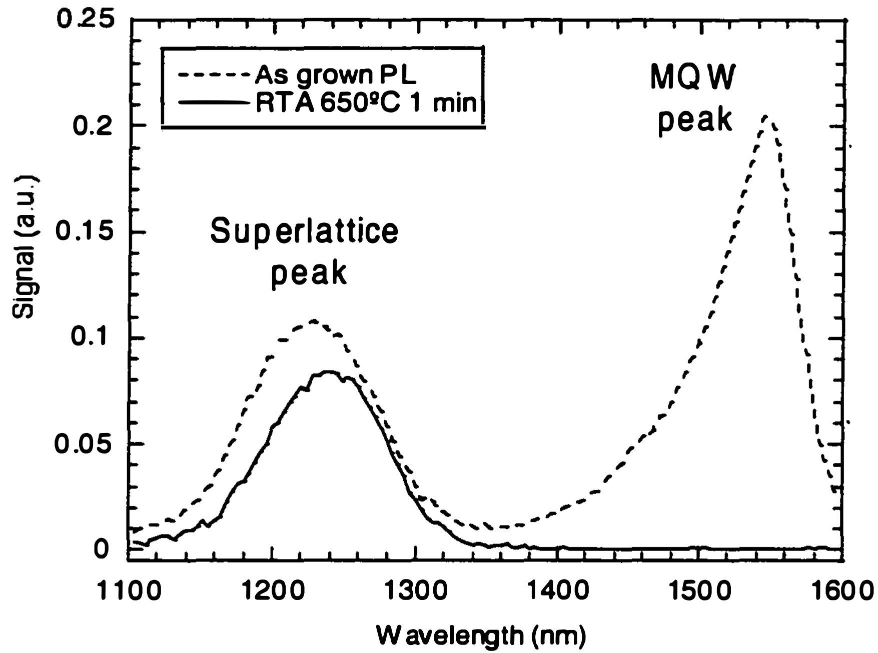


Figure 3.18 PL spectra from doped superlattice sample before and after rapid thermal annealing at 650°C for 1 minute.

However, when the same samples are fused, the fused interface itself may serve as a gettering site for defects, in 'competition' with the strained MQW region. By diverting defects from the critical active area, the fused interface assists in the improved luminescence from that area.

The high temperatures and pressures that characterize the wafer fusion process can have a deleterious consequence on the quality of materials and interfaces in close proximity to the fused junction. The Zn doped InP/InGaAsP system is especially sensitive to high temperature treatment. We have demonstrated the successful introduction of a superlattice defect blocking layer that when coupled with the gettering ability of the fused junction improves the luminescence of MQWs after fusion.

3.03 Summary

This chapter attempts to relate the understanding developed in Chapter 2 pertaining to the structure and chemistry of the wafer fused interface to the electrical and optical characteristics essential to device performance and design. In particular, the electrical characteristics of the p-p interface were analyzed. A large voltage drop across the fused interface was attributed to the structure and chemistry of the fusion mechanism- inherent to our normal fusion procedure. A remedy to this problem was proposed in the form of a dopant supplying layer slightly removed from the fused junction. However, the optical loss associated with this layer has not yet been addressed. The kink at the interface was revealed in a simplistic model to be similar to thyristor type action, resulting from the n-type charge situated at the fused interface. However, it was noted that the kink is much more complex than this simple model can reflect.

The optical integrity of material adjacent to the interface was studies using low and room temperature photoluminescence. It was shown that the InP based material is more susceptible to the harsh fusion conditions. Despite this, QWs as close as 50 nm to the fused interface showed little degradation in LT-PL upon fusion. Room temperature PL studies demonstrated a minimum factor of 2 degradation of strained MQW luminescence upon fusion. However, after the introduction of a mitigating defect gettering superlattice at the active region fusion surface, an *improvement* in the MQW luminescence was demonstrated after fusion. For the first time, the fusion process can be thought of as an annealing process as opposed to a degrading process to all materials on hand. Building upon this understanding of the fusion mechanism

and its effects on the resultant device, Chapter 4 attempts to better integrate the fusion process into both device design and fabrication development.

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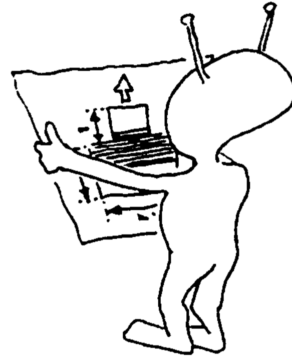


Chapter 4

LW-VCSELs: Device Design

The history of long wavelength VCSEL research at UCSB has spanned the past 6 years. Jim Dudley reported the first single fused 1.3 μm VCL in 1994[1]. Dubravko Babic demonstrated the first room temperature continuous wave (cw) operation of a 1.55 μm VCL in 1995[2]. Shortly thereafter, Near Margalit demonstrated high temperature cw operation of LW VCSELs in many successive device runs, owing his success to many improvements in device design[3]. Specifically, Margalit adopted the double fused etched pillar design of Babic and introduced the oxide aperture for current confinement. He placed the aperture at a null in the standing wave to minimize optical diffraction loss. He then re-designed the top p-mirror to minimize the penetration depth of the optical field and the loss associated therewith by using Al_9Ga_1As/GaAs carbon doped mirrors with low doping in the layers closest to the active region. Additionally, he optimized the band structure of the mirrors for low resistance to hole flow. Finally, he developed a top emitting structure with a single intra-cavity contact such that diffraction loss and absorption through the n-doped substrate was obliterated.

This work in this thesis includes the design, fabrication, and analysis of three different structural VCSEL designs. The devices fabricated in this thesis leverage much of the basic epilayer design off the structure of Margalit. However, the performance of the VCSELs as Margalit left them did not meet industry specifications for commercial application. At this point, the device and epilayer design had just about been optimized. It is at this point that the technology that enabled these devices also became their greatest limitation: the fused junction.

This thesis attempts to look at the fused junction and fusion process in great detail in order to both improve the device design and performance. In addition to optimization of the fusion process and small changes in the DBR design, two major additions to the device design were made. The first attempts to incorporate a defect blocking superlattice at the fused interface to improve the gain of the active material, as discussed in the previous chapter. The second is the development and incorporation of selective area fusion into the device design. Selective area fusion enables a new method of both current and carrier confinement in VCSELs, very similar in benefits to buried heterostructure designs. This chapter presents the most basic VCL theory necessary to understand the considerations in epilayer and device design. For an excellent background in laser theory and practical device analysis, the reader is referred to the PhD theses of Babic[4] and Corzine, and Diode Lasers and Photonic Integrated Circuits, by Coldren and Corzine[5]. An overview of the design considerations specific to the epilayers used for the devices fabricated in this thesis will be given, but the primary focus of this chapter is the design improvements afforded by the fusion process itself. For more detailed discussion of the evolution of the other existing design choices, the reader is referred to the dissertations of Babic[6] and Margalit[7], as well as references[8, 9].

The design of epilayers for devices must take both the transverse (1D) as well as the lateral (2D) structure of the device into account. This chapter begins with an overview of the optical cavity design in Section 4.01. Section 4.02 will briefly overview the electrical, and hence thermal considerations of epilayer design. A delicate balance exists between the optimal optical and electrical designs of the VCSEL. Because of the thermal and power conversion efficiency issues involved, the electrical resistance of the device (specifically the mirrors and fused junctions) must be minimized. Minimization of mirror resistance involves both the doping and grading of the epilayer structures for ease of hole flow. This oftentimes compromises the optimal optical cavity design because of free carrier absorption associated with doping, and reduced mirror reflectivities resulting from the graded index interfaces. Section 4.03 introduces the reader to the specific epitaxial structures designed in this thesis, and Section 4.04 overviews the final device structures to be analysed in Chapter 6.

4.01 The optical cavity

4.01.1 Background for round trip gain and loss estimation

The first consideration in VCSEL design is the optical path length of the mode, and the loss and gain that mode encounters. Specific to VCL design is the fact that the overlap of the mode with the gain region is extremely small. The condition for lasing is simple: the round trip modal gain must balance the round trip loss before any additional gain provided would indefinitely increase the power in the optical mode. Because of the small interaction of the gain region with the optical mode, the losses must be correspondingly small. However, the mode can experience loss at any point in the optical cavity. The losses can be broadly broken down into transmissive loss, T, (power emitted in

the lasing mode), and all other loss, L, including absorptive, diffractive, and scattering losses. The transmission loss is equal to (1-R) where R is the reflectivity of the mirrors. This places a constraint on the minimum acceptable reflectivity of the mirrors to be largely in excess of 99%. Again, in simple formalism, gain must equal loss:

$$G = L_{total} = T + L = (1-R) + L \tag{4.1}$$

Considering the travelling wave picture of the VCL, gain and loss add exponentially *per pass* in the cavity:

$$\begin{aligned} P &= P_0 \exp(gl) \\ P &= P_0 \exp\left(-\alpha_{mirror1} \cdot l_{pen1} - \alpha_{mirror2} \cdot l_{pen2} - \alpha_{active} \cdot l_{interaction}\right) \end{aligned} \tag{4.2}$$

where P is the final power, P_o is the initial power, g is the gain, α is the loss and l is the length of interaction. Oftentimes it is useful to consider the single pass or round trip gain and loss in a structure. The effect of the cavity (two mirrors plus a gain region) on the forward and backward travelling electromagnetic waves is the formation of a standing wave resulting from constructive and deconstructive interference. The period of the standing wave is $\lambda/2n$, where λ is the wavelength of light and n is the refractive index of the material. The power is proportional to the square of the electromagnetic field; the power in the standing wave peak is double that in the case of incoherent interaction. Because gain and loss are proportional to power, the interaction of gain or loss for a given layer must be multiplied by the standing wave factor in the region of interaction. The standing wave factor is also called the gain enhancement factor. Similarly, for loss placed at or near a null in the standing wave, there is a loss reduction factor. The gain enhancement factor is calculated for a length of material that interacts with the standing wave by integrating the field strength over that length and dividing by the length of the material. This average value is called the gain enhancement factor, denoted as ξ. The formalism is given in the following equation:

$$\xi = \frac{2}{\ell}\int_{x_o-\ell/2}^{x_o-\ell/2} Cos\left[\frac{2\pi n}{\lambda}x\right]^2 dx \qquad (4.3)$$

The integral has an analytical solution expressed as:

$$\xi = \frac{Sin\left[\frac{2\pi n}{\lambda}(l+2x_o)\right] + Sin\left[\frac{2\pi n}{\lambda}(l-2x_o)\right]}{2\pi nl/\lambda} \qquad (4.4)$$

The gain enhancement and loss reduction factors become significant when growth error forces the quantum wells out of the standing wave peak and forces lossy regions such as the fused interface out of the standing wave null. Using these factors, the gain and loss can be approximated by:

$$\begin{aligned} G &\approx 2\varsigma gl = 2\varsigma n_w d_w \\ L &\approx 2\varsigma_{loss}\alpha l_{tot} \end{aligned} \qquad (4.5)$$

where ξ and ξ_{loss} the calculated gain and loss enhancement factors, respectively, g is the material gain, α is the loss, n_w is the number of wells, and d_w is the well thickness. For many wells, the average enhancement factor over all the wells can be used. For our structures this number is typically 1.76.

The broad area loss can be estimated using the above equations, with a correct knowledge of the penetration depth of the optical field into the mirrors and active region. The penetration depth into the mirrors is dependent upon both the index difference between the high and low index materials, and the grading at the interface between the two constituent materials. For high reflectivity mirrors, the penetration depth is approximately:

$$l_{penetration} = \left(\frac{\lambda_o}{4\Delta n}\right) \qquad (4.6)$$

where Δn is the index difference between the materials. The penetration depth is increased for non-abrupt interfaces. It will become apparent in the next section that this trade-off between reduction in penetration depth and graded interfaces for better current conduction is necessary.

The high index contrast afforded by the GaAs/AlAs system results in a reduced penetration depth that can result in reduced diffraction loss because of the shorter effective cavity. Another advantage of high-contrast mirrors is that they have a larger optical bandwidth over which they have high reflectivity. This allows for reduced growth tolerances to achieve high reflectivity; however, this does not reduce the growth tolerance for the lasing mode position. Quarter-wave stacks have a different phase of reflection at different wavelengths. The lasing mode is greatly affected by the center mirror wavelength. The amount the mirrors affect the final lasing wavelength is directly proportional to their phase penetration depths. The percentage error in the final lasing wavelength is simply the weighted average of the percentage growth error in each mirror and the active region:

$$\lambda_{lase} = \frac{\Delta\lambda_{m1} \times L_{m1} + \Delta\lambda_{m2} \times L_{m2} + \Delta\lambda_c \times L_c}{L_{m1} + L_{m2} + L_c} \tag{4.7}$$

The penetration depths of each mirror is three times larger than the active region cavity length; the error in the final cavity mode is more determined by the growth error in the mirrors than the active region cavity.

Much work has been done to extract accurate values for absorptive losses in GaAs and InP at the wavelengths of interest for VCSELs. A table of these loss values in cm^{-1} per 10^{18} cm^{-3} doping is given in Table 4.1.

Table 4.1 Absorptive losses per $10^{18} cm^{3}$ doping.

Material	980 nm	1550 nm
p-InP	---	15 cm^{-1}
n-InP	---	5 cm^{-1}
p-GaAs	10 cm^{-1}	25 cm^{-1}
n-GaAs	5 cm^{-1}	6 cm^{-1}

Clearly, the absorptive losses are higher at longer wavelengths, and a more important consideration in the p-type material.

In order to estimate the actual round trip gain and loss in the VCSELs fabricated in this thesis, it is useful to understand the relation of external efficiency to transmission and loss in the structure. This relationship is given as

$$\eta_d(d) = \eta_i \frac{T}{T + L_{broadarea} + L(d)} \tag{4.8}$$

where η_d is the external efficiency, η_i is the injection efficiency, T is the transmission, $L_{broad\ area}$ is the broad area loss, and L(d) the size dependent optical loss. Knowledge of the LIV characteristics versus device size lead to an estimate of size dependent scattering and diffractive loss experienced by the mode.

4.01.2 Design of the active region

The typical design standard for a 980 nm or 850 nm VCSEL is either a one or one half lambda cavity. For fused VCSELs, we typically choose a $3/2\lambda$ cavity to remove the MQW active region from the epilayer area most affected by the fusion process. This is especially important when using strained quantum wells for reduced Auger recombination; the strain between the wells and their barriers make it energetically favorable for interdiffusion to occur. We have shown in Chapter 3 that this interdiffusion is enhanced with proximity to the fusing surface.

A calculated energy band diagram of a typical active region used for the devices fabricated in this thesis is shown in Figure 4.01. The active region incorporates two InGaP barrier layers on either side of the multiple quantum well region. The MQW region consists of six 7 nm 1%-strained quantum wells (QWs) with seven 7 nm thick barriers. The emission wavelength of the barriers is 1180 nm. On either side of the MQW region is a strain compensating $In_{0.9}Ga_{0.1}P$ layer and a 300 nm InP cladding. The InGaP barriers

serve both to slightly compensate the compressive strain in the QWs and increase the confinement energy of the electrons in the active region by 30meV relative to InP. Considering a simple thermionic emission model this confinement energy increase can decrease the current leakage out of the active region by a factor of 3 at elevated temperatures (~50°C)[10].

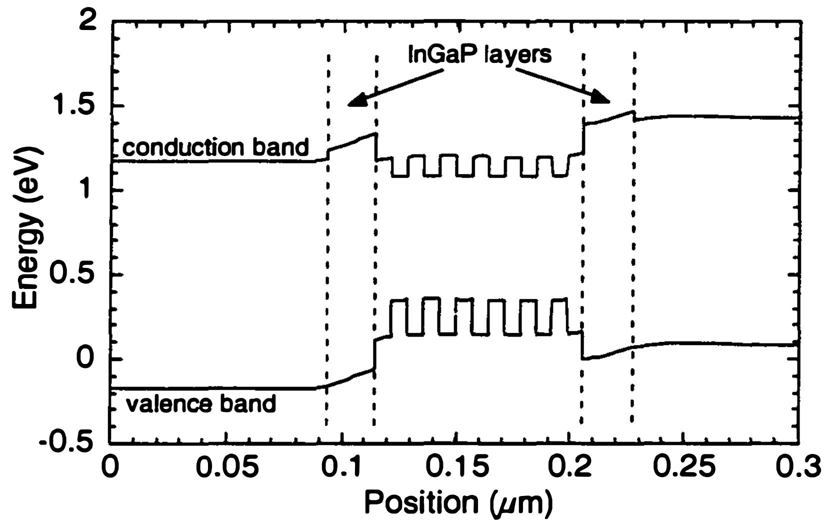


Figure4.01 Calculated energy band diagram of active region comprised of six 7 nm QWs with 1% compressive strain. Two InGaP layers are designed into the cladding to increase the electron confinement in the active region by 30meV and for modest strain compensation.

Placing this active region in a 3/2λ cavity produces the axial standing wave profile shown in Figure 4.02. This Figure was calculated using Vertical, a program that uses a 1-D transmission matrix method[11]. The MQW region is centered in the cavity at a standing wave peak. The fused junctions are placed at the second nulls as the first null in the cavity is a mere 500Å from the QWs. The oxide aperture is placed close to the third null in the standing wave to minimize diffraction loss, yet not exactly on a null to provide a modest

index perturbation of $\Delta n = 0.02$ for index guiding. The distance between the first QW and the oxide aperture is approximately 458 nm which when compared to the shorter wavelength systems is a large distance between the current confining aperture and the active region. In the all epitaxial 850 nm and 980 nm GaAs based VCSELs, the oxide aperture is places as close as 30 nm from the QWs.

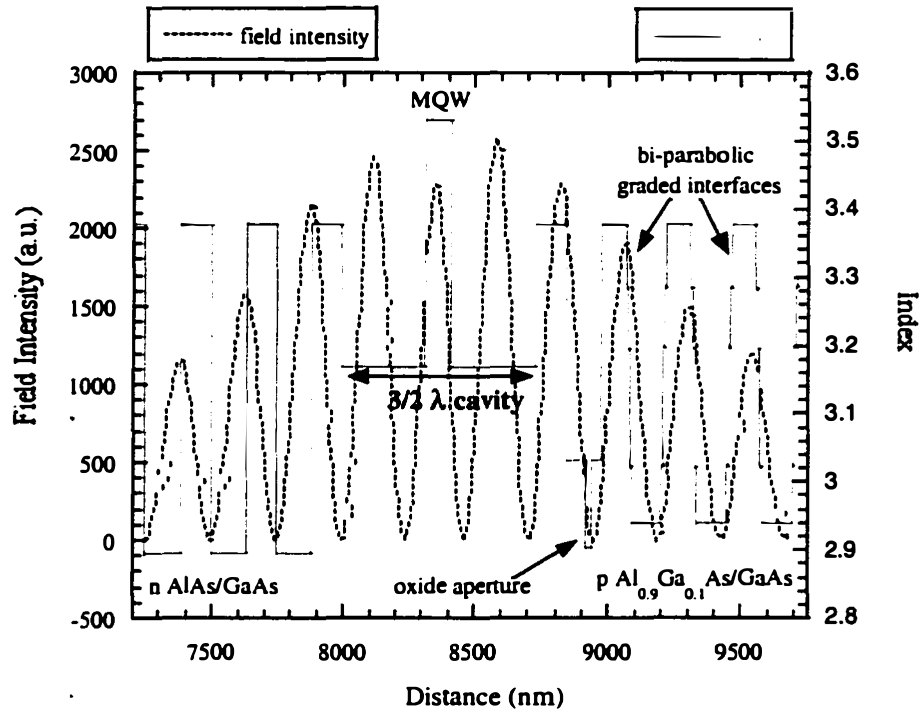


Figure 4.02 Calculated 1D standing wave and cavity index profile. (Vertical)

4.01.3 Design of the mirrors

The reflectivity of a quarter wave DBR stack is largely determined by the index contrast between the layers. The peak reflectivity of a quarter wave stack is given by the relations:

$$R = \left(\frac{1 - qap^{m-1}}{1 + qap^{m-1}} \right)^2 \qquad q = \frac{n_i}{n_H} : p = \frac{n_L}{n_H} ; a = \frac{n_e}{n_H} \qquad (4.9)$$

where n_i is the refractive index of the incident medium, n_H is the refractive index of the high index material, n_L is the refractive index of the low-index material, n_e is the refractive index of the exiting material, and m is the number of epitaxial layers. The formula assumes that all the interfaces are phase matched. As the index difference between the two materials is decreased, through reduced Al concentration, larger numbers of periods are needed to achieve the same reflectivity.

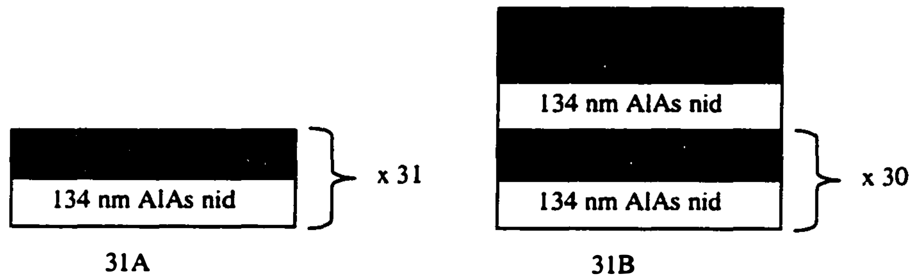


Figure4.03 Schematics of nid mirrors.

Since index is proportional to band gap, alternating GaAs and AlAs layers provide the largest index step in the AlGaAs system. However, there are many more considerations when choosing the material composition of the mirrors. Namely, along with high index contrast comes a large band offset, detrimental to series resistance of the structure. The p-type mobility in the AlGaAs system is low. Doping levels and proper gradients between the layers therefore become important. Another consideration is the ability to grow high quality materials of a given doping and concentration. For instance, the addition of solid source carbon to the MBE growth systems on campus allowed

for the incorporation of 90% AlGaAs layers alternating with GaAs as opposed to the former limitation of 67% AlGaAs. This limitation was imposed because higher composition Al compounds were difficult to dope with the existing Be source. However, initial growths incorporating solid source carbon doping were very rough. During the time span of this thesis, the Coldren group vastly improved the surface quality of the solid source carbon doped material, and also installed gas source carbon to one of the machines. Gas source carbon is able to achieve very high doping levels that the solid source carbon was unable to achieve while maintaining proper surface quality. The trade-off is the inability to dope layers with low doping concentration. These trade-offs will have a serious impact on the devices fabricated in this thesis.

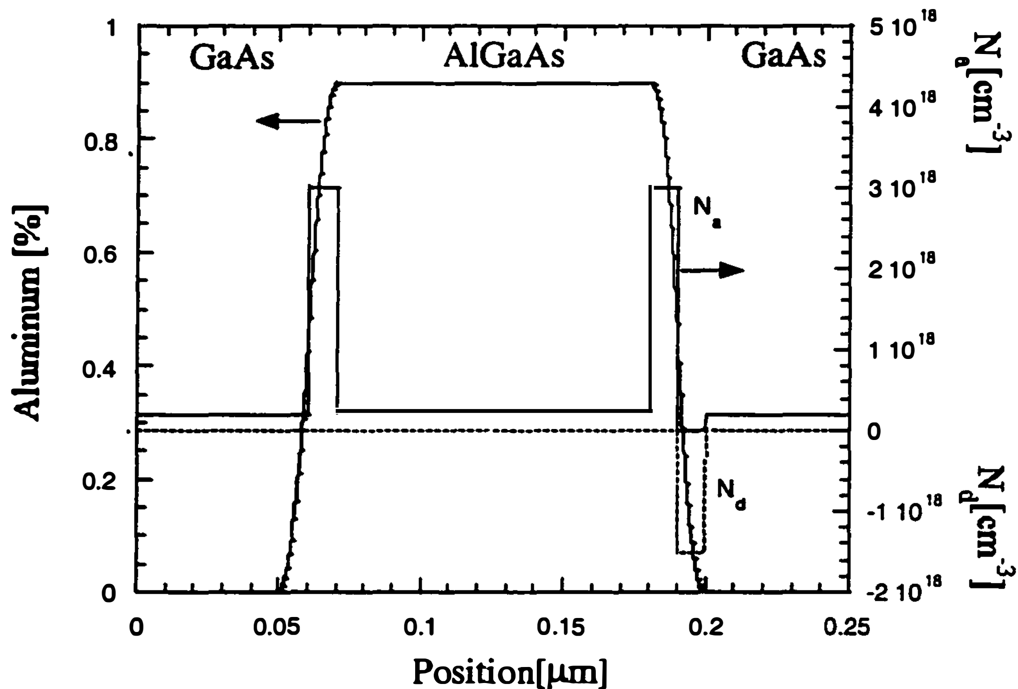


Figure 4.04. Schematic of double parabolic doping grade and doping levels in the bulk of the layer (2.7(10)17/cm3) and at the interfaces.

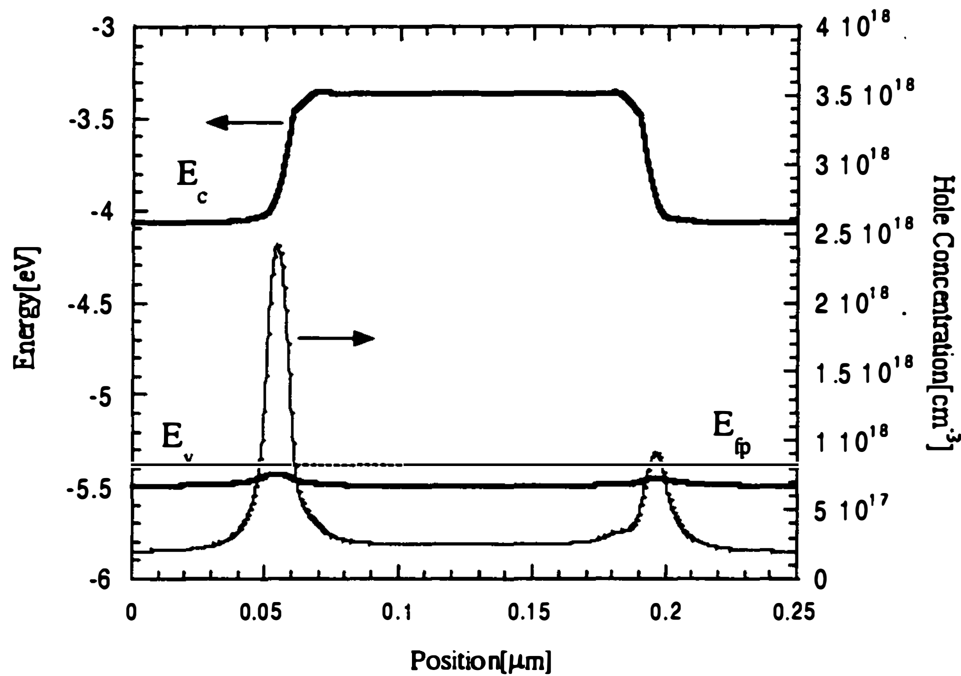


Figure 4.05 Calculated energy band diagram and hole concentration for mirror design of Figure 4.04.

Three p-mirrors and two unintentionally doped mirrors were designed and used for the devices fabricated in this thesis. All devices fabricated were top emitting, with high reflectivity unintentionally doped bottom mirrors. The bottom mirror consisted of 31 periods of AlAs/GaAs yielding a peak reflectivity at 99.99%. Schematics of structures 31A and 31B are shown in Figure 4.03. The only difference between the two growths is that the top 100Å of the top GaAs layer in 31B is n-doped at a doping concentration of $5(10)^{18}/cm^3$. The doping in this layer is to reduce the resistance of the n-intra-cavity contact that will be discussed later in this chapter.

As is indicated in Table 4.1, the absorptive losses in the p-mirror are perhaps the most important to control. Contrary to shorter wavelength VCSEL design, the doping in the layers must be kept to an absolute minimum. Of the

three p-mirrors designed for this thesis, 25.5A and 25.5B were grown using solid source carbon doping and 24.5C was grown using gas source carbon. The number of mirror periods in each respective growth is indicated before the letter (A, B, or C). Much work has been done on the grading of AlGaAs/GaAs interfaces for minimum resistance. We have chosen a bi-parabolic grade over 27 nm from GaAs to $Al_{.9}Ga_{.1}As$. The doping in the first seven mirror periods closest to the active region is nominally $2.5(10)^{17}/cm^3$ for structures A and B, and $4(10)^{17}/cm^3$ in structure C. The doping at the interfaces is much higher ($3(10)^{18}/cm^3$) to reduce the barriers to hole flow that come about as a result of the valence band offset in this materials system. A schematic of the compositional grade as well as the doping profile in the low doping layers (first 7 periods) is shown in Figure4.04. In contrast, the highly doped layers have nominal doping of $8(10)^{17}/cm^3$ in the AlGaAs layers, and $4(10)^{17}/cm^3$ in the GaAs layers. The reason for the different doping levels requested is that the AlGaAs is more difficult to dope, and consistently results in a factor of two lower doping in the layer. Usually this is accounted for by the grower, but it does not hurt to incorporate such measures in the design of the epilayer itself. A calculated energy band diagram and corresponding spatial hole concentration according to the doping specifications detailed above is shown in Figure 4.05. More doping is placed at the interfaces situated at a standing wave null as associated the free carrier absorption loss is minimal due to the weak interaction with the optical field.

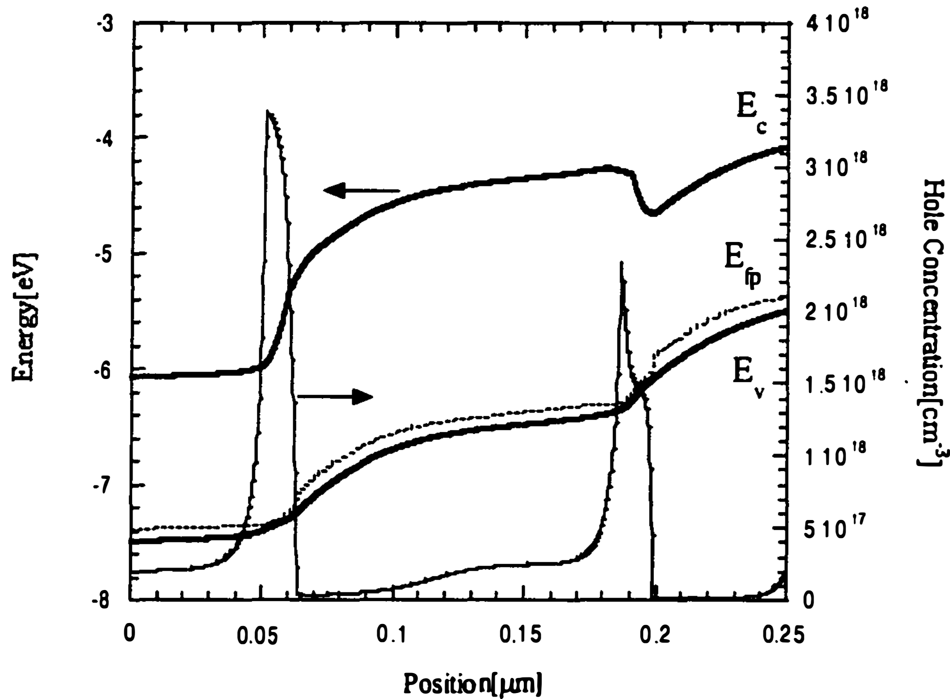


Figure 4.06 Calculated energy band diagram and hole concentration under 2V applied bias.

The preceding device design has been analyzed under static conditions. It is interesting to look at the properties of the specified structure under bias. Figure 4.06 is the corresponding energy band diagram and hole concentration under 2V applied bias. It is clear that there will be more absorptive loss under non steady state conditions. Once again, to find the loss associated with the large pile up of holes in the system, one simply must multiply the hole concentration at a given point by the standing wave factor assuming a loss of 25 cm^{-1} per 10^{18} free carriers.

Other differences in doping profiles between the mirror sets have to do with the contact layer (top-p contact) and the fusion layer. Previous studies have deemed it necessary to highly dope the fusion surfaces, in an attempt to

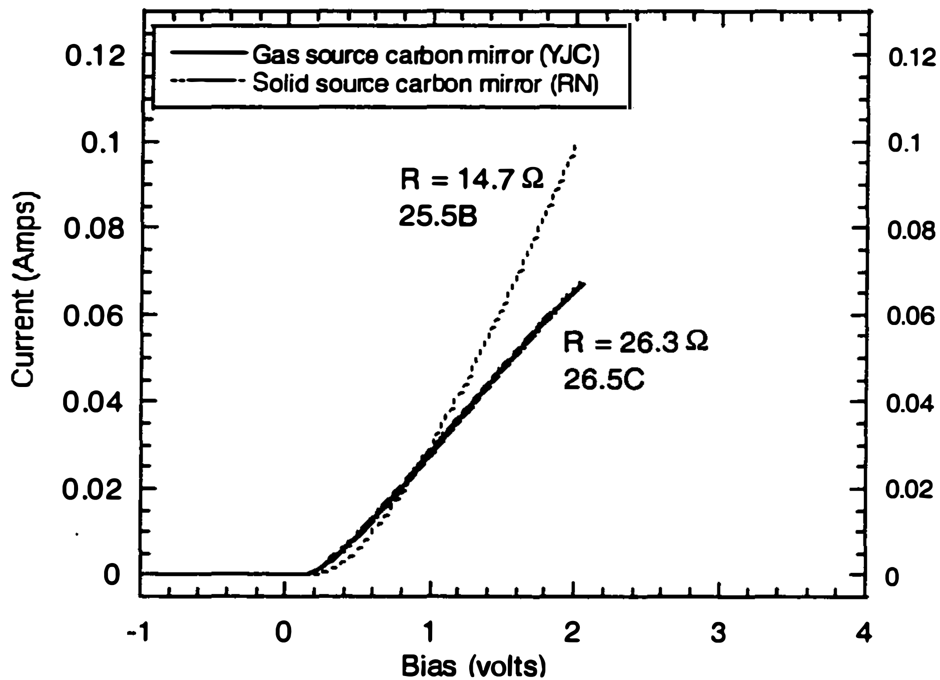


Figure4.07 I-V characteristic of mirrors 25.5B and 26.5C.

compensate the n-type charge that inevitably ends up at the interface. It is this charge that leads to the kink in the I-V that we are calling a thyristor effect. To compensate the n-type charge at the interface, we have tried to highly p-dope the fusion surface. Because it was difficult to achieve high doping densities using solid source carbon, we were forced to re-grow a beryllium cap on the surface of the mirror. This cap has a doping density of $5(10)^{18}/cm^3$ over 30 nm in sample 25.5A. Sample 25.5B was re-grown with gas source carbon in a 10 nm linear grade from $3(10)^{17}/cm^3$ to $1(10)^{19}/cm^3$ at the surface. In the gas source fusion structure, 26.5C, the entire sample was grown with gas source carbon, so the problem was not control of highly doped layers, rather the low doped layers. This structure had a 30 nm fusion layer with doping of $1(10)^{19}/cm^3$. A summary of all mirror properties is given in Table 4.2.

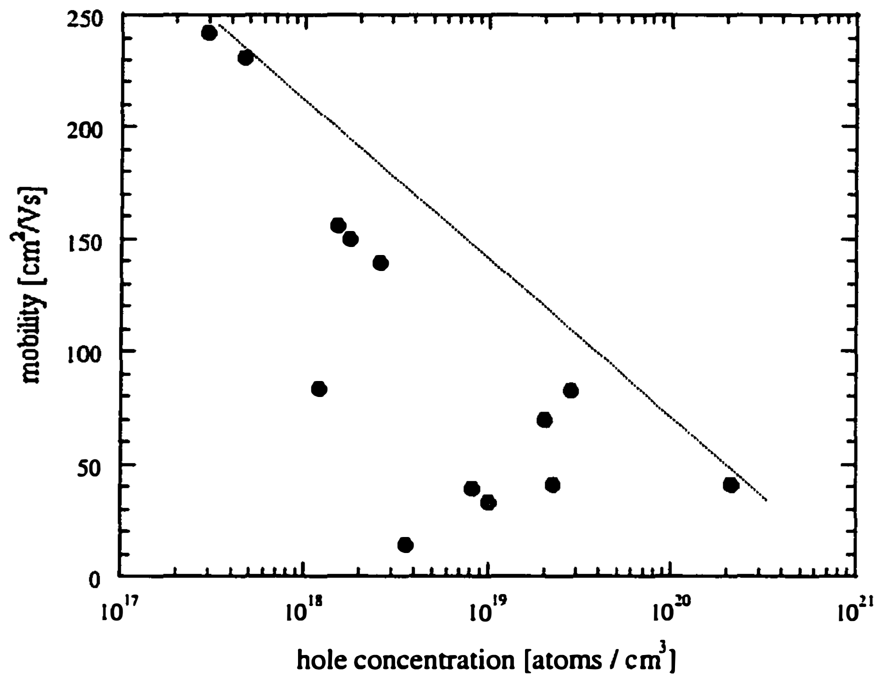


Figure4.08 Plot of gas source carbon hole concentration and mobility as measured by Hall effect. From Ryan Naone.

The I-V characteristics from the actual mirrors are plotted in Figure 4.07. The differential resistances are very good, considering the fact that transport occurs over more than 50 interfaces per mirror. Although the doping levels are higher in the gas source carbon doped mirror, the differential resistance is higher. The reason for this is that the gas valve doping source makes it hard to control lower doping levels. To obtain low doping, one must modulation dope thin layers within a thicker nominally undoped layer. As carbon is relatively immobile within the lattice, this can lead to high parallel mobilities and conductivities, but causes problems for vertical resistance. Indeed, the in-plane mobilities are quite high. Figure 4.08 is a plot of mobility versus layer concentration from the gas source carbon doping calibration. This

data was provided by Ryan Naone. The in-plane mobility is quite high, a problem which will resurface in the next chapter.

Table 4.2 Summary of mirror characteristics. Theory in bold, measurement in italics.

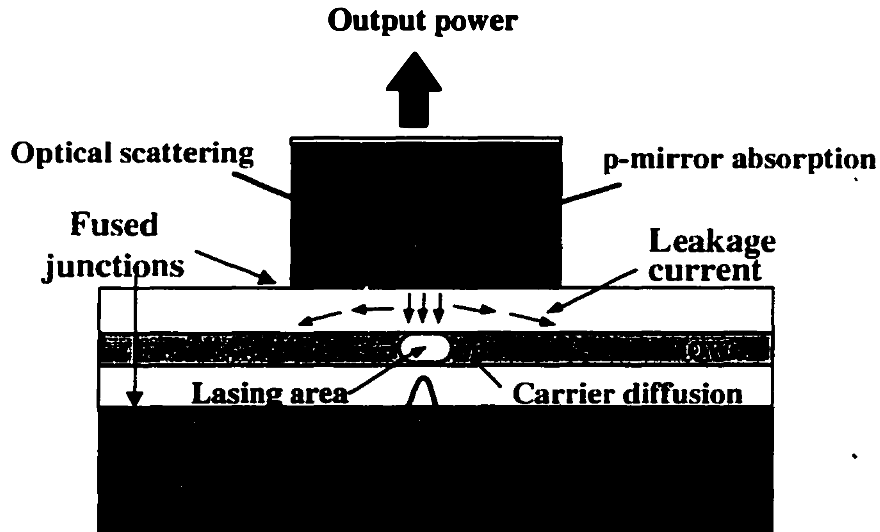
	25.5A Hegblom	25.5B Naone	24.5C Chiu
Al content	90%	90%	90%
Number of periods	25.5	25.5	24.5
Peak reflectivity	**99.885%**	**99.885%**	**99.85%**
Transmission through mirror	**0.115%**	**0.115%**	**0.15%**
Center wavelength	*1520 nm*	*1540 nm*	*1565 nm*
Low doping	$2.25(10)^{17}/cm^3$	$2.25(10)^{17}/cm^3$	$3.25(10)^{17}/cm^3$
High doping	$7(10)^{17}/cm^3$	$7(10)^{17}/cm^3$	$7(10)^{17}/cm^3$
Differential resistance	---	*14Ω*	*26Ω*
Expected $loss_{BA}$ contribution	**0.1%**	**0.1%**	**0.15%**
Aperture thickness	40 nm	30 nm	25 nm
Aperture distance from MQW	448 nm	448 nm	400 nm
Index pertubation	**0.02**	**0.015**	**0.012**

4.02 Two dimensional design

4.01.1 General design issues

There are many mechanisms of loss in a VCSEL. Not only must one consider the one dimensional analysis, but also the losses contributed by the two dimensional structure as well. Figure 4.09 is a VCL schematic illustrating the many different loss mechanisms to consider. In the previous section we covered material loss and transmission loss to the optical mode. This next section considers the effect of the two dimensional structure on current and

carrier loss in the active region, as well as additional optical loss induced by the choice of modal confinement.



$$I_{th}(T) = I_{ABC}(T) + I_{vertical\ leakage}(T) + I_{lateral\ leakage}(T)$$

Figure 4.09 Loss mechanisms in VCL design. Carrier losses are mainly from current spreading after the constricting aperture, and carrier diffusion out of the lasing region. Optical losses are mainly from free carrier absorption, diffraction and size dependent scattering loss.

The basic vertical cavity laser structure is shown in Figure 4.09. It consists of a gain region (MQWs) surrounded by two spacer layers that define the cavity, and two mirrors, one extremely reflective and the other slightly transmissive. Current is usually injected through the top mirror and collected through the bottom. To define the path the current takes, one can either ion implant through the injection mirror or etch to provide the confinement. It is difficult to scale ion implanted structures down to very small dimensions because of the deep implant and correspondingly high acceleration voltages necessary. In addition, lateral straggling and damage to the material is of

concern. Etched pillar devices are easier to fabricate, but fail to scale to small sizes due to scattering of the optical mode off the rough sidewalls of the pillar. In the etched approach, however, it is possible to further restrict the current via an oxide aperture. The purpose of the aperture is twofold: to constrict current and to guide the optical mode. Improper lensing through blunt oxide apertures, however, can cause diffraction loss at small oxide opening diameters.

We have chosen the etched pillar with an oxide aperture approach. Ion implantation would be especially difficult in a fused structure as the implant would have to maintain its profile throughout the high temperature fusion process. In addition, it is desirable to be able to guide the mode through the index perturbation afforded by the oxide aperture (n=1.6). Ion implanted structures are normally gain guided which can be detrimental to the dynamic performance of the device due to issues with thermal lensing. By placing the oxide aperture close to a null in the standing wave, we minimize the diffraction loss while still maintaining an index guided device.

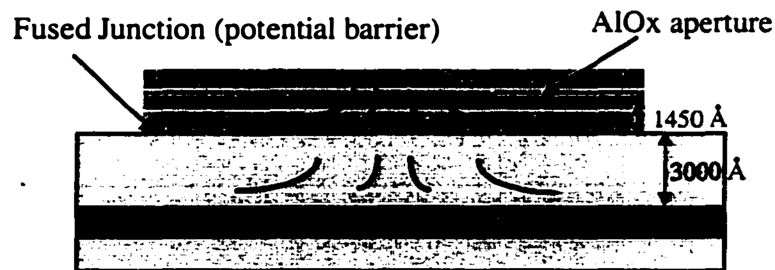


Figure 4.10 Current spreading considerations in a fused structure.

Thus, using an oxidized device, we concern ourselves mainly with the issues of current and carrier confinement in the active region. Short wavelength VCSELs have seen record minimum threshold currents using the oxide aperture approach[12]. However, in the GaAs system, it is possible to place the oxide aperture at the first null in the standing wave. Although there

has been promising work on the oxidation of InAs/AlAs superlattices lattice matched to InP[13], to date there is no reliable oxidation mechanism that can be included in the active region growth. Because we wish to remove the MQW region from the fusing surface, we have chosen a $3/2\lambda$ cavity. The fused junction itself is therefore placed at the second null in the standing wave. This relegates the AlGaAs oxidation layer close to the third null in the standing wave, 148 nm above the fused junction, which is still 300 nm removed from the MQWs. A schematic of this situation is depicted in Figure 4.10. The large distance between the current constricting layer and the active region is non-optimal for current confinement. Indeed, we believe lateral current spreading to be a large contributor to deviation from calculated threshold current of our devices. In particular, fused devices with a p-p fused junction suffer from a large distance between current confining aperture and the QWs. The voltage drop associated with the p-p junction will act as a barrier to hole flow, causing increased spreading.

This effect has been modeled by Piprek to show 50% less current entering the lasing region of the device at threshold[14]. The results from his calculations are shown in Figure 4.11(a) and 4.11(b). Figure 4.11(a) shows the structure of the device modeled. It consists of an oxide aperture in the GaAs side, a fused junction, and the InP active region. The simulation is run with and without the presence of traps at the fused junction. A n-type trap density of $1.7(10)^{13}$ per cubic centimeter is assumed and shown in the Figure 4.11(b) on the right. It is shown that with a modest interface trap level, over 50% of the injected current is lost due to spreading around the active region.

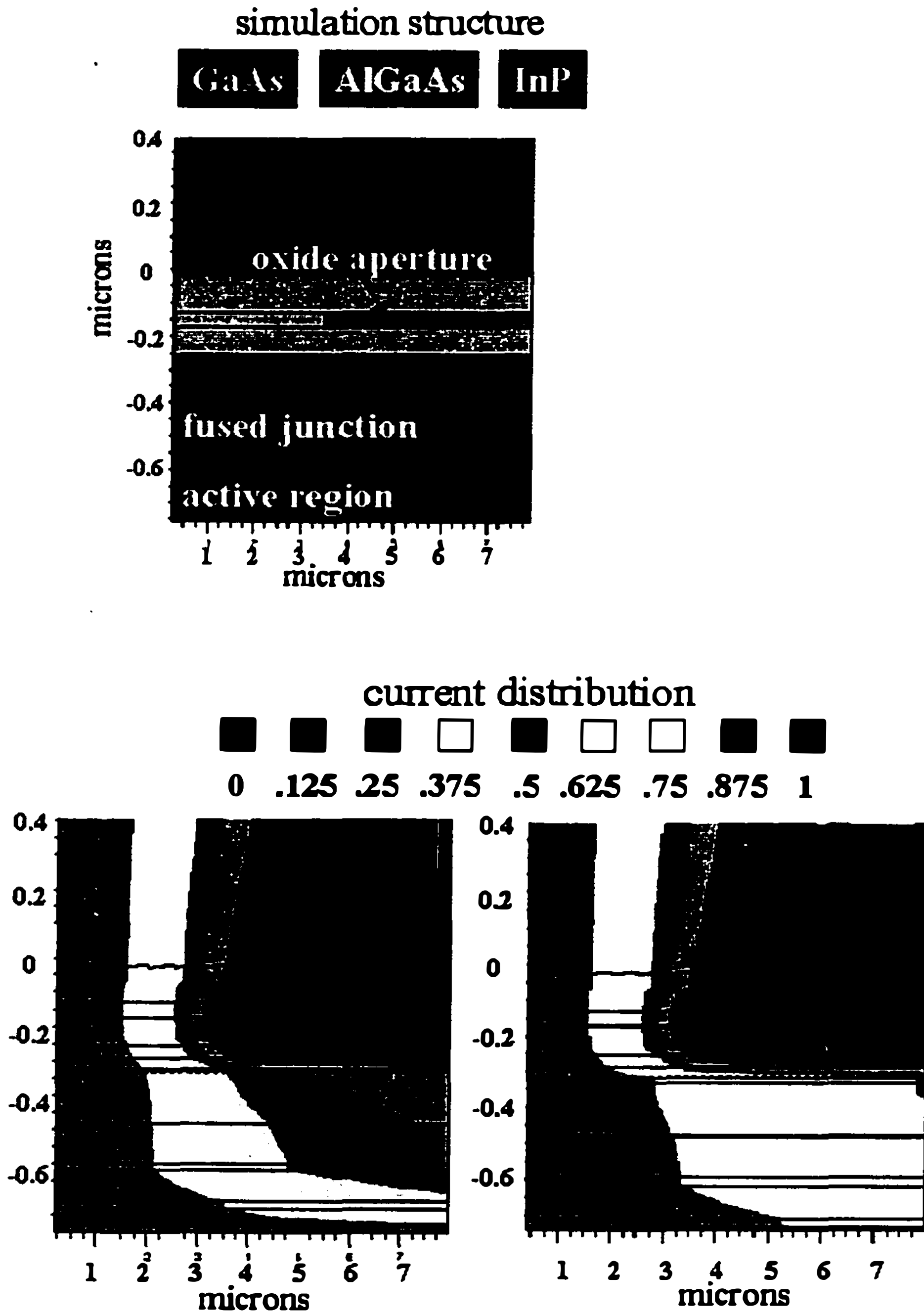


Figure4.11 (a) Structure of device. (b) Simulation results with and without traps at the fused junction. Simulation by J. Piprek.

Another concern in the two dimensional design of VCLs is carrier confinement. Lateral carrier leakage due to diffusion out of the active area has previously been addressed through buried heterostructure devices. Currently, there is much work on disordering to control this effect as well. To date, there has not been an appropriate method demonstrated with which the fused VCL could experience lateral carrier confinement. Re-growth on a fused epilayer is impossible due to the cross-hatch pattern arising from thermal mismatch. The next section will describe a design that attempts to use selective area fusion to both constrict current and confine carriers to the active region.

4.01.2 Designs fabricated in this thesis

The work in this thesis includes the design, fabrication, and characterization of three different structural VCSEL designs, which will be described in this section. The first is the basic design, drawing heavily upon the foundational design work of Margalit. However, the generations of this structure were fabricated with modifications in the fusion process, gentle modifications of the mirror and active region epilayer designs, and improvements in the structure to reduce bondpad parasitics. A schematic of this design is given in Figure 4.12. Current is injected through the top p-mirror and collected at the n- intra-cavity contact. An oxide aperture is used for current constriction and index guiding of the mode. Device 71 was fabricated using this exact design; device 75 was fabricated with an improvement in the n-intra-cavity bondpad for reduced capacitance.

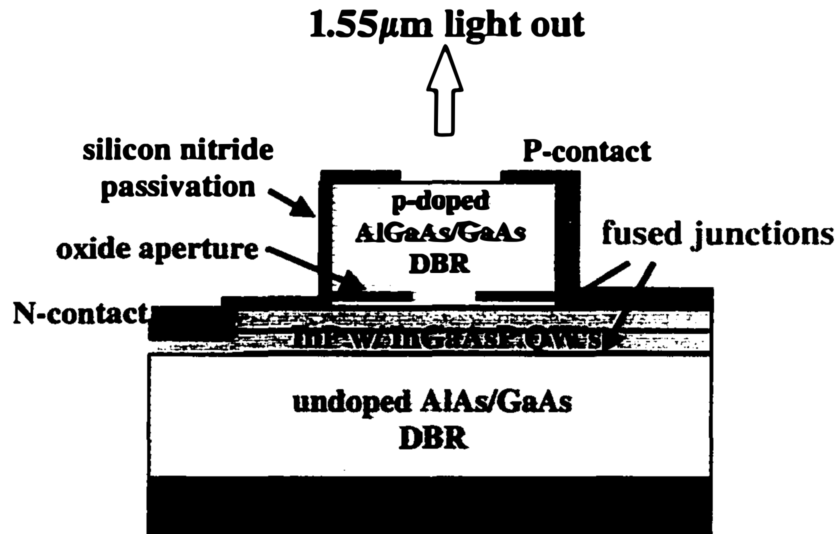


Figure 4.12 Schematic of the basic double fused VCL design. Current is injected through the top p-mirror and collected at the n- intra-cavity contact. An oxide aperture is used for current constriction and index guiding of the mode.

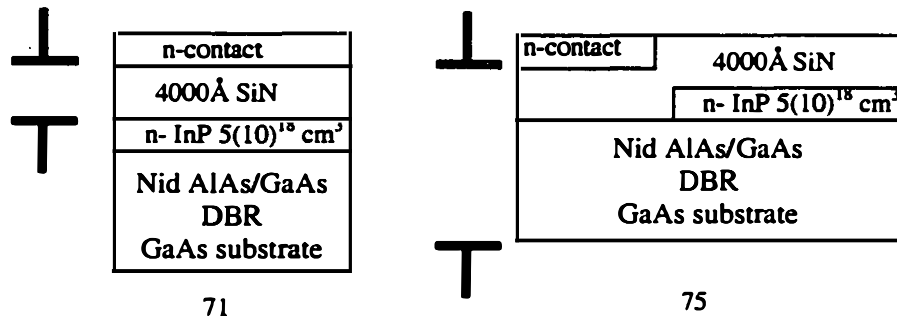


Figure 4.13 Schematic of the different bond pad configurations used to fabricate devices 71 and 75 from the basic VCL design. Bondpad capacitance is noted with the capacitor symbol.

Figure 4.13 illustrates this slight change in structure that will be shown in Chapter 6 to have a grand impact on the modulation performance of the device. Device 71 was fabricated with a 4000Å SiN layer between the

bondpad and the n-type InP cladding. To reduce the bondpad capacitance, the n-type InP was etched away to create the low capacitance bondpad of device 75. Besides this difference, the devices are essentially the same. Table 4.3 gives a summary of the individual structures. The active regions are similar and the mirrors are 25.5A for the device 71, and 25.5B for device 75.

Table 4.3. Summary of laser structures fabricated using the basic design.

	Device 71	Device 75
nid-mirror periods	31	31
p-mirror	25.5A	25.5B
Junction doping	Be $8(10)^{18}$ cm^3 300Å	Be $3(10)^{18}$ cm^3 300Å
Mode	1507 nm	1515 nm
Gain Peak	1542 nm	1540 nm
Estimated RT loss	.55%	.55%

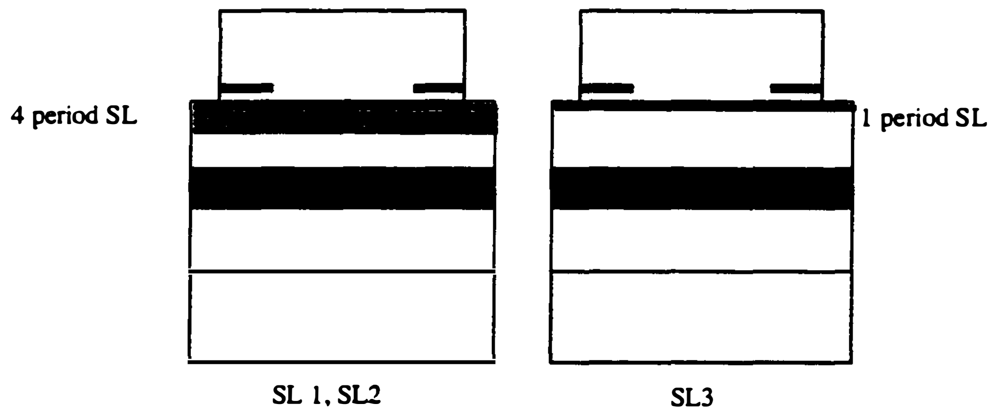


Figure 4.14 Schematic of the differences between the SL-VCLs.

The second structure is a direct result of the studies performed to characterize the electronic and optical properties of the fused interface. It incorporates a superlattice into the design of the active region in an attempt to increase the gain, getter the defects otherwise generated at the fused interface, and reduce the resistance of the fused junction. This structure is similar to the

basic VCL structure shown in Figure 4.12, but with the magnified changes to the active region illustrated in Figure 4.14. Three generations of devices were fabricated with these changes. The first two, SL1 and SL2, were fabricated with a 4 period superlattice at the fusing surface. SL3 was fabricated with but one SL period, or dopant supplying layer 75Å removed from the interface. A table of the different structural differences from the device runs is given in Table 4.4.

Table 4.4 Summary of SL-VCL parameters

	SL1	SL2	SL3
nid-mirror periods	31	31	31
p-mirror	25.5B	25.5B	24.5C
Junction doping	C $1(10)^{19}$ cm^3 100Å	Be $8(10)^{18}$ cm^3 300Å	C $1(10)^{19}$ cm^3 300Å
Mode	1570 nm	1570 nm	1530 nm
Gain Peak	1542 nm	1545 nm	1550 nm
Estimated additional SL loss	0.07%	0.07%	0%
Estimated RT loss	0.63%	0.63%	0.6%

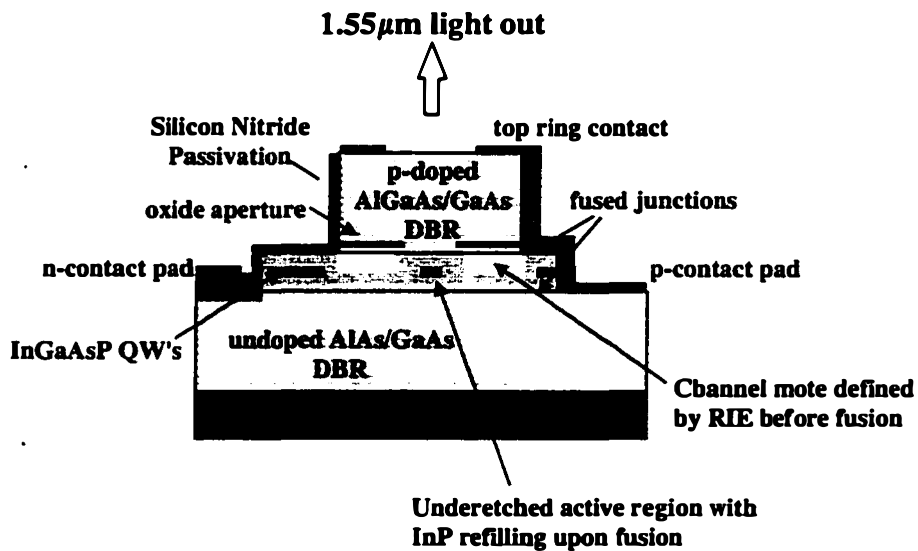


Figure 4.15 Schematic of Selective Area Fused (SAF) VCL.

The final device structure is an ambitious attempt to use the freedom afforded by the fusion process to confine both current and carriers in the active region. A schematic of this structure is given in Figure 4.15. Using selective area fusion, the channels that were once used strictly as liquid escape routes are incorporated into the device as an air aperture. One can use this technique simply as a current restriction technique by etching through the cladding, or more aggressively, as a carrier confinement technique, by etching through the cladding *and* the QWs. The high temperature processing step of fusion has been shown to involve a good deal of mass transport both to facilitate the fusion as well as simple because the fusion tales place above the growth temperature of the constituent materials. Sidewall recombination at the etched sides of the QWs will be avoided by the re-flow of InP into the under etched active region. This will not only serve to passivate the non-radiative surface recombination, but the higher band gap InP will confine the carriers, preventing lateral leakage. The large index step between the active area and the air gap will serve as a very strong waveguide for the mode. Only one working device was fabricated using this design. The epilayer information for this run is given in Table 4.5.

Table 4.5 Characteristics of the first selective area fused, underetched active region double fused VCSEL.

	SAF
nid-mirror periods	31
p-mirror	24.5C
Junction doping	C $1(10)^{19}$ cm^{3} 100Å
Mode	1550 nm
Gain Peak	1548 nm
Estimated RT loss	.6%

4.03 Summary

This chapter gave an overview of VCSEL design from the standpoints of both the 1D transverse optical design and the 2D structural design considerations. Detailed descriptions of the epilayers designed for the work in this thesis as well as the actual VCL generations that will be discussed in Chapter 6 were given. Special attention was given to the mechanism of current constriction chosen for each device design, as it has been shown that current spreading in fused structures is of the utmost importance to control.

4.04 References

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Chapter 5

Laser Processing

Every step in the processing of double fused VCLs is affected by the quality of the fused interface, and the fact that the device has undergone the fusion process. Poor fusion results in textured films, which have an adverse affect on all subsequent process monitoring techniques. Buckling of the fused film over channels affects the application of smooth resist profiles. The buried channels can act as capillaries into which all liquids will flow and at times etch the surrounding material. Excess strain at the fused interface has a dramatic affect on the oxidation of current apertures. The generic process sequence used in the fabrication of double fused VCLs is included in Appendix B. This chapter overviews that process, and details the extra process steps necessary for fabrication of the selective area fused, under-etched active region VCLs. Unfortunately, the generic process sequence is merely that- generic. The actual processing of double-fused VCSELs relies heavily upon experience and careful observation after every processing step. Many differences in performance between the generations of VCL s fabricated in the duration of

this work can be attributed to processing errors and oversight- by simply assuming that the generic process sequence would work.

5.01 Choice of active material and mirrors

The most important factor affecting the quality of the fusion is the surface quality of the materials to be fused. Chapter 2 described the tolerable defect densities and defect types to be accepted as good growth. It is many times useful to fully characterize the as-grown material before the processing sequence begins. This will aid in the choice of the correct materials for a proper gain mode offset. To do this, RT photoluminescence of the active region should be taken. The RT peak gain should be noted, taking into consideration that the peak gain in an active device will be slightly blue-shifted due to higher injection density. In addition to this, the thickness of the cavity can be determined through selective etching of the MQW region cladding and wells; the effective cavity length is determined by λ/n. Because the resolution of the Dektak is not better than 100Å, it is also useful to mount the active region on a glass slide, remove the substrate and etch stop layer, and use the lambda9 interferometer to determine the optical thickness of the film.
A severe problem in the past has been the misplacement of the QWs in the cavity. Table 5.1 lists the measurements of n versus p side cladding for some of the active regions processed in this thesis. The n side of the cladding is at times 15% shorter than the p side, resulting in a misplacement of the gain area from the standing wave peak. Such a large misplacement of the QWs results in a reduction in the gain enhancement factor from 1.76 to 1.26 for the worst case scenario of sample B (resulting in 28% less gain) and a reduction to 1.62 for the best case scenario, sample A.

Table 5.1 Sampling of active region calibrations showing the effect of misplacing the QWs with respect to the standing wave peak in the cavity. Although a symmetric cavity is designed, the n-cladding always ends up shorter than the p-cladding. The average gain reduction factor reduces the gain enhancement factor that results from the standing wave pattern in the cavity.

sample	p-cladding thickness (nm)	n-cladding thickness (nm)	Misplacement of peak gain (nm)	Average gain reduction factor
A	295	273	22	0.92
B	287	239	48	0.72
C	363	320	43	0.75
D	310	280	30	0.86

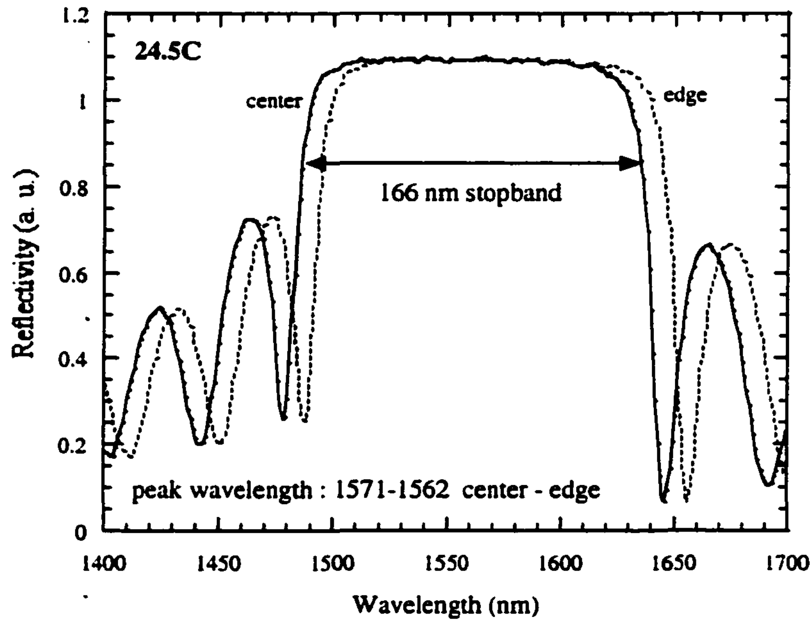


Figure 5.01 Example of non-uniformity in expitaxial growth of the mirror samples. Dotted line represents a measurement 1 cm from the edge of a 2-in. wafer and solid line represents measurement from the center of the wafer.

The mirror growths must also be taken into account. Since the final lasing mode is determined both by the optical path in the cavity and in the mirrors, it is important to choose wisely from the available epilayer growths. Figure 5.01 shows the lateral variation of the mirror reflectivity across a two-inch wafer for mirror 24.5C. By choosing pieces from the edge or center, one can get as much as 50 nm (3% growth rate variation) of play for the same growth. To start the fabrication, 8x8 mm pieces of the active region, p-mirror, and n-mirror are chosen and cleaved according to the desired final wavelength.

5.02 Etching channels for current confinement

Once the appropriate materials have been selected, channels can be etched in order to create a current confining structure at the same time that the channels are etched for liquid and vapor escape. A scanned image of the channel pattern is shown in Figure 5.02. The liquid escape channel width (straight lines) is 10 μm, and the width of the current confining channels (circles) ranges from 3μm to 15 μm, depending on the size of pillar that will be etched over it. The center of each current aperture is 8μm in diameter. A dotted circle indicates where the actual laser pillar will reside.

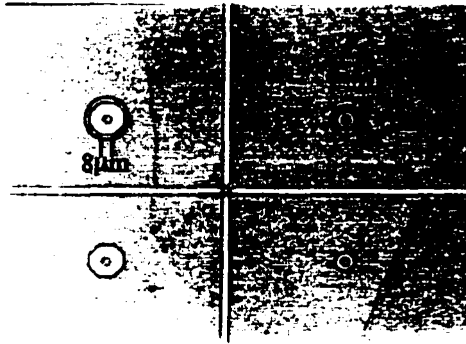


Figure 5.02 Optical micrograph of photoresist pattern to define both liquid escape and current aperture channels. Dotted circles indicate future position of VCL pillar.

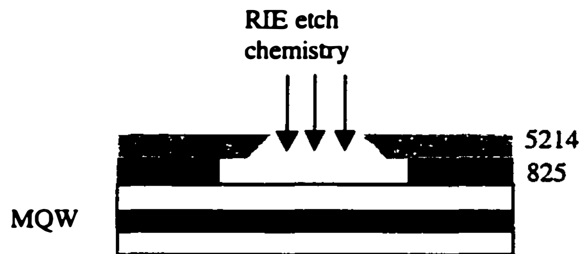


Figure 5.03 Schematic of photoresist profile required for RIE etch of channels. A deep undercut is desired to maintain surface quality.

Because of the feature size, it is impossible to wet etch the channels as a severe undercut of the photoresist would ensue. For this reason, a dry etch is preferred. However, the fusion is very sensitive to surface roughness. The physical component of dry etching is known to burn in, or leave a residue on the surface of sample at the edge of the PR covered region, in this case, right at the edge of the channels. It is therefore important to use a resist profile with a severe undercut. We use a combination of 825 and 5214 photoresist to yield a PR profile cartooned in Figure 5.03. This combination of resists as well as feature sizes is the most challenging to perfect. The positive 825 resist on bottom experiences a flood expose after spin on. This purpose of the flood expose is to overexpose the 825 resist layer, so that a good undercut of the resist is easily obtained. The 5214 resist exposure and develop is straightforward. However, the smaller the feature size, the longer the developing takes. In a normal lithography this is fine- however since the central feature of all the constricting channels is the same, the 5214 resist for the channels will develop at different rates, while the rate of undercut remains the same. The end result is that the undercut is different for each channel width, which is fine as long as the undercut does not go to completion, effectively popping the top layer of 5214 resist off. Also, if the 5214 resist is

not rigid enough, it will bend down and touch the sample surface, undermining the efforts at achieving an undercut.

The channels are etched in either $CH_4/H_2/Ar$ or $SiCl_4/BCl_3/Cl_2$. At this point, one can choose to either etch through the QWs for both carrier *and* current confinement, or simply as deep into the cladding as possible, for current constriction. If etching through the QWs is chosen, then the QWs should be under-etched approximately 1μm. This will result in a 6 μm device diameter, for which we have consistently had the best results. The effects of carrier confinement will only be rewarded in very small aperture devices, something which can be tested in future work. To under-etch the QWs, a slow, anisotropic selective etch is required. A 3:1:5 solution of H_2SO_4: H_2O_2: H_2O at a constant temperature of 90°C has an etch rate of .75 μm undercut per 5 seconds. A simple tool for measuring the undercut was incorporated into the mask and is shown in Figure 5.04. It includes a series of small features ranging in size from 1 μm diameter to 6μm diameter. After the underetch is complete, simply by using the microscope one can determine an etch rate by how many of the features have been popped off. For example if the one and two micron features are missing but the three micron feature is intact, then the under-etch is between 1 and 1.5 μm. A cross-sectional SEM of an under-etched active region fused to a test mirror structure is shown in Figure 5.05. The fusion is good, with an approximate under-etch of 1μm.

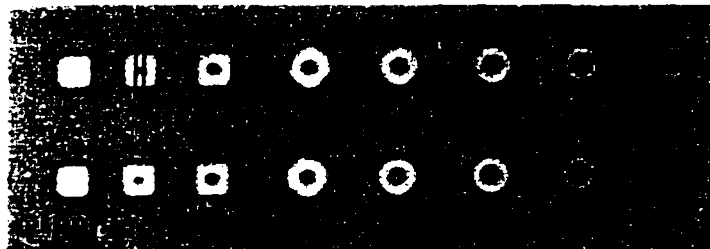


Figure 5.04 Structures to monitor under-etch of MQWs. This under-etch is between 0.5 and 1μm.

Figure 5.05 Cross-sectional SEM of fused active region with under-etch.

5.03 Double fusion

Once channels are etched, one can fuse the InP/InGaAsP active region to the GaAs/AlGaAs p-mirror as described in Appendix A. The InP substrate can be removed as described in Chapter 2. The photoluminescence from the fused layer can be measured using room temperature PL as shown in Figure 5.05. With the substrate removed, the etch-stop layer is etched with 3:1:50 H_3PO_4:H_2O_2:H_2O. This process can take between 5-10 minutes depending on the exact etch-stop layer composition. Important to the laser design is that the etch-stop layer is completely removed, so over-etching of this layer is usually done. With this layer removed, the second fusion can proceed. This second fusion is done at slightly lower temperatures (575-600°C), and slightly lower pressures (1.5 MPa) in order to minimize the effects of high temperature and pressure processing. The second fusion, contrary to popular belief, is easier than the first. One hundred percent uniformity is almost always achieved. This may be a result of the stiffer GaAs substrate- in effect, two GaAs wafers are being pressed together with an intermediary InP layer. After the second

fusion, the AlAs stop etch layer is removed in 1:1: $HF:H_2O$ for 10 seconds. The epilayer structure is complete, and processing proceeds as if one had just grown a monolithic structure, with the complications of a crosshatch pattern on the surface of the sample, and some unfused areas. At this point, the mode position of the laser is recorded, as shown in Figure 5.06. In this particular case, the mode of the laser is at 1571 nm whereas the peak gain is at 1545 nm. Such a large mode gain offset is non-optimal, although this laser (SL1) did lase CW up to 40°C.

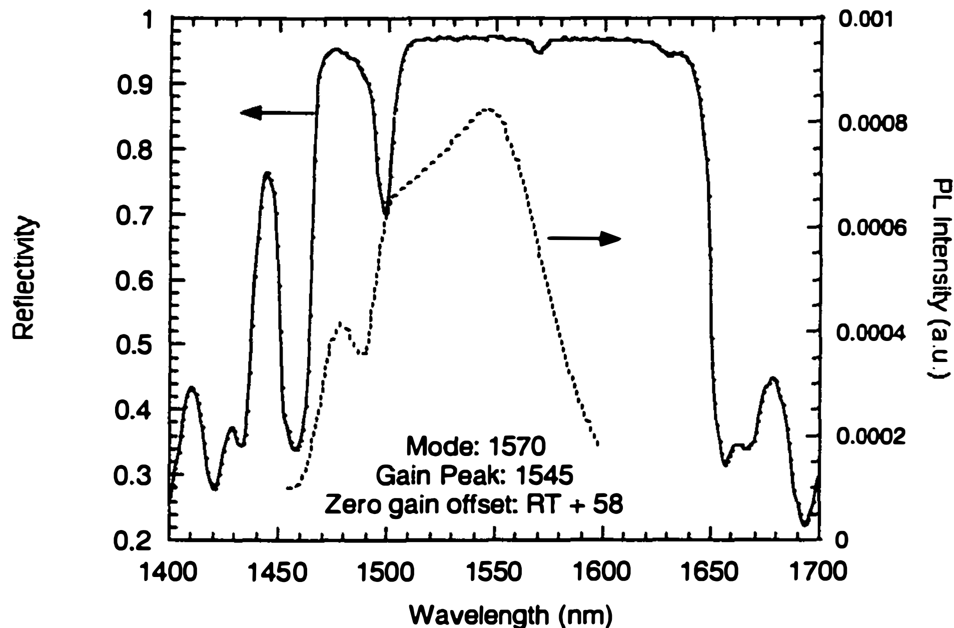


Figure 5.06 Room temperature PL and mode position of single and double fused structure, respectively.

5.04 p-contacts and pillar definition

The next step in the processing is the deposition of the p-contact. This ring contact will undergo treatment in the oxidation furnace at 430°C for 10-20 minutes. Because of this, an un-annealed contact is chosen, in this case,

Ti/Pt/Au (200Å/2000Å). The surface clean before deposition is important: after opening the rings in the PR, the sample is dipped for 10 seconds each in 1:10 $NH_4OH:H_2O$ and 1:10 $HF:H_2O$ to remove the Ga and Al oxides, respectively. After liftoff of the metal, the entire sample is coated with SiN before lithography to define the pillars is begun. The SiN layer will later serve to protect the metal during the oxidation step.

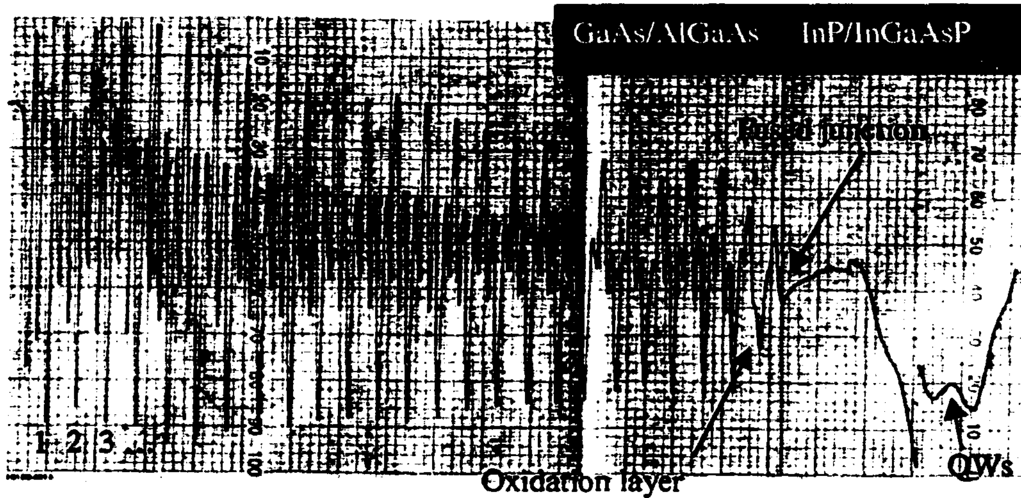


Figure 5.07 RIE etch monitoring with HeNe laser.

The mask for the pillar etch is AZ4330, a 3μm resist. The SiN layer is etched in CF_4. The pillars are then etched using a 5:2.5:25 mixture of $SiCl_4$:Cl_2:BCl_3. The chamber pressure of 5 mtorr and applied microwave power of 60W is used. A graph of the optical monitoring of the etch is given in Figure 5.07. The BCl_3 is essential to maintain the surface quality throughout the 30 min etch as it removes any forming oxide. Although Cl_2 gives a much straighter sidewall profile, using Cl_2 alone is very sensitive to the cleanliness of the RIE chamber and surface morphology of the sample. As indicated before, the fused surface after fusion has a crosshatch pattern which can detrimentally interfere

with the optical monitoring of the RIE etch. Also, specific to the under-etched structure, it is desirable to have a bit of a shoe at the bottom of the etch to

Figure 5.08 Example of undesirable sidewall profile frequently obtained after plasma-therm RIE has been opened for maintenance.

improve the stability of the structure. In some cases, only 1 μm tolerance is left between the outer edge of the current confining channel and the edge of the pillar being etched. A shoe in the sidewall profile grants additional tolerance. The plasma-therm RIE that was used to perform this etch suffered many problems with background pressure and general cleanliness. The deterioration of this machine over time lead to many problems such as undesirable sidewall profiles shown in Figure 5.08. This sidewall will pose a serious problems when trying to contact the top of the pillar with appropriate bondpads for high speed modulation. The inter-connect metal will need to climb the sidewall profile, a much easier task with a smooth sidewall. In that case, it is suggested to use the pure Cl_2 etch with a minimum amount of BCl_3 in the background. Figure 5.09 illustrates the sidewall profile obtained using the pure Cl_2 etch.

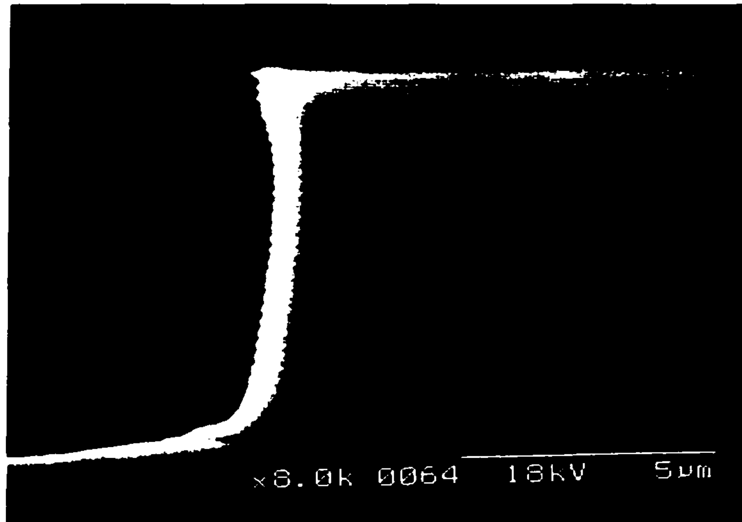


Figure 5.09 Example of etching sidewall in pure Cl_2 gas.

Once the fused junction is reached, the power of the etch must be increased to 200W. Under the same etch chemistry, the InP and quaternary layers will etch in about 1000Å/ minute. Figure 5.07 illustrates the optical reflectance monitoring of this etch. After the junction is reached, the etch will slow, and the signal will decrease. The break in the signal line results from turning the sensitivity from 0.2V/ division to 0.1V/ division on the graph paper. After etching through the InP cladding, the signal will increase. When the signal is halfway down the peak, the etch through the QWs is complete. It is important to note the position of the laser monitor on the actual sample: there is non-uniformity even over a 1 cm^2 piece. After etching the pillars, the sample is ready for oxidation.

5.05 Lateral Oxidation

Although the selective area fused, under-etched active region samples utilize the channels for current constriction, the oxidation of the edges of the pillars

could reduce the effects of a stray current path that may flow around the center device region, as shown in Figure 5.10.

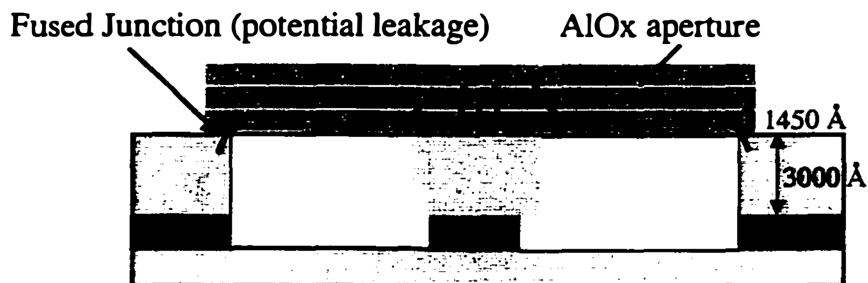


Figure 5.10 Schematic of fusion region indicating the need for an oxide aperture. The fused areas on the circumference of the channel are potential current leakage paths. Oxidation would minimize this effect.

As can be expected, the fused junction affects the oxidation rate of the AlGaAs layer. It is necessary to calibrate each new mirror by fusing a test piece to an active region and calibrating the oxidation rate. This can be done either by infrared camera or through cross-sectional SEM. The infra red camera is a quick way to determine the oxide depth, although it is difficult to resolve. An example image is shown in Figure 5.11.

Figure 5.11 Reproduction of an infrared image through a 6µm mirror showing a 20µm oxidation depth. The calibrated rate is 1µm/ minute for a 40 nm $Al_{98}GaAs$ *layer.*

The oxide depth is 20 μm. The benefit of using an infrared microscope is that the oxide depth will not be obscured by a diagonal cleave across a SEM sample. The tilt in the SEM can also play tricks on the eye when determining the oxidation depth. In the SEM, the oxidized layer will appear darker than the surrounding AlGaAs layer, and the front is easy to spot as it is normally marked by a cleave plane due to the high stress associated with the shrinking oxide layer. An example is shown in Figure 5.12.

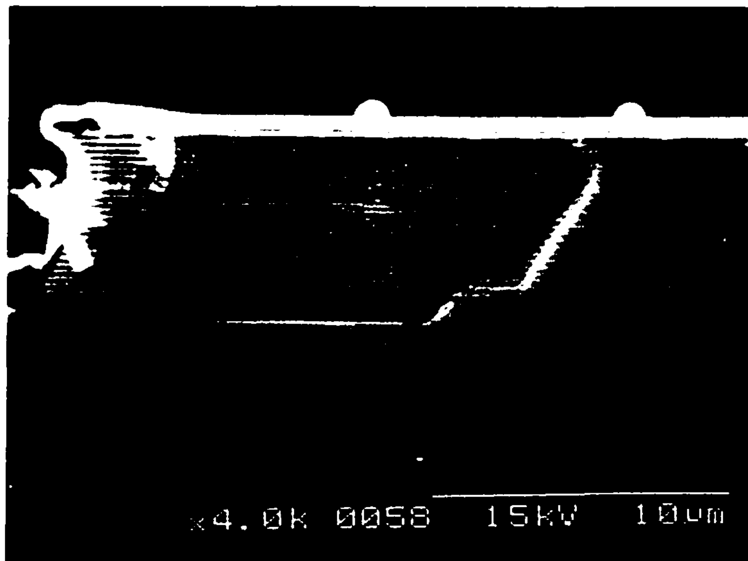


Figure 5.12 SEM image of a 40 nm $Al_{.98}GaAs$ oxidation layer. The cleave damage is a good indicator of where the oxidation front lies.

5.06 Process completion

After oxidation, the SiN is removed from the top of the pillars, and preparation begins for the n-contact. The n-contact is Ti/Au, and will at once contact the n-InP as an intra-cavity contact and create the p-bondpad interconnect to the top of the pillar. First, one tries to minimize the p-bondpad capacitance by etching away the n-InP underneath the contact area. This

underetched region can be seen in Figure 5.13 as a square slightly larger than the p-contact bondpad.

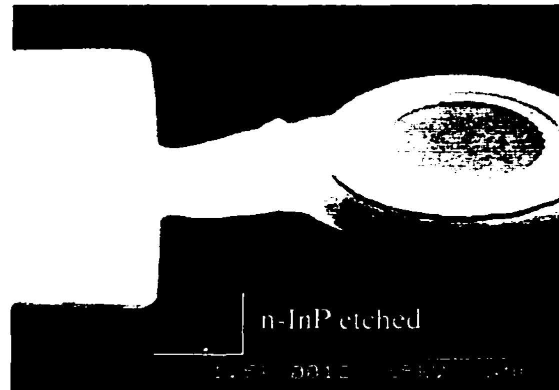


Figure 5.13 SEM of p-bondpad etch, pillar climb, and metallization.

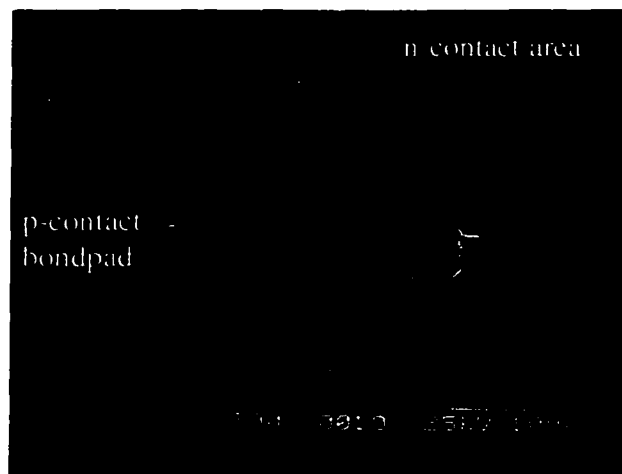


Figure 5.14 SEM of final laser structure showing n and p-contact areas for 50Ω impedence matching to coplanar ground-signal-ground microwave probe.

SiN is then put down over the whole sample for isolation of the inter-connect. A ring is opened at the top of the pillar and around the base of the pillar where the broad area n-contact is made. These regions are shown in Figure 5.14. In

order for the inter-connect metallization to be made, an angled, rotating evaporation must be performed. The metal must climb the 7 μm tall pillar. Once again, this is a very difficult lithography, as a large undercut of the photoresist profile is necessary to assure liftoff of the metal. Again, the wide variation in feature size complicated the exposure time, and the topography of the sample complicated this matter even further as resist piles up at the foot of the pillar, and is very thin on top of the pillar. The same photolithography scheme is used as was discussed in the channel definition section earlier. An angle of 18-20° is chosen for the evaporation. The desired metal thickness is achieved by calculating the distance of the sample relative to the crystal monitor from the source, and realizing that the thickness follows a $1/d^2$ law. A cross-sectional schematic of the finished device alongside a cross-sectional SEM are shown in Figures 5.15 and 5.16, respectively. The device performance will be discussed in the next chapter.

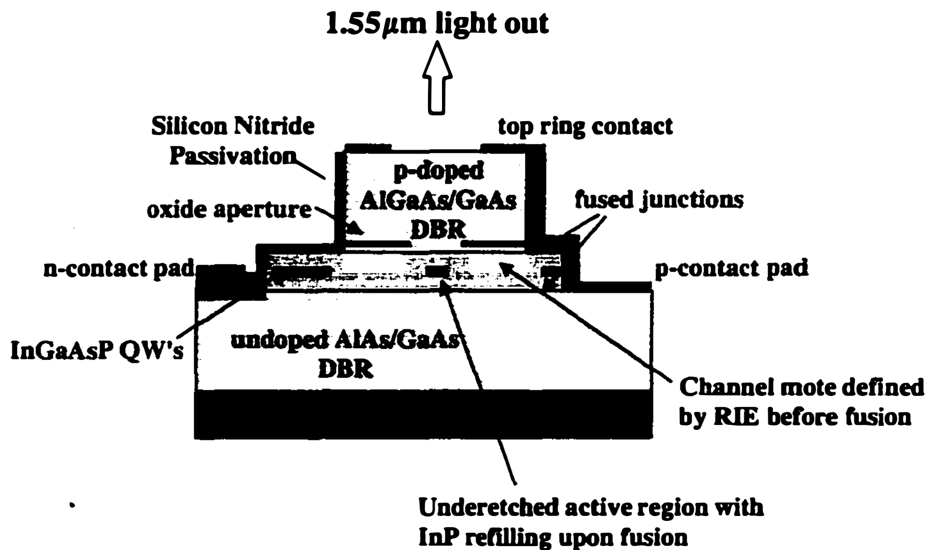


Figure 5.15 Schematic of final device structure.

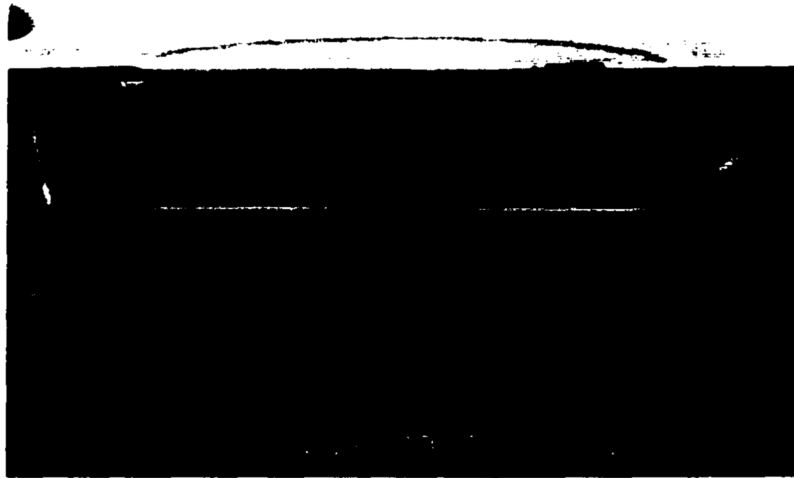
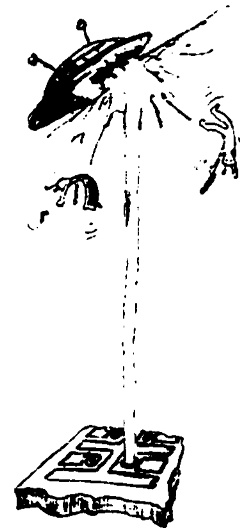


Figure 5.16 Cross-sectional SEM of final device. The current confining aperture is clearly visible.



Chapter 6

Analysis of Device Results

The balance between gain and loss in a VCL is delicate. Device performance is extremely sensitive to subtle growth errors, dopant concentrations and distribution, and potential barriers to current flow. Chapter 1 outlined the large number of challenges facing long wavelength materials systems. The physics of low energy gap materials make the realization of a VCL at long wavelengths just a little bit more difficult to achieve than at shorter wavelength. Most significantly, the absorptive losses are higher, Auger recombination is more pronounced, and the index contrast in the lattice matched mirrors is smaller, resulting in larger penetration depths of the mode into the mirrors and consequently more loss. Fusion bonding allows for the integration of high index contrast mirrors usually at the expense of a resistive interface. Feared optical loss associated with the interface forces the current confining aperture to a non-optimal position relative to the QWs. The fusion process can deteriorate the quality of the designed epilayers, and make processing more difficult. However, the fusion process affords new possibilities and creativity to the device designer. The current constricting

channel and the SL VCL for enhanced material gain after fusion are two examples of this freedom.

The trade-offs between this freedom and the sometimes deleterious effects of the fused interface on device performance are explored in this chapter. Section 6.01 presents the general light-current-voltage characteristics from all generations of devices. This is meant as an introduction and comparison of the many generations of devices described in Chapter 4. Section 6.02 will present an analysis of the scaling of the VCLs and summarize the round trip loss. The thermal behavior of the device generations will be analyzed in Section 6.03. Perhaps the most important limitation to the future improvement of the double-fused VCLs is presented in Section 6.04: the kink in the LIV. Finally, the modulation response of three different generations of devices will be presented in Section 6.05. A summary will be given in Section 6.06, and the benefits of each design will be reviewed. In the end, however, there can be no argument that fusion bonding is at present the most viable technique to demonstrate and realize a commercial quality long wavelength VCL.

6.01 Light –Current-Voltage Characteristics

6.01.1 Basic design: Devices 71 and 75

Device 71 was fabricated using the original VCL design, with an oxide aperture for current confinement. The oxidation depth was 20 μm; any device diameters henceforth quoted will refer to oxide aperture diameter. A room temperature trace of the L-I-V characteristic from one of the best VCLs on the wafer is shown in Figure 6.01. With an aperture of 6 μm, the threshold current is 2 mA, and the threshold voltage is 2.5 V. If 0.8 V is attributed to the active region diode, and 1.2 V attributed to the fused junction, then 0.5 V can be

attributed to the mirror. Indeed, this is the measured voltage drop across the mirror used in the fabrication of this device. The differential resistance is 200 Ω, and the differential efficiency is 6.7 %. The maximum output power of this device is 250 μW, however the maximum output power from this generation is 850 μW. Devices of aperture size 6 μm and less were single mode, exhibiting side mode suppression ratios in excess of 50 dB. The average room temperature single mode output power was 200 μW; the average multi-mode output power was 500 μW. The lowest threshold current achieved was 0.8 mA for a 4 μm device.

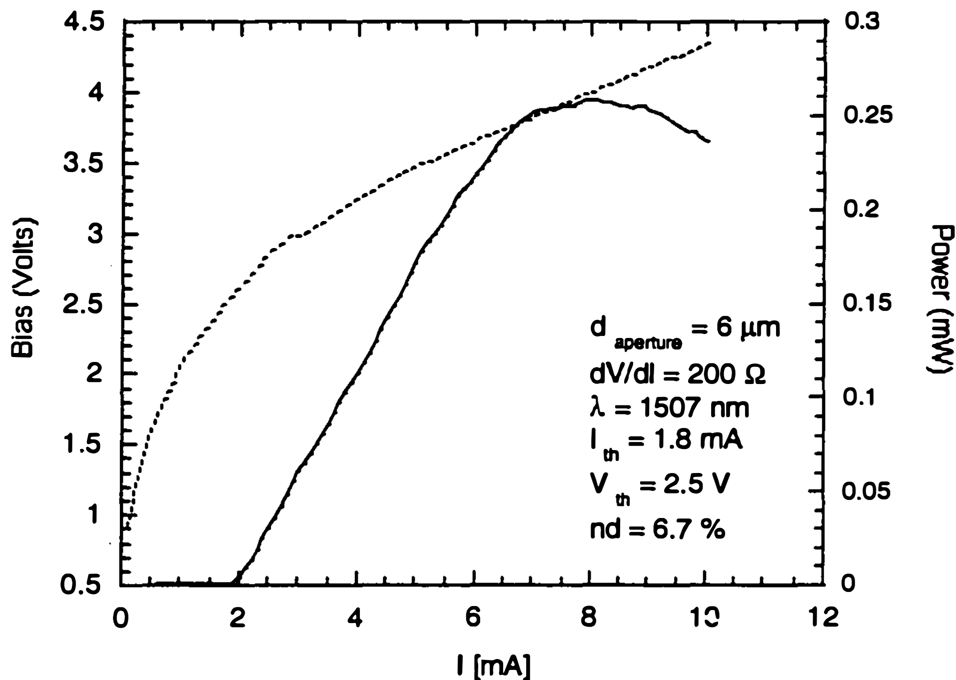


Figure 6.01 Light-current-voltage characteristic from a typical laser on device 71.

The threshold current density of the devices fabricated in this thesis is hard to measure, as we are unsure of the exact amount of lateral spreading underneath the oxide aperture. If we neglect current spreading and scattering,

the corresponding threshold current density for this device is 6.4 kA/cm^2. This is much higher than traditional values quoted in the literature of $1 kA/cm^2$. Much work has been done to understand this spreading by way of size dependent threshold analysis[1, 2]. A plot of threshold current and aperture threshold current density versus aperture diameter is given in Figure 6.02. Clearly the threshold does not scale with device diameter. Perfect scaling would result in a reduced threshold current with size, and would therefore be inversely proportional to the square of the device radius. However, we see a deviation from this decrease at small apertures, similar to trends seen in GaAs based VCSELs. This deviation results from the fact that as the device diameter is reduced, the effects of current spreading around the aperture become more pronounced. In addition, increased resistance, both thermal and electrical, are a direct result of device scaling. Many factors contribute to the non-ideal device scaling of threshold currents. For a detailed discussion of such effects, the reader is referred to[2].

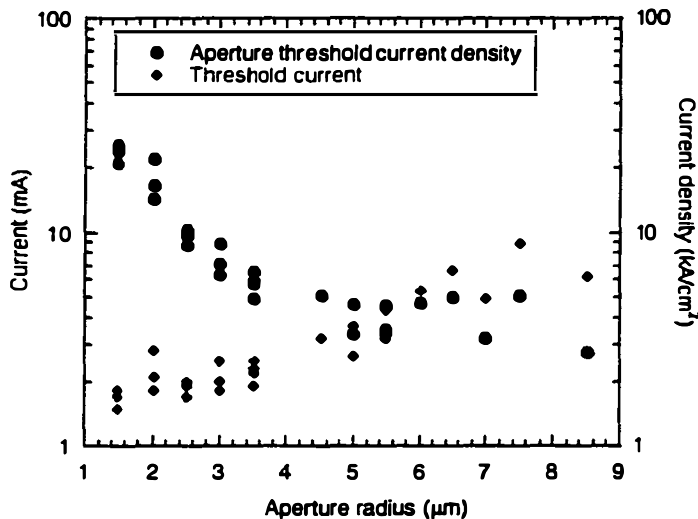


Figure 6.02 Plot of threshold current and aperture threshold current density versus oxide diameter for device 71. Non-ideal scaling is attributed to lateral current spreading after the aperture.

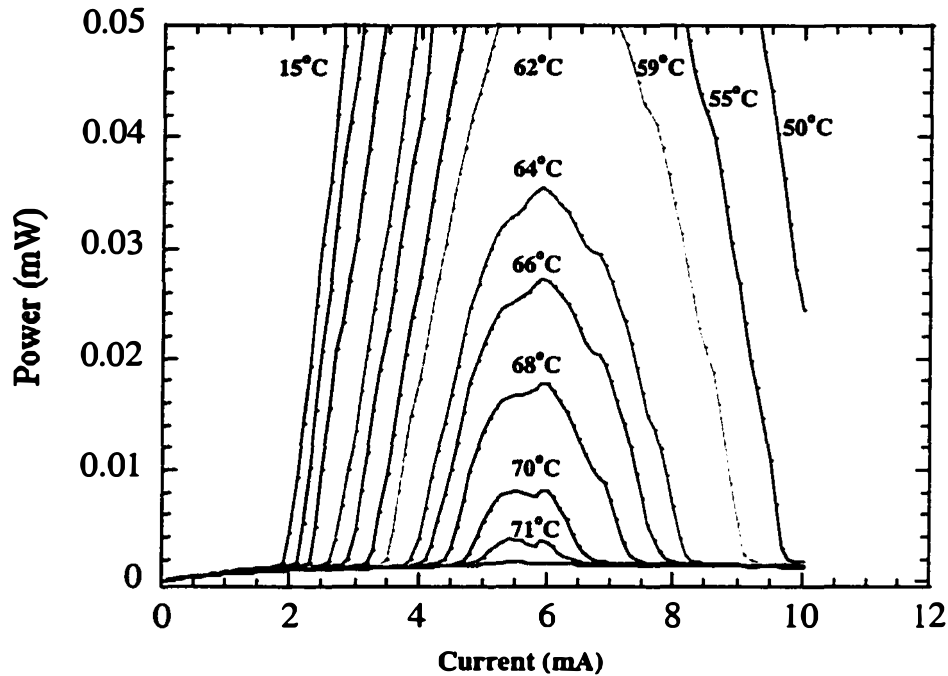


Figure 6.03 L-I-V characteristic of device 71, demonstrating superb high temperature performance.

The room temperature (RT) photoluminescence peak of the active region is at 1542nm and the lasing mode is at 1507nm. The most remarkable performance spec of this device is its high temperature operation. Figure 6.03 shows the high temperature L-I curves of a device with a 6μm oxide opening. The improved temperature performance of this device (over the previous record of 64°C) cannot be attributed to the misalignment of the gain peak and optical mode at RT, as the gain-offset increases with temperature. The gain peak and mode wavelength shifts with temperature are 0.54 and 0.11 nm/K, respectively[3]. The zero gain offset is calculated to be at -53°C and the optimum temperature for low threshold operation is expected at –123°C when the mode wavelength is 30 nm longer than the gain peak wavelength[3].

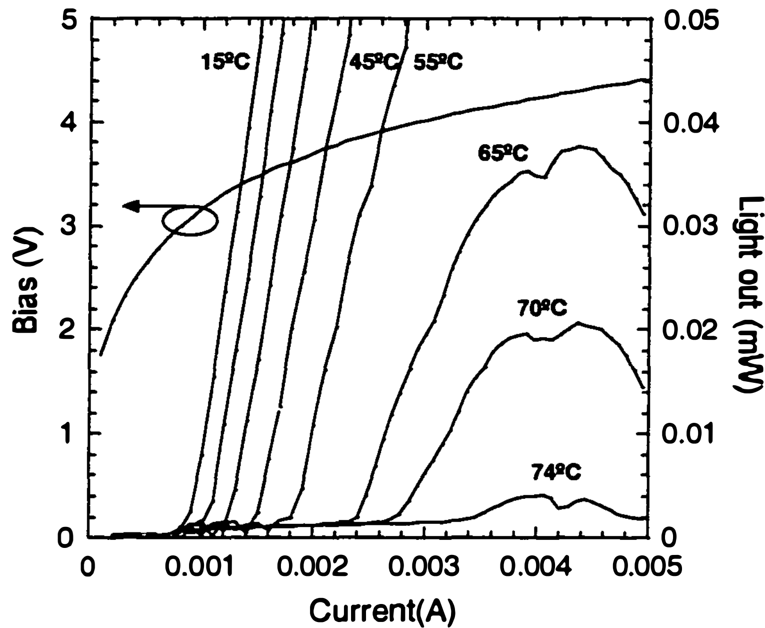


Figure 6.04 L-I-V characteristic for device 75, demonstrating the highest reported temperature operation of any electrically pumped LW-VCL.

The high temperature performance of generation 75 is slightly better, reaching a maximum cw operating temperature of 75°C. The characteristic L-I-V is shown in Figure 6.04. This particular device has a 5 μm oxide opening, and a room temperature threshold current of 0.9 mA. The only design difference between the 71 and the 75 devices are changes that were made to the processing sequence to improve device parasitics and some differences in the mirrors. Once again, the high temperature performance of this device cannot be attributed to the misalignment of the gain peak and optical mode at RT, as the gain-offset increases with temperature. The RT peak gain is 1542 nm and the mode of this VCL generation is at 1515 nm. The zero gain offset is calculated to be at -38°C and the optimum temperature for low threshold

operation is expected at −108°C. However, the slightly better alignment of the mode gain offset may account for the slight improvement of device performance.

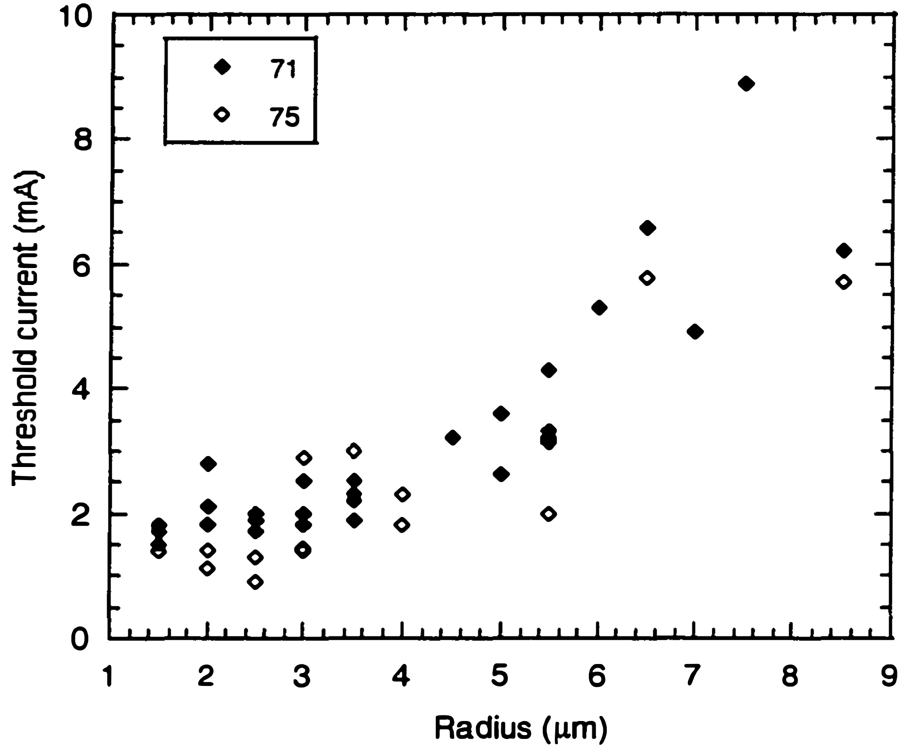


Figure 6.05 Comparison of threshold current scaling between device 71 and device 75. No significant difference is noted.

One important difference between the device runs to note is the higher threshold and operating voltage of device 75 : 3.2 V. This increased voltage can possibly be attributed to the carbon doped re-growth on the p-mirror. For the first time, we tried to use a structure that was entirely carbon doped. However, subsequent fused junction analysis reveals that carbon doping on the GaAs side of the fused interface always results in larger fused junction resistance. A possible explanation for this is that the Be is mobile and

accumulates at the junction, whereas carbon is less mobile and cannot compensate the n-type charge at the interface. In general, however, when the threshold currents and scaling thereof are directly compared between the two generations of devices, no difference is noted. A plot of threshold current versus aperture radius comparing the two sets of devices is included in Figure 6.05. Despite the added voltage drop, the overall performance of device run 75 was better. Ninety-five percent of the sample area fused, and 100% of the devices with open oxide apertures lased. A histogram comparing the high temperature performance of the two generations is included in Figure 6.06.

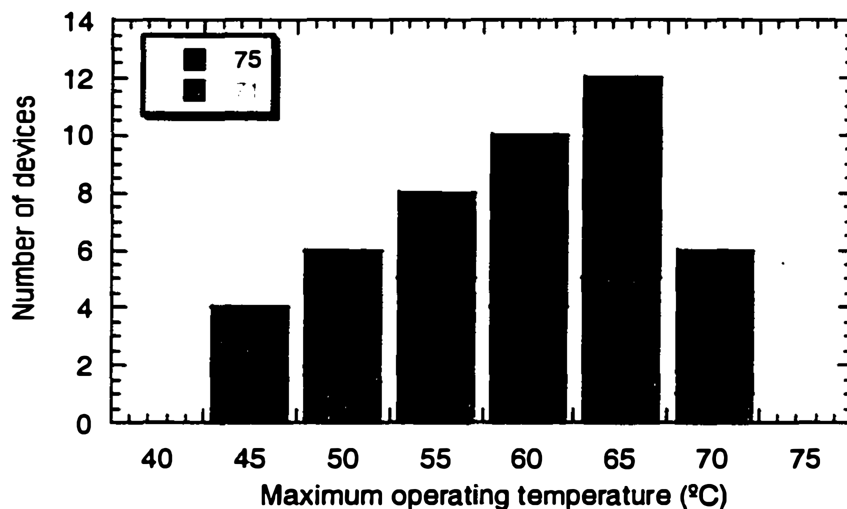


Figure 6.06 Histogram comparing the high temperature operation between the device runs 71 and 75. Despite larger threshold voltages, more devices from set 75 operated to higher temperatures, a testimony to the uniformity of the fusion.

A parameter of interest to measure is the wall plug efficiency of the devices. A plot of wall plug efficiency versus device size is included in Figure 6.07. A maximum wall plug efficiency of 1.8% is achieved for the smallest devices of generation 75. This low wall plug efficiency is a direct result of the

high reflectivity mirrors used in this device generation, and is an order of magnitude less than typical wall plug efficiencies quoted in GaAs based VCSELs[4].

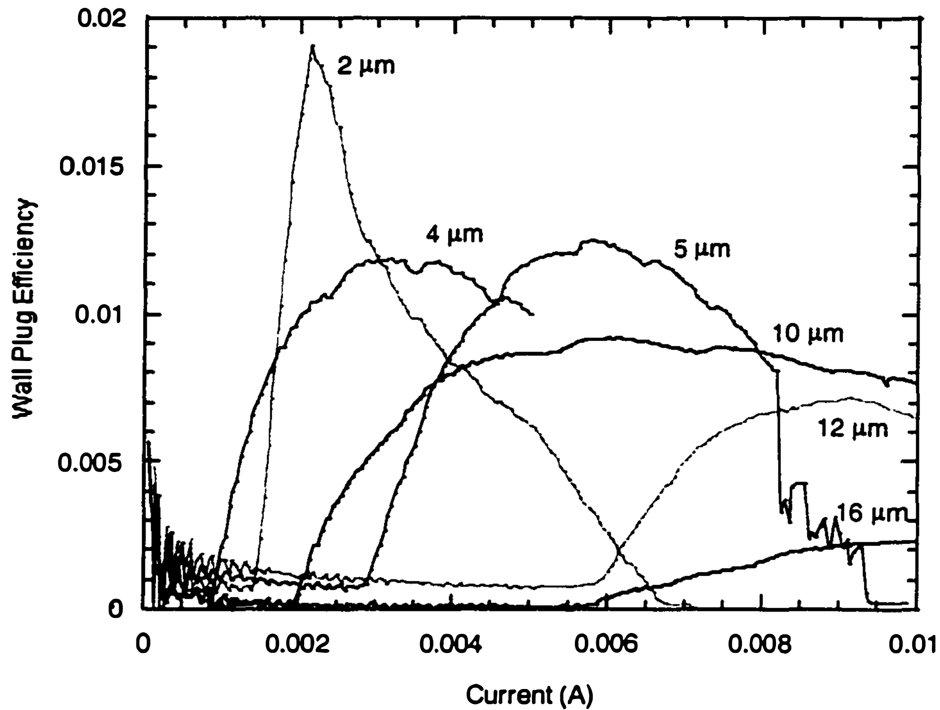


Figure 6.07 Plot of wall plug efficiency versus current for devices ranging in size from 2µm to16µm. The maximum wall plug efficiency is 1.8%.

The differential efficiency of both sets of lasers is also quite low. A plot of measured external efficiencies versus device size for generation 75 is shown in Figure 6.08. A maximum external efficiency of around 15% is measured for both a 12 µm and a 5 µm device. In general, however, there is no scaling of differential efficiency with size. This will prove important when trying to estimate the round trip loss in the structure. Differential efficiency will scale with device size if there are size dependent losses such as diffraction losses from the oxide aperture, or scattering losses of the sidewall of the pillar

in the etched pillar case. Because we see no trend with device size, we assume that the size dependent losses are negligible in our structure, mainly due to the low index perturbation of our aperture, placed close to the null in the standing wave, of $\Delta n = 0.02$.

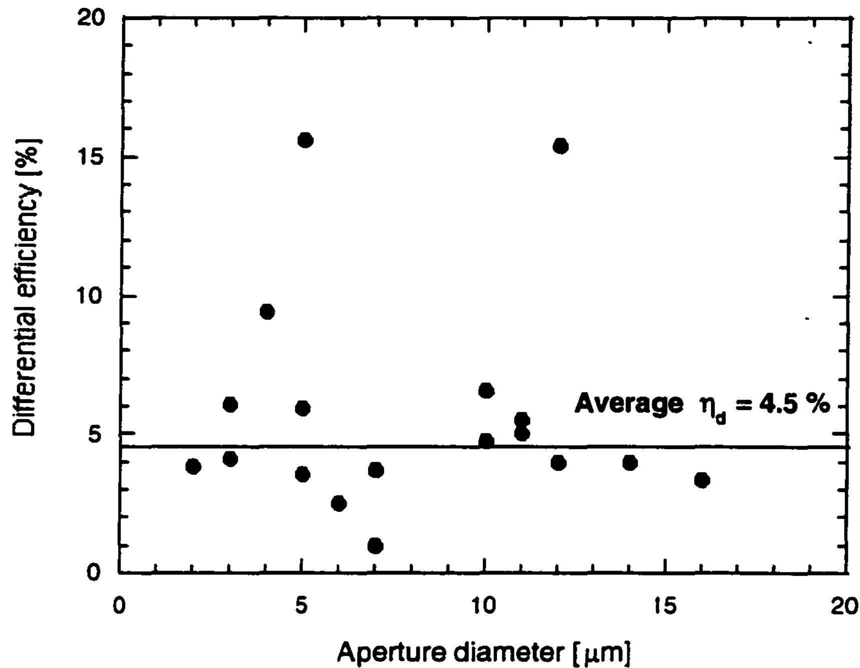


Figure 6.08 Differential efficiency of device generation 75 versus aperture opening. No scaling of differential efficiency is noted. It is concluded that size dependent losses are negligible in this structure.

In summary, the devices fabricated with this basic structure (runs 71 and 75) are the best performing devices fabricated in the course of this thesis. The high operating temperature, low threshold characteristics currently define the state of the art in the field. As indicated in Chapter 4, however, this design has pushed the limit on epilayer design and material properties. In order for the next breakthrough in device performance to be made, it has become necessary to fully understand the fused junction and the role it plays in device

performance. Although the superlattice structure and selective area fused channel aperture structure have not yet outperformed the basic design, the building blocks are here laid for this pursuit to continue.

6.01.2 Superlattice devices

The premise behind the superlattice structure is simple: the superlattice provides a defect blocking layer at the fused interface which acts not only as a barrier, but also as a gettering site for defects that would otherwise migrate towards and degrade the quality of the active region. It was shown in Chapter 3 that the benefit of the superlattice manifests itself in the form of improved luminescence, i.e. improved gain. The first two SL device generations were fabricated with 4 periods of 75 Å InP/ 75 Å 1.2 μm InGaAsP at the fusing surface. The SL was uniformly doped with Zn at a concentration of $1(10)^{18}/cm^3$. Because of the high doping in the absorptive quaternary layer, we wished to place the SL precisely at a null in the standing wave. Two SL periods were thus incorporated in the cladding, and two were grown on top of the 3/2λ cavity. Since the growths are normally short, we expected the cavity mode to be pushed to 1550 nm with the added layers. However, for this active region the calibration was precise, and the mode position was overshot, yielding a 25 nm mode gain offset in the "right" direction for high temperature performance. Because the gain curve is steep, an offset in this direction is more sensitive to temperature. A plot of the peak gain after single fusion as well as mode position is shown in Figure 6.09. The zero-gain offset is calculated to be 58° above room temperature. Assuming 30° heating in the active region at threshold (calculated in Section 6.2), the zero gain offset is expected to occur at a stage temperature of 53°C.

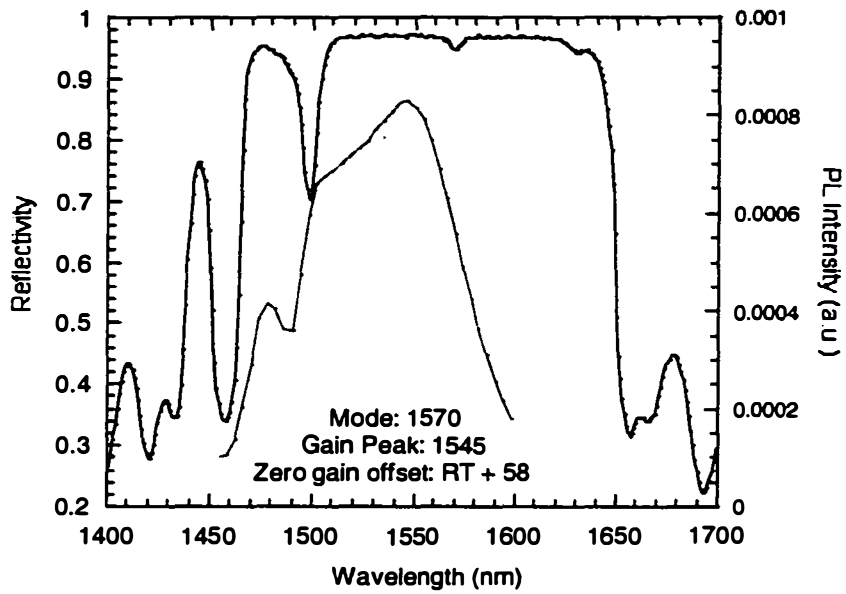


Figure 6.09 Plot of RT PL of the single fused active region and measured mode position after double fusion. The zero gain offset is calculated to be 83°C in the active region.

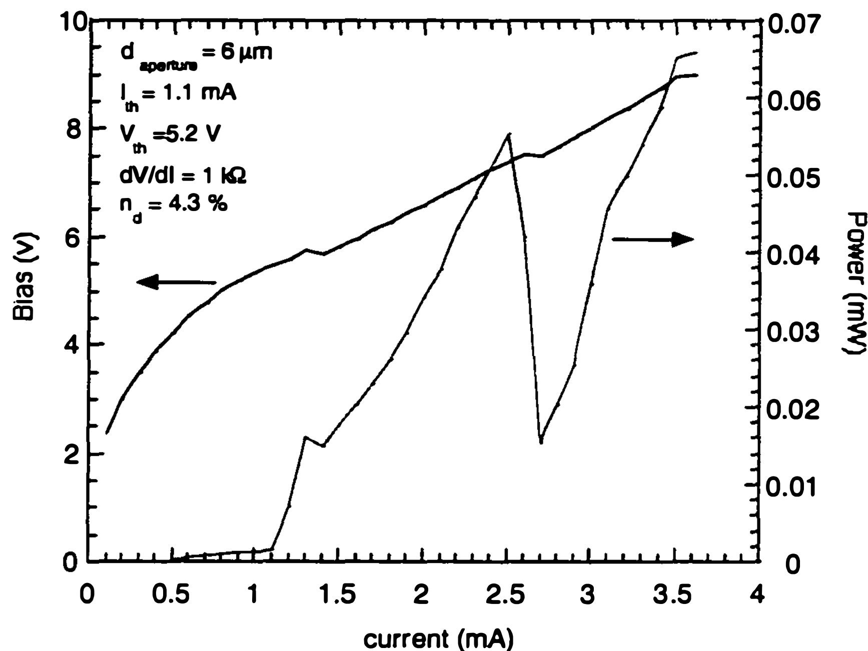


Figure 6.10 L-I-V characteristic of SL1. The aperture opening is 6 µm, the threshold current is 1.1 mA, and the threshold voltage is 5.2 V. The most alarming feature of this device is the differential resistance of 1kΩ, and a large kink in the light output.

A typical L-I-V characteristic from device SL1 is included in Figure 6.10. The device has an oxide aperture opening of 6 µm and operates at a threshold current of 1.1mA. This corresponds to an aperture current density of 3.9kA/cm^2. However, there are many problems with this device, most notably, the threshold voltage is 5.2 V and the differential resistance is 1 kΩ. Typically, fused VCLs operate at voltages between 2.5 and 3.5 volts and differential resistances of 200 Ohms. The obvious reason for the increased turn on voltage and resistance is the SL. Although the band offset is smaller, the SL acts much like a MQW region does to trap carriers. However, in the test fusions, the additional voltage drop attributed to the SL was on the order of

200 mV. The difference between the test I-V structures and the real sample was the doping profile. In the test structures, the quaternary layers were highly doped, to a level in excess of $5(10)^{18}/cm^3$. As explained in Chapters 2 and 3, diffusion of Zn during the fusion acts to intermix the interface region. Diffusion occurs as a result of both concentration and strain gradients. In the test structure, the dopant profile in the SL QWs and barriers acted to intermix the SL region, reducing the barriers and minimizing carrier trapping. In the actual sample, however, the doping was reduced to a constant doping of $1(10)^{18}/cm^3$ throughout the SL wells and quaternary barriers, in an effort to minimize free carrier absorption in the VCL. The increased electrical resistance can be explained by a combination of two effects. The defects trapped in the SL act to increase the resistance of the structure. In addition, the constant doping profile in the InGaAsP/InP layers provides no concentration gradient to promote the diffusion of zinc through the SL region, leaving the SL wells and barriers essentially intact, ready to impede transport of carriers. Besides the different doping profile, the reduced doping level could possibly be below the critical concentration needed for enough diffusion to occur. It important to note, however, that *despite* the large amounts of power dissipated in the active region as a result of the high voltage, these devices operated at very low threshold currents, perhaps a testament to the increased gain in the MQW active region as a result of the SL barrier.

In order to minimize the resistance across the SL layer, the third generation of SL VCLs was designed with but one period of superlattice. A 75Å 1.3 μm InGaAsP layer with maximum achievable doping of $5(10)^{18}/cm^3$ was placed 75Å from the fusing surface, in effect reproducing the dopant supplying layer that demonstrated low resistance conduction across the fused interface in Chapter 3. The temperature dependent L-I-V characteristic from a 1 μm oxide aperture device of this set is shown in Figure 6.11.

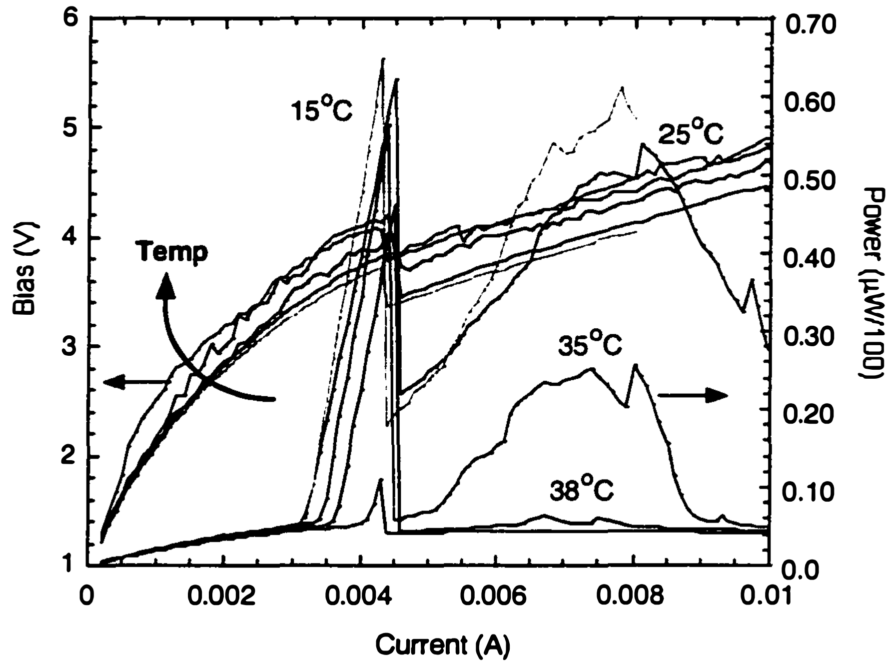


Figure 6.11 L-I-V characteristic from a 1 μm oxide aperture device from generation SL3.

One 75Å dopant supplying InGaAsP layer is incorporated into the active region, 75Å removed from the fused interface. The threshold current is 3.1 mA and the threshold voltage 3.25V. As the temperature is increased, the voltage is also *increased*, contrary to the normal decrease in voltage with temperature.

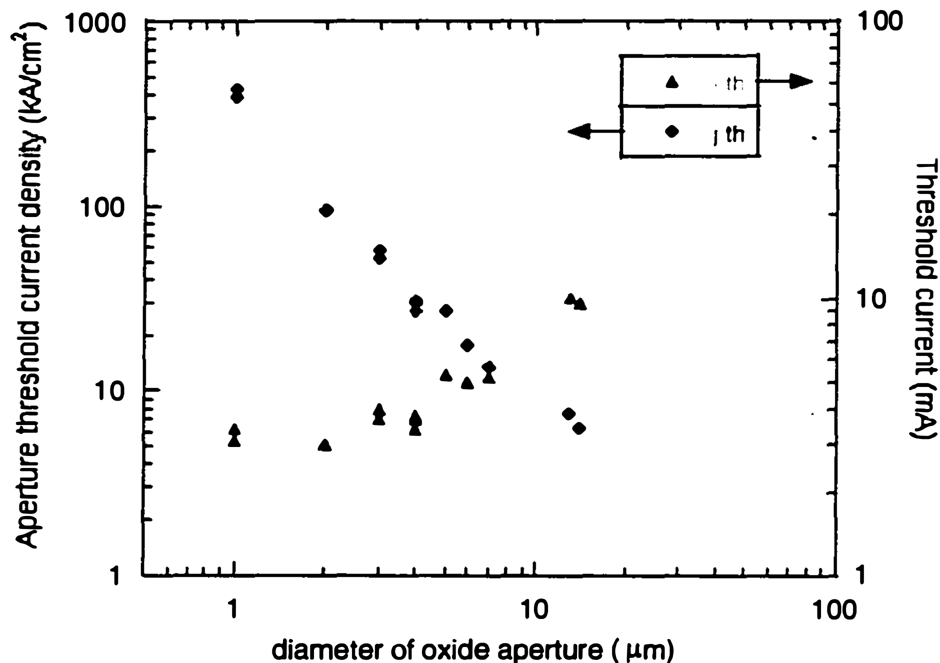


Figure 6.12 Threshold current scaling for device SL3, showing slightly larger threshold currents than devices 71 and 75. The unrealistic aperture current densities are an indication that large amounts of current spreading is occurring as a result of the gas source carbon modulation doping profile.

The differential resistance of these devices is back to an acceptable level- 300 Ohms. The threshold current is 3.1 mA and the threshold voltage 3.25 V. Once again, large kinks in the L-I-V are noted. A discussion of these kinks will be given in the next section. The calculated aperture current density using these numbers is 394 kA/cm^2, clearly an outrageous number, and two orders of magnitude higher than usual for these devices. A plot of threshold current and aperture current density versus aperture diameter is shown in Figure 6.12.

Standard calculations of aperture current density yield approximations for aperture threshold current densities in excess of 300 kA/cm^2. Such a

current density could not be supported by the active region. Assuming a more reasonable yet high current density of 10 kA/cm^2 would mean current spreading under the aperture of 2.5 μm. This large spreading can be attributed to the doping profile in the GaAs mirror, and is substantiated by the fact that the voltage characteristic of the device has an abnormal temperature behavior: the voltage increases with temperature. Figure 6.13 shows a more typical I-V characteristic dependence on temperature. This particular curve is for device generation 71, but is the same for all devices *not* fabricated with the gas source carbon mirror.

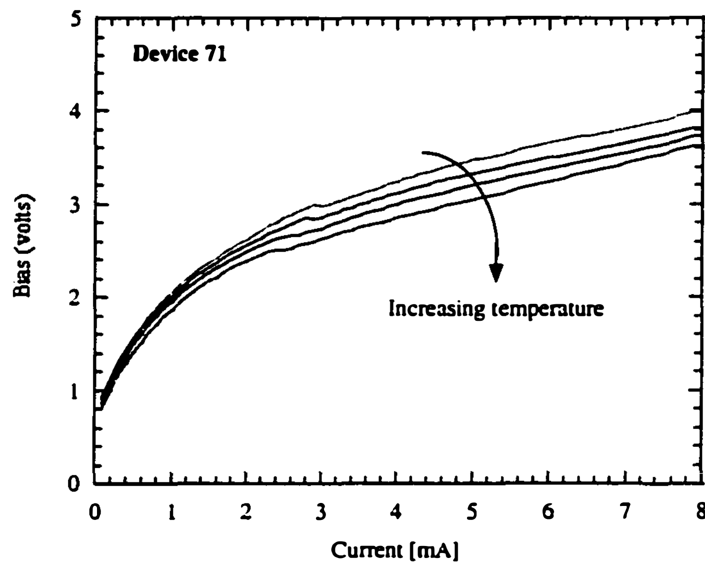


Figure 6.13 I-V curves as a function of temperature characteristic of all devices not fabricated with the gas source carbon doping.

As discussed in Chapter 4, in order to achieve low doping of the mirror periods close to the active region using gas source carbon, modulation doping is used. The lateral mobility of carriers in these layers is high, on the order of 250 cm^2/Vs. As the temperature is increased in a normal structure, the average kinetic energy of the carriers is also increased, and current is passed at lower

applied voltages. This results in a decrease in voltage with increase in temperature. The actual dependence of voltage on temperature is more complicated, however. The decreased voltage effect is countered in the gas source carbon structure by the effect of decreased mobility of carriers at higher temperatures. Resistance is inversely proportional to mobility and area. At higher temperatures, in the case of the gas source carbon mirror, the in plane mobility of the carriers is reduced, reducing current spreading in those layers. In turn, the actual area through which current is passed in decreased, increasing the resistance at a given bias through the structure. In the normal structure, such a high in-plane mobility is not as great an issue, so the effect of temperature on mobility is dwarfed by the increased kinetic energy of carriers at elevated temperatures.

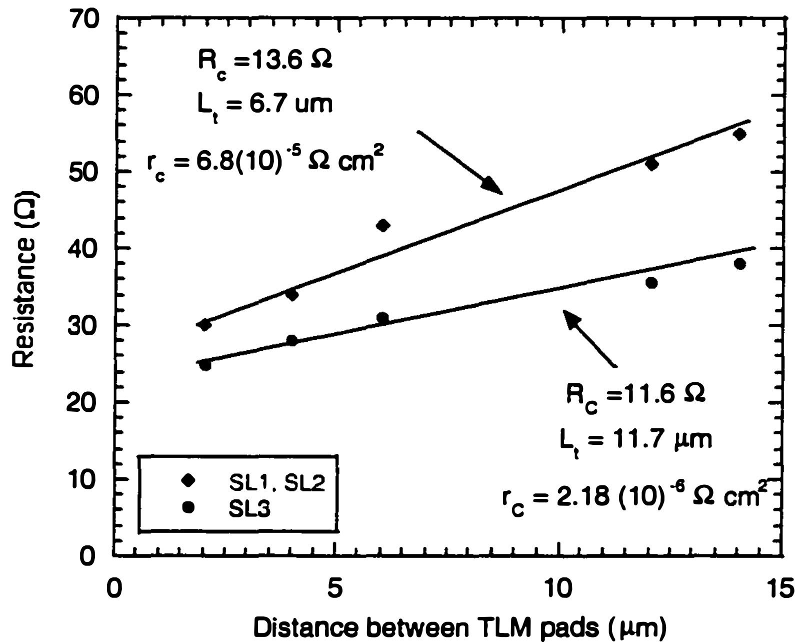


Figure 6.14 Comparison of contact resistances between SL1 and SL3. The difference can be attributed to a modified surface clean before metal evaporation in which both GaAs and AlAs oxides are removed, respectively.

It is especially important to look at the contact resistance of the p-contact in order to determine the portion of operating voltage that can be attributed to the contact. Many changes in the device process were made to minimize this resistance. A comparison of contact resistances for the SL generation of devices is shown in Figure 6.14. SL1 and SL2 suffered from poor contact resistances on the order of $7(10)^{-5}$ Ωcm^2. Some of the improvements in device performance from SL3 can be attributed to the better contact resistance achieved using the combination of acid dips before metal evaporation as described in Chapter 5. The p-contact resistance for generation SL3 is $2(10)^{-6}$ Ωcm^2, nearly ohmic.

While the first generations of SL VCSELs did not outperform the basic design generations, the initial results look promising. The persistence of low threshold devices despite high voltage drops across the interface is substantial evidence that the SL defect gettering layer is effective in improving the gain of the MQW region. Unfortunately, the benefits of incorporating of a dopant supplying SL in generation SL3 are unable to be decoupled from the poor mirror doping/design. The obvious direction for this approach is to couple a SL/ dopant-supplying layer with a solid source carbon doped mirror.

6.01.3 Selective area fusion, under-etched active region devices

The first and only set of devices fabricated by selective area fusion operated in pulsed current injection mode only. The L-I-V characteristic from a 1% duty cycle for pulse widths of 10 μs and 1 μs is shown in Figure 6.15. It is obvious that excessive heating occurs at pulse widths in excess of 1 μs. Shorter pulses could be used, and give "better" L-I-V characteristics, but due to the characteristic rise in output power at the beginning of the pulse, it is believed that the integrity of the measurement is unduly compromised. A

spectra showing single mode behavior of a 45 μm pillar diameter, 6 μm under-etched active region diameter is included in Figure 6.16.

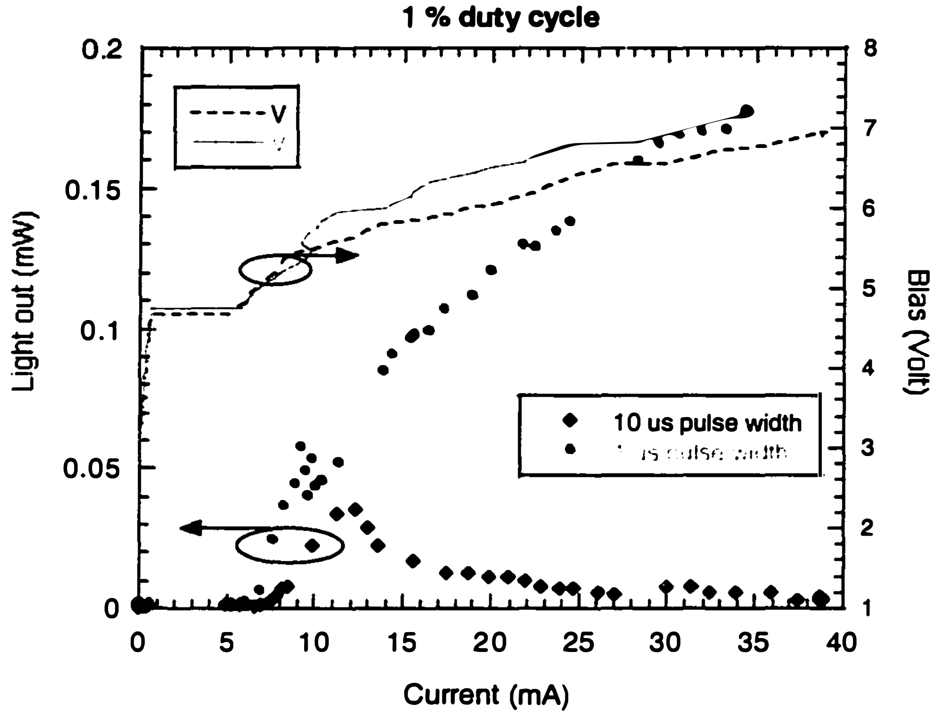


Figure 6.15 L-I-V characteristic of a channel apertured, underetched active region device. The device shows excessive heating under 10μs pulse widths. The threshold current is 7mA; the threshold voltage is 4.9V.

The poor performance of these lasers can be attributed to two factors: poor heat conduction away from the active region resulting from the air aperture and deformation of the mirrors in the selective area fusion. The conduction of heat away from the active device area is essential to CW operation and stable lasing. The thermal conductivity of InP 0.68 W/cmK, as compared to for .0003 W/cmK for still air. The vertical management of heat will have to compensate for these apertures, or the channels could be filled

(taking advantage of their capillary nature) with a better heat conductor post processing. At present, the thermal management issues in this device structure remain unresolved.

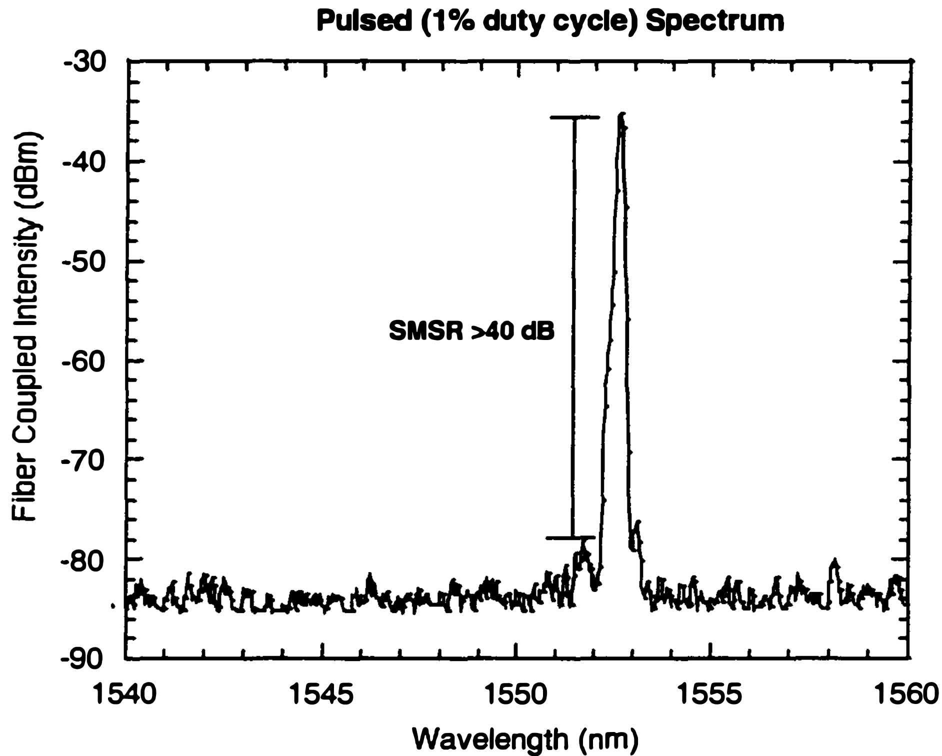


Figure 6.16 Spectrum of 6 μm diameter under-etched active region, selective area fused device showing high side mode suppression of greater than 40 dB under pulsed operation.

Perhaps the larger contributor to the relatively poor performance of these lasers is found in an examination of the processed laser structure itself. Figure 6.17 shows two cross-sectional SEMs of the finished device. Figure 6.17 (a) clearly shows cleave damage at the base of the locally fused region. This is not surprising as cleave damage occurs anywhere in the structure where there is excess stress that can be relieved. The fused interface provides this

stress in the locally fused area. Another example of this was made in Chapter 5 where the stress at the forming oxidation front is marked by characteristic cleave damage. More significant to device performance is the close-up of the mirror in the region below the localized fusion, Figure 6.17 (b). The mirror periods are blurred, indicating that their integrity has been compromised. Similar intermixing was shown in the dissertation of Babic in the event that particles were caught at the fused interface[5]. Surface aberrations such as particles or patterned surfaces may result in increased stress at the edges of the mesas. Mesas are always present in the fusion, as channels are always used. TEMs in the region of the channels indicate larger dislocation densities in that region, in part because of localized stress[6]. This effect is magnified with smaller mesas. An interesting thing to note is that this deformation of the mirror occurs only during the second fusion (to the nid mirror). The only difference between the fusions is that during the first fusion a GaAs substrate is being fused to an InP substrate; during the second fusion two GaAs substrates are being fused- both substrates are stiff. It is unclear whether the deformation is contained in the area at the perimeter of the mesa, or throughout the locally fused area. There is no doubt, however, that the blurred mirror would increase the loss in the structure significantly, and thereby increase the threshold gain, explaining the relatively poor performance (as compared to both the basic and SL designs) of this structure. However, with upwards of 20 individual efforts around the world investigating long wavelength VCL structures, the performance of this laser is still impressive, especially for the first attempt at this structure. The obvious direction for this research approach is reduced applied pressure during the second fusion. As stated before, the second fusion is easier relative to the first, and as such there is more leeway in the choice of fusion conditions.

Figure 6.17 Cross-sectional SEM of selective area fused, under-etched active region device that operated in pulsed mode only. (a) Shows cleave damage associated with localized stress in the fused areas. (b) Shows actual intermixing and material degradation in the mirror below the active region. It is unclear if this blurred region is only at the perimeter of the device.

6.02 Round trip loss

In order to better compare the device runs, a summary of estimated round trip loss is performed on the device generations. Tables 6.1 and 6.2 estimate the round trip *absorptive* loss in each structure. The material used for each device run is similar, with the exception of the higher doping in mirror 24.5C, and the superlattices. Table 6.1 summarizes the absorptive round trip

loss in the basic structure; table 6.1 estimates the additional and total loss contributed to the devices from the different mirror and incorporation of superlattices.

Table 6.1 Estimate of absorptive losses in the basic structure.

Region	Material/doping [atoms/cm^3]	Length of interaction [nm]	Absorptive loss [cm^{-1}]	Percent Loss[%] Round-trip
nid-mirror	AlAs/GaAs nid	780	2	0.03
n-cladding	InP 5 10^{18}	300	25	0.15
MQW	InGaAsP nid	175*	50	0.17
p-cladding	InP 1 10^{18}	200[1]	15	0.06
p-mirror	$Al_{0.9}Ga_{0.1}As/GaAs$ 2.25 10^{17}	900	5.6	0.1
Total				**0.51**

Table 6.2. Estimate of additional absorptive losses contributed by changes in device structure.

Region	Material/doping [atoms /cm^{-3}]	Length of interaction[nm]	Absorptive loss [cm^{-1}]	Percent Loss[%] Round-trip
InGaAsP SL 4 periods	5 10^{18}	1.5[2]	250	0.008
Total (SL1, SL2)				**0.52**
p-mirror	$Al_{0.9}Ga_{0.1}As/GaAs$ 4 10^{17}	900	10	0.18
Total (SL3)				**0.59**

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* actual MQW thickness ~1000 nm, but is multiplied by gain enhancement factor.

[1] P-cladding is 3000Å, but only 2000Å is doped due to a 1000Å doping setback layer.

[2] Because the SL is intended to be placed at a null, the actual interaction is found by taking 30nm of InGaAsP SL material and dividing by the loss reduction factor.

In order to calculate the round trip gain and loss from the device runs, it is necessary to measure both the injection efficiency and the differential efficiency of the devices. The injection efficiency was measured according to a method devised by Margalit[7]. Because no size dependent loss was found for any of the device generations, the average differential efficiency for each device run is used. In the under-etched aperture structure, no size dependent loss was found because the aperture sizes were all 6 μm. Table 6.3 compares the overall performance of the device runs, and calculates the threshold gain and round trip loss for each generation.

Table 6.3 Summary of device performance and estimate of threshold gain and round trip loss.

Generation:	71	75	SL3	SAF
p-mirror	25.5A	25.5B	24.5C	25.5B
n-mirror	31A	31A	31A	31A
mode	1507 nm	1515 nm	1530 nm	1550 nm
PL peak	1542 nm	1545 nm	1550 nm	1550 nm
Oxide depth	18 μm	20 μm	22.5 μm	Various
Max. CW temperature	71°C	74°C	38°C	pulsed
V_{th}	2.1V	3V	3.2V	5.3V
Minimum I_{th}	1.5 mA	0.8 mA	3 mA	9 mA
Best CW output power	850W	500μW	200μW	200μW (pulsed)
Typical CW output power	300μW	400μW	50μW	200μW
Transmission	0.115%	0.115%	0.15%	0.115%
Internal efficiency η_i	40%	40%	35%	60%
External efficiency η_e	5.6%	4.5%	4.75%	1.75%
$G_{th} = L + T = \eta_i/\eta_e * T$	**0.8%**	**1%**	**1.1%**	**3.9%**
Round trip Loss	**0.7%**	**0.9%**	**0.95%**	**3.8%**

6.03 Thermal performance

The high temperature performance of long wavelength VCLs is of great importance if these devices are to be considered for telecommunication and datacom applications. In addition to the temperature dependence of free carrier absorption, Auger recombination and intra-valence band absorption are also extremely sensitive to temperature. In this next section, both the characteristic temperature and the thermal resistance of the structure will be analyzed to give insight to the overall temperature sensitivity of the double fused structure.

6.03.1 Characteristic temperature

To analyze the temperature sensitivity of the double fused structure, the dependence of threshold current on temperature was measured over a broad temperature range for all generations of devices. Figure 6.18 illustrates this dependence over a temperature range spanning from -190°C to the highest CW operating temperatures achieved, i.e. 38°C for the SL3 structure and 71°C for device 71. A record characteristic temperature of 132K is measured in the temperature range from -75°C to 35°C for device 71. This exceeds the best reported value of 95K for InGaAlAs/InP 1.55μm Fabry-Perot lasers [8] and the more typical values reported for InGaAsP 1.55μm lasers that fall in the 60 to 70 K range. When measured in pulsed mode, however, the characteristic temperature of device 71 is only 90K. This is an indication that the additional heating of the device under CW operation acts to decrease the temperature sensitivity of the device, perhaps by reducing the spreading of current under the oxide aperture. Once again, the explanation for this lies in the inverse relation of carrier mobility to temperature. Either way, the CW characteristic temperature is valid. Just as there are many contributing factors to the increase

in threshold current with temperature, it is equally valid to include current spreading (effectively internal efficiency) into the calculation of T_o.

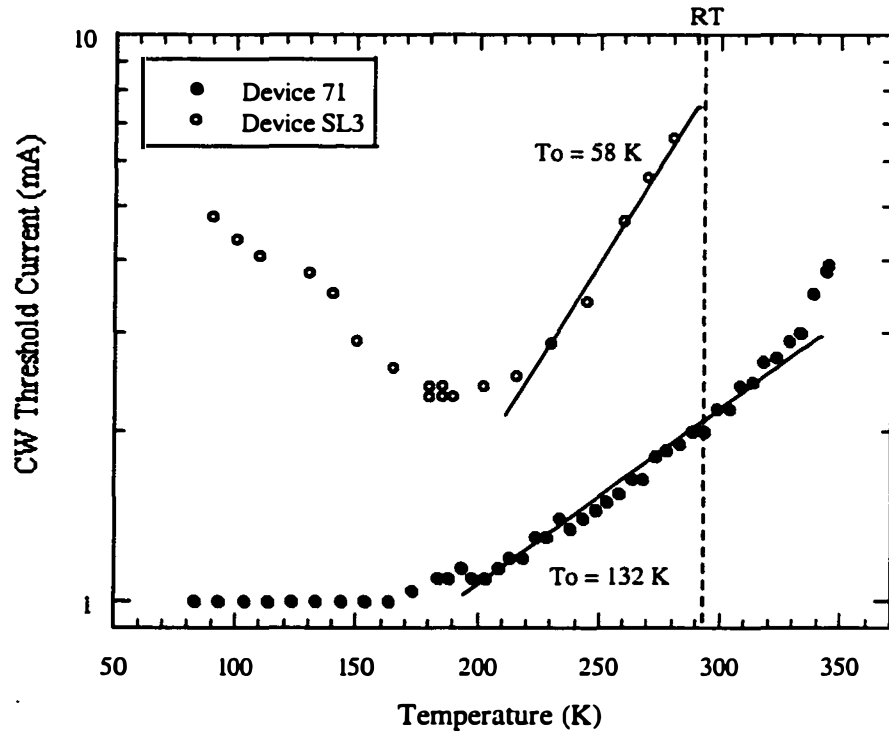

Figure 6.18 Characteristic temperature as measures by the sensitivity of threshold current to temperature for devices 71 and SL3. The characteristic temperatures calculated are 132K and 58K, respectively.

The SL3 structure is more sensitive to temperature than device 71. This is apparent first of all through the lower maximum operating temperature. Also, the threshold current is more dependent on temperature, as indicated in Figure 6.18. A characteristic temperature of 58K is reported. Calculations of zero mode gain offset are 220K for device 71 and 251K for device SL3. A more interesting feature to note is the expected offset for low threshold operation when the mode is 30 nm shorter than the gain peak. This corresponds to 150K for Device 71 and 181K for device SL3. Indeed, we see a clear minimum threshold current at 181K for SL3, but no absolute minimum is

reported for device 71. Instead, the tendency is a constant threshold for lower temperatures. Explanations for this may reside in either a very broad gain spectrum or measurement due to cooling problems in our cryostat. The measurements on SL3 were performed at conductus[9].

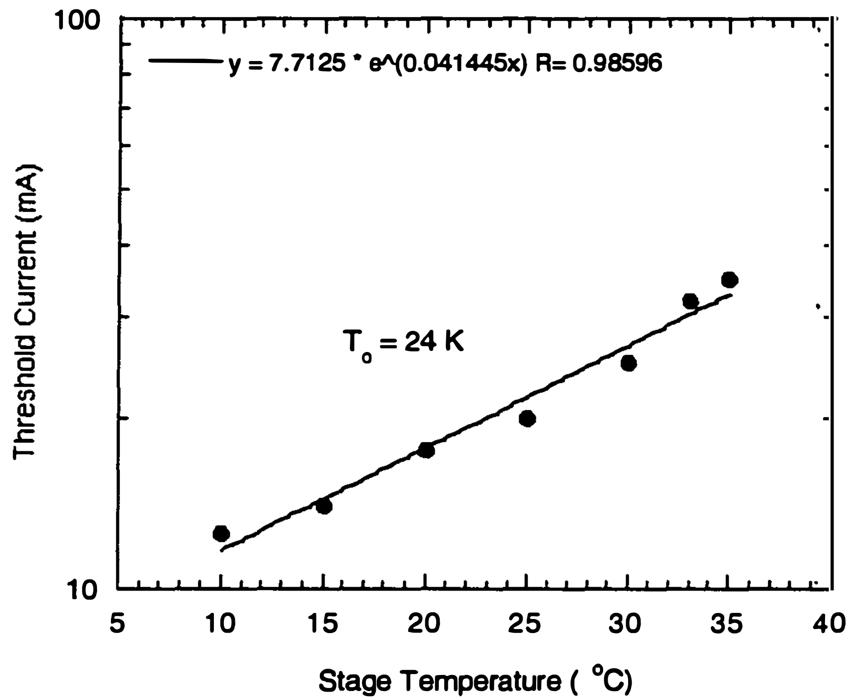

Figure 6.19 Temperature sensitivity of SAF, under-etched active region device. A characteristic temperature of 24K is reported.

The characteristic temperature of the selective area fused device with an under-etched active region is shown in Figure 6.19. A characteristic temperature of 24K is reported. This is consistent with the fact that these devices operate in pulsed mode only, and is possibly attributed to the poor thermal conductivity of air in the current confining channel. In addition, deformation of the mirror under the localized fusion would contribute to phonon scattering and reduced thermal conductivity.

6.03.2 *Thermal management*

The active region of a device operates at considerably higher temperatures than the stage temperature. The heating in the device is found by taking the product of the thermal resistance of the device and the power dissipated:

$$\Delta T = P_D \cdot Z_T \qquad (6.1)$$

where P_D is the dissipated power and Z_T is the thermal impedance of the device. The thermal impedance of the device is found by considering the three dimensional heat flow in the device. For the case of a small diameter VCL, the heat flow can be vaguely approximated by a disk sitting on top of an ideal heat sink, the GaAs substrate. The expression for thermal impedance, Z_T, is then:

$$Z_T = \frac{1}{2\kappa d} \qquad (6.2)$$

where k is the thermal conductivity and d is the diameter of the device. A discussion of thermal conductivities in GaAs/AlAs DBRs is given in chapter 1. It is known that although the thermal conductivity of GaAs is ~ 0.45 W/cm°C, and the thermal conductivity of AlAs is 0.9 W/cm°C, the thermal conductivity of DBRs is reduced due to interface scattering of phonons.

In order to better understand the temperature performance and limitations of our devices, the thermal impedance was measured by two separate methods. The first, more traditional method examines the *pulsed* lasing mode shift in wavelength with temperature. Increasing temperature affects both the index and the optical path length of the cavity. A precise measurement of the shift of wavelength with both temperature and dissipated power allows one to calculate the temperature rise associated with power dissipated the thermal resistance.

$$Z_T = \frac{\partial T}{\partial \lambda} \cdot \frac{\partial \lambda}{\partial P_D} = \frac{\partial T}{\partial P_D} \qquad (6.3)$$

A plot of the pulsed shift of wavelength with temperature is given in Figure 6.20. All active regions used in this thesis are of similar composition and displayed similar wavelength shifts with temperature for same size devices- the measured shift is 0.08 nm/K.

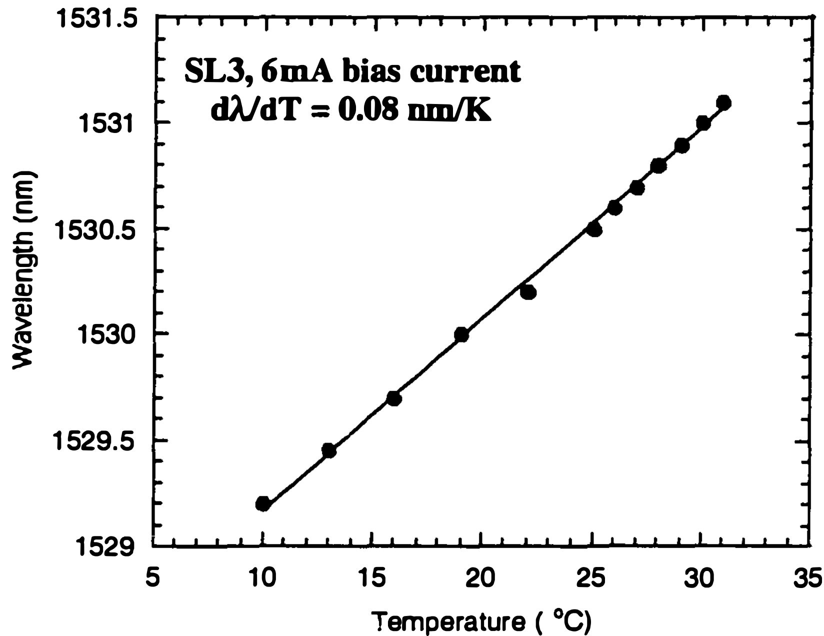

Figure 6.20 Wavelength shift of SL3 with stage temperature. A shift of – 0.08nm/K is recorded. The same shift is measured for all device generations.

Knowing the wavelength shift with bias current allows one to calculate the wavelength shift with dissipated power. A plot of change in wavelength versus dissipated power is provided in Figure 6.21. The shift is 0.101nm/mW for the 4μm aperture diameter device and 0.103 nm/mW for the 1 μm aperture diameter device. This corresponds to a thermal resistance of 1.2°C/mW, and a calculated thermal conductivity of 1mW/cm°C, an order of magnitude larger than expected.

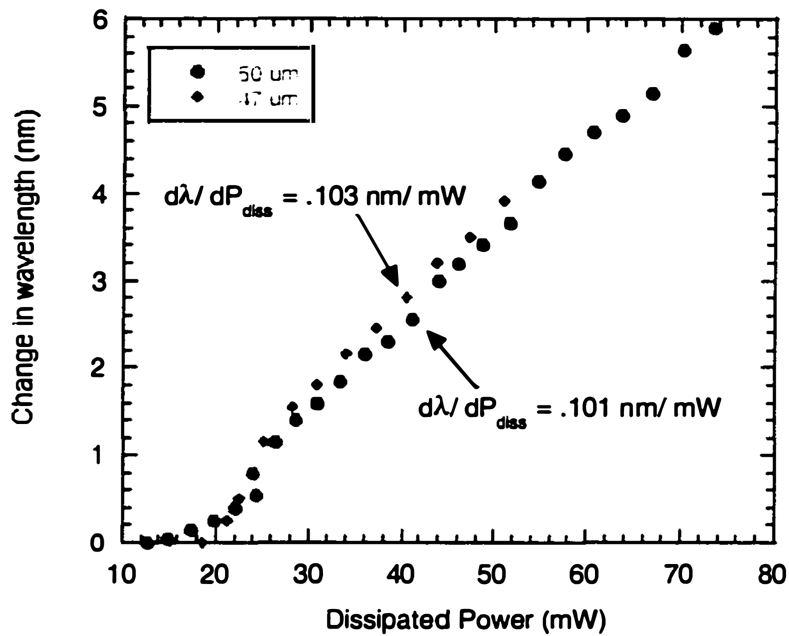

Figure 6.21 Measured change in wavelength versus dissipated power.

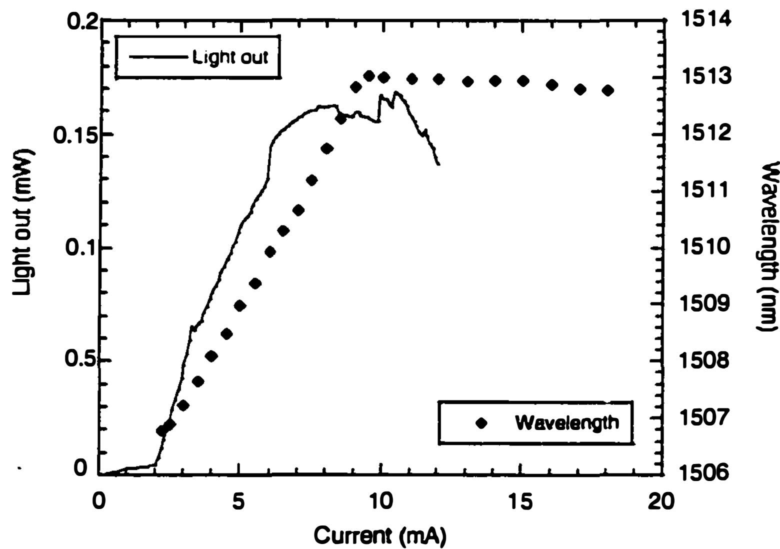

Figure 6.22 Plot of wavelength versus bias current for a device on the 71 set. Superimposed is the L-I of the device showing the point at which the wavelength ceases to shift corresponds with rollover in the device.

The change in wavelength versus bias current is shown in Figure 6.22. Superimposed on this plot is the L-I characteristic from a device on set 71 for which the spectral change was measured. It is interesting to note that at the point of thermal rollover in the L-I, the wavelength ceases to shift. All excess power is dissipated as electrical power, however, this should still cause a temperature rise in the active region as well as a corresponding wavelength shift. The origin of this phenomenon remains a mystery. Noting that the point at which the L-I curve hits the current axis after rollover is the point at which all power dissipated in the structure is electrical, one can plot this power versus temperature to disclose the thermal resistivity and maximum pulsed operating temperature of the device. Such a plot is shown for the actual 71 degree device in Figure 6.23. The second method of determining thermal resistance is shown here, simply by taking the inverse of the line fit to the rollover power versus temperature. This method assumes that the maximum operating temperature of the device is constant. A thermal resistance of .91°C/mW is measured, slightly higher than for the previous device from the same set for which the spectrum was measured. Indeed, this 71 degree device was the best on the wafer. The maximum pulsed operating temperature can be speculated by the intersection of the fit to the electrical dissipation with the current axis. For this device, the plot predicts a maximum pulsed operating temperature of 91°C. Actual measurements revealed a maximum pulsed operating temperature of 88°C, in excellent agreement with this analysis.

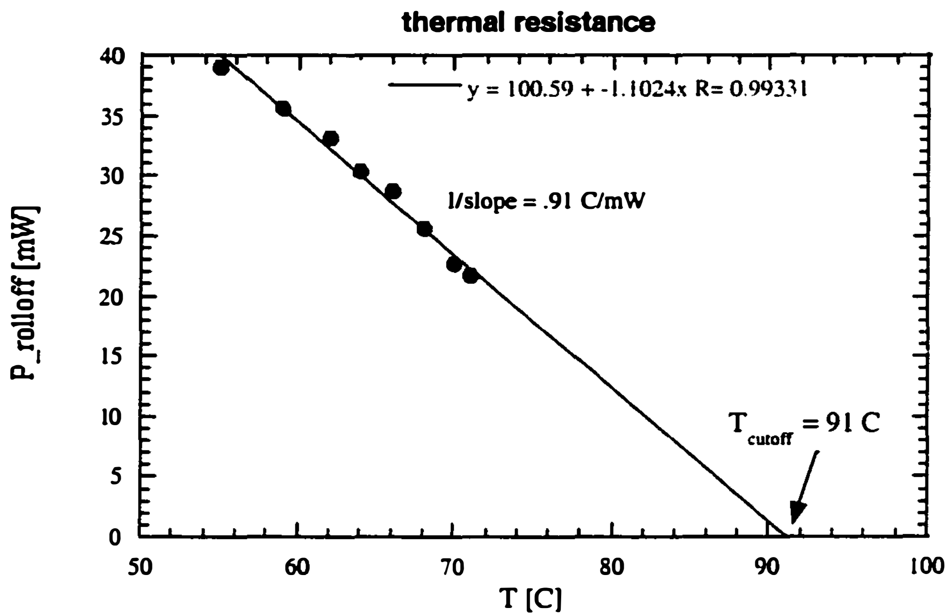

Figure 6.23 Plot of electrical power dissipation at complete rollover versus temperature. The point of intersection of the rollover versus temperature indicated the maximum pulsed operating temperature of the device.

Knowledge of the thermal resistance leads to an understanding of the temperature in the active region of the operating device. A plot of the internal device temperature is included in Figure 6.24. An ambient temperature of 20°C is chosen. Rollover of the L-I characteristic begins when the internal device temperature is 50°C. The effect of temperature on long wavelength materials systems is harsh. The terminal current to a device has many components that do not contribute directly to the lasing mode of the device. These components include current contributing to spontaneous emission, Shockley Reed Hall recombination, Auger recombination, and leakage currents, both lateral and vertical. A simulation by J. Piprek and included as Figure 6.24, of a previous generation of long wavelength VCSELs (fabricated by Babic) reveals the largest *temperature dependent* contributor to stray

current is Auger recombination[10]. This temperature sensitivity of non-radiative recombination processes manifests itself in the differential efficiency of the devices. A plot of differential efficiency versus temperature for the 71 degree device is given in Figure 6.26.

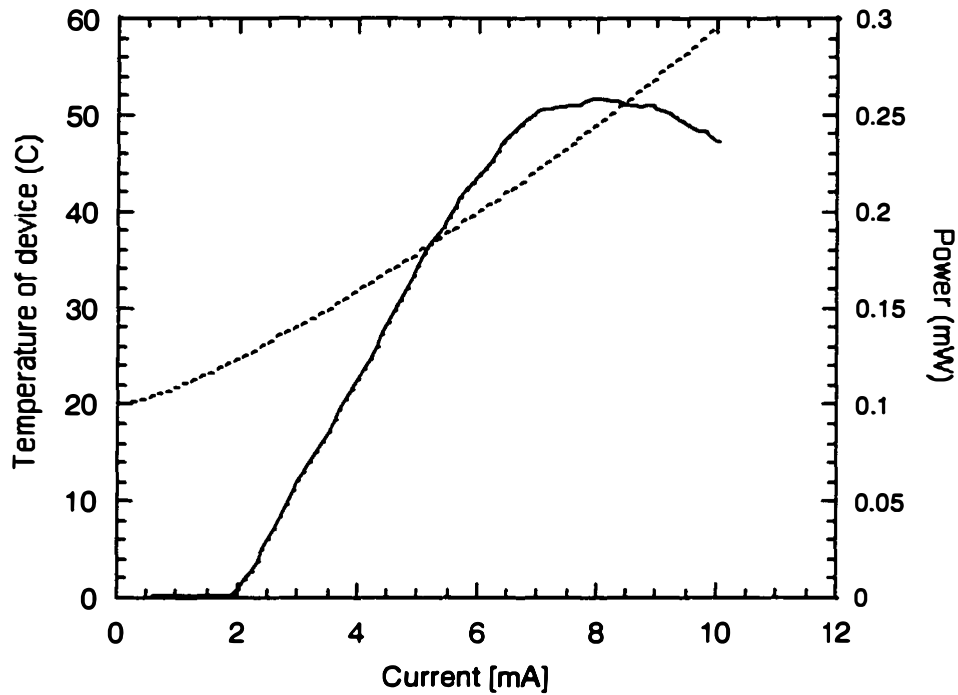

Figure 6.24 Plot of internal device temperature versus bias current overlain upon the actual L-I characteristic.

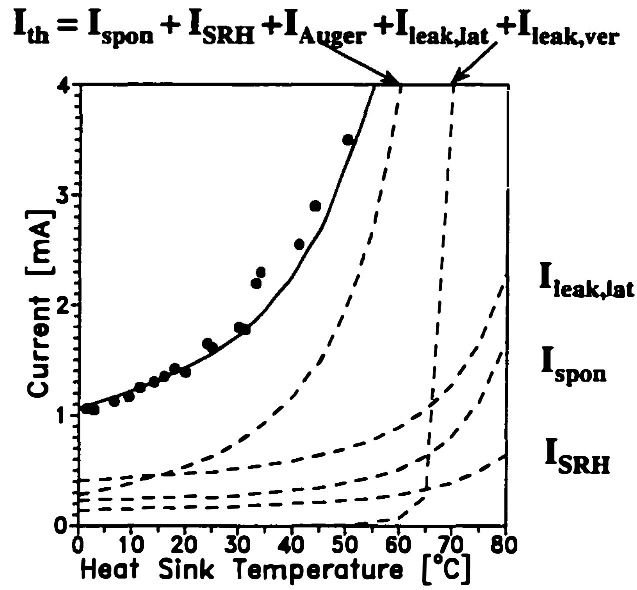

Figure 6.25 Temperature dependent contribution of various current paths to the threshold current of a device. At high temperatures, Auger recombination is the largest contributor to stray current.

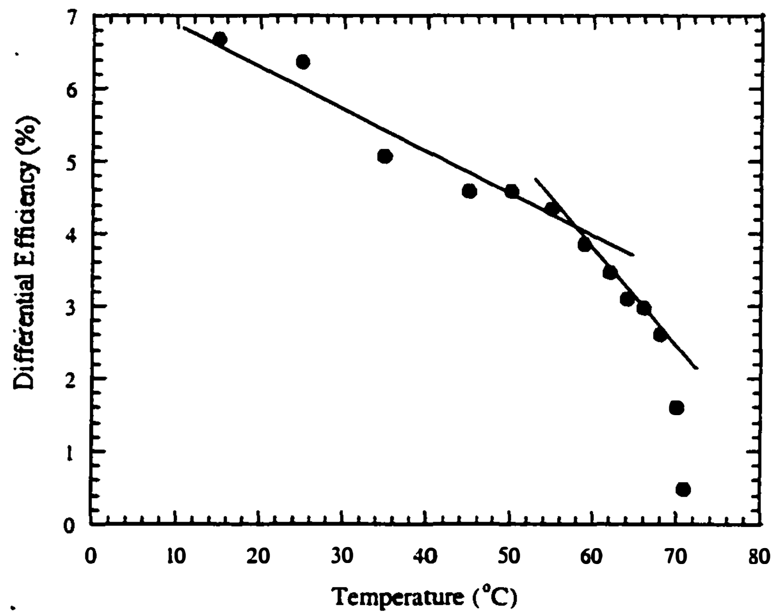

Figure 6.26 Temperature dependence of differential efficiency.

6.04 Limits to device performance: the kink

Ubiquitous to fused VCLs is the presence the kink in the L-I-V. As described in Chapter 3, the kink arises from the presence of n-type traps at the p-p fused interface, which in conjunction with the active region diode yields a thyristor type effect. Chapter 3 explored the electrical nature of the kink at length. This section attempts to look at the effect of the kink on the VCL performance and reliability.

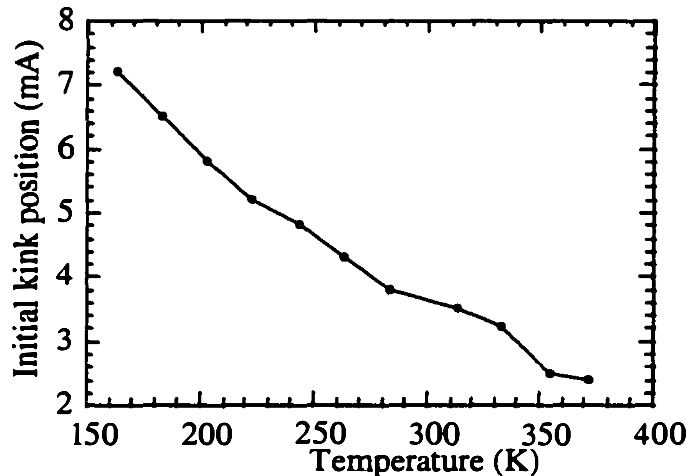

Figure 6.27 Kink position in mA as a function of stage temperature. The kink occurs at smaller bias with increasing temperature. No activation energy associated with the kink position could be derived.

The dependence of kink position in mA on stage temperature is noted in Figure 6.27. The kink occurs at smaller applied bias with increasing temperature. The dependence did not lend itself to fitting, nor could an activation energy be derived. However, the general trend can be attributed to increased leakage of carriers out of the active region due to higher kinetic energy afforded by the stage temperature increase. Perhaps the most significant observation is the effect the temperature dependence of the kink has

on laser reliability. As the temperature is raised, the kink moves lower in current. When the kink hits threshold, a shunt current path is created around the active region diode, and it becomes nearly impossible for the active region to support the carrier density necessary for lasing.

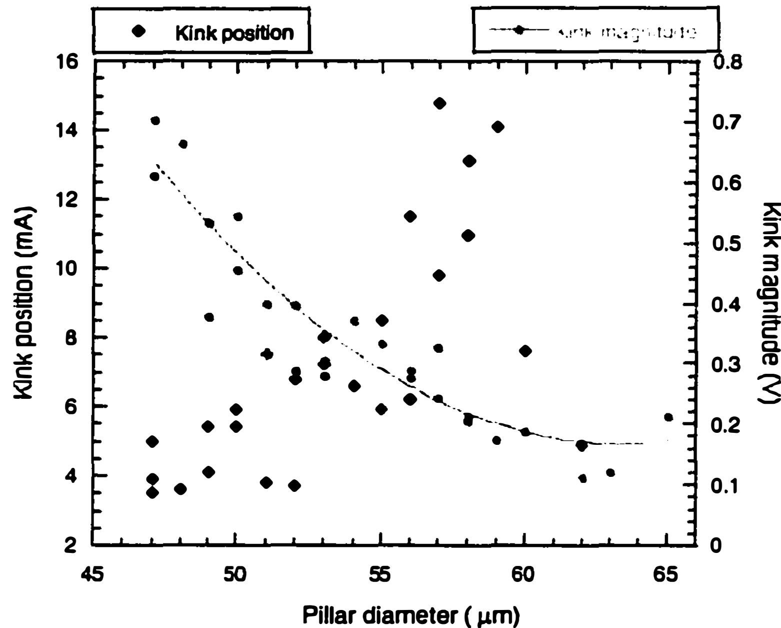

Figure 6.28 Position of kink in mA and magnitude of kink in Volts versus pillar diameter. Line drawn to guide the eye.

The dependence of kink position and magnitude on pillar diameter is described in Figure 6.28. The magnitude of the kink refers to the magnitude of the voltage drop at the kink bias. The kink position once again refers to the applied bias in mA at which the kink first appears. As should be evident in any of the L-I-V curves shown in this chapter, there can be more than one kink in a given structure. The dependencies derived from this are once again general. Without proper knowledge of current spreading under the oxide aperture, little can be said about kink position versus current density. However, it is noted that as the pillar diameter is increased, the position of the

kink in mA increases and shrinks in magnitude. The presence of multiple kinks in a given L-I-V is indicative of capacitor-type action, whereby a voltage is built up and discharged repeatedly.

Perhaps the most interesting feature associated with the kink is the effect of the kink on the near field pattern of the device. Figure 6.29 is an image taken with an infrared camera of the fundamental mode of a device biased below the initial kink position. The mode pattern is stable at a given bias current for both single and multi-mode devices. Once the laser is brought above threshold, however, the mode oscillates between the fundamental and various higher order modes with no apparent pattern established, and no change in bias current. The period between mode shifts is on the order of two seconds, corresponding in nature to the time scale of thermal effects. The wavelength of emission is precisely monitored, however, and the stage temperature controlled, and does not indicate thermal mischief. Most likely the mode shifting is a consequence of spatial hole burning that results from non-uniform current injection across the fused barrier after the p-n-p-n junction has been turned on. Shunt current paths across the junction will lead to gain compression in localized areas of the device. Figure 6.30 shows three near field images taken at different times at the same bias current above the kink. The time varying near field is clear.

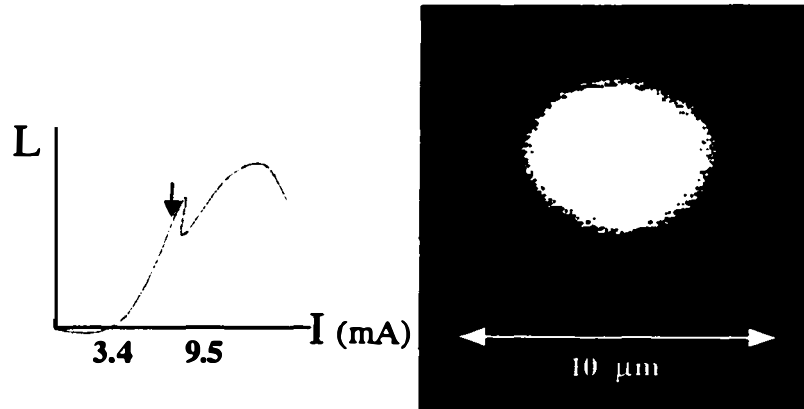

Figure 6.29 Near field image of a device biased above threshold but below the initial kink current. The near field pattern is stable and shows the fundamental gaussian mode.

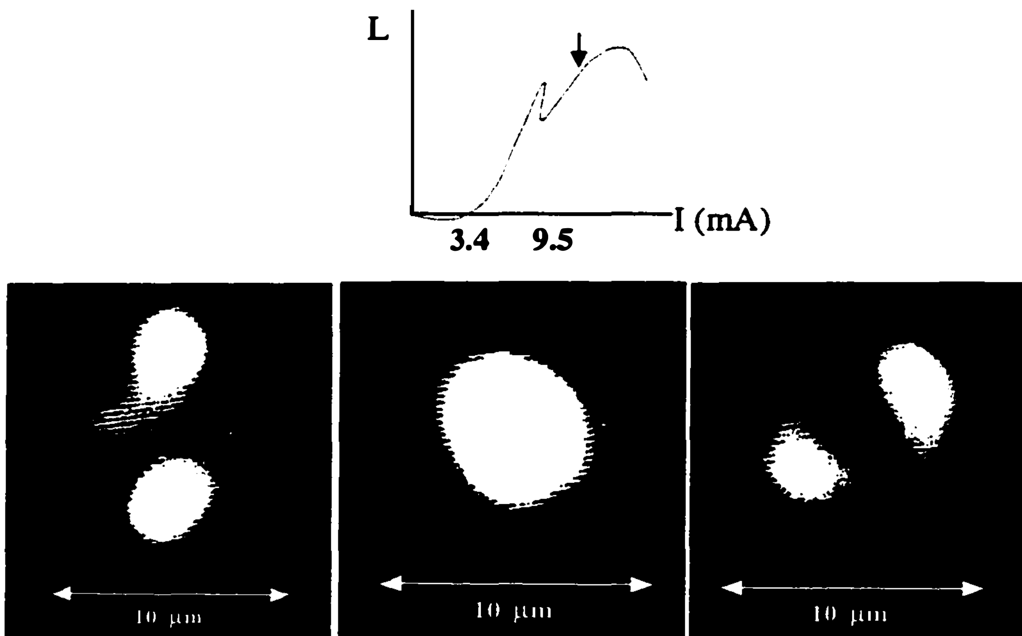

Figure 6.30 Near field image of device biased at 12 mA (above the kink at 2 second intervals). The temperature and wavelength are constant. The near field variation with time is attributed to non-uniform shunt current paths through the fused junction after the kink resulting in spatial hole burning.

6.05 Dynamic performance

The small signal modulation of long wavelength VCLs is important in determining the maximum possible large signal modulation the laser will achieve. In this section, the small signal modulation response of three generations of lasers is analysed. All measurements were performed using a 20 GHz bandwidth HP8150 network component analyser. A microwave frequency ground-signal-ground coplanar probe was used to contact the VCL bondpads that were designed for 50Ω impedance matching. The optical response of the lasers was collected using a cleaved multi-mode lightwave fiber probe.

6.05.1 Device 71

The small signal (-10dBm) modulation response of a 7 μm device from the 71 set is shown in Figure 6.31. The measured data is shown by dots. To quantitatively analyze the device performance, the modulation response was fit to a general modulation transfer function:

$$|M(f)|^2 = \frac{1}{1+(f/f_L)^2} \cdot \frac{f_0^4}{(f_0^2-f^2)^2+(\gamma/2\pi)^2 \cdot f^2} \qquad (6.4)$$

where $M(f)$ is the normalized ratio of the small signal light output to the modulation current, f is the modulation frequency, f_0 is the resonant frequency, f_L is the parasitic roll-off frequency, and γ is the damping rate. The fit is shown as a solid line. The general modulation response behaves as a second order low-pass filter with a damped resonance occurring near the cut-off frequency (-3dB drop in electrical power response). At a DC bias of 1.5 x I_{th} (3 mA), a maximum 3dB bandwidth of 3 GHz is achieved. At larger biases, an initial low roll-off of response characteristic of external parasitic damping limits the response. The parasitic roll-off frequency associated with this device is found

to be 1.2GHz. A plot of f_L extracted from the transfer function fit versus DC bias current is shown in Figure 6.32. Knowledge of the parasitic bandwidth allows one to extract the capacitance of the device from the RC time constant, $f_p=(C_pR_d)^{-1}$. The differential resistance of this device is measured to be 138 Ohms; the capacitance of the device is 2.6pF. The maximum internal parasitic VCL capacitance is estimated to be less than 1pF[11]. Future device designs for high-speed operation should thus attempt to reduce the parasitic capacitance.

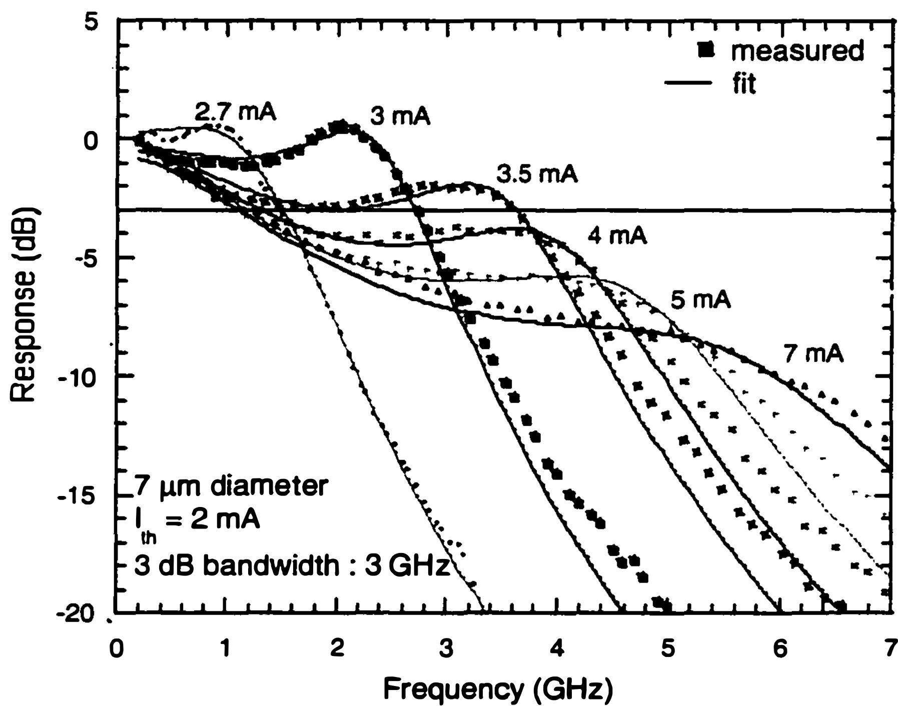

Figure 6.31 Small signal (-10dBm) response of a 7µm aperture diameter device from set 71. A maximum 3dB bandwidth of 3GHz at 1.5 I_{th} (3mA) is achieved. At larger bias currents, damping limits the bandwidth.

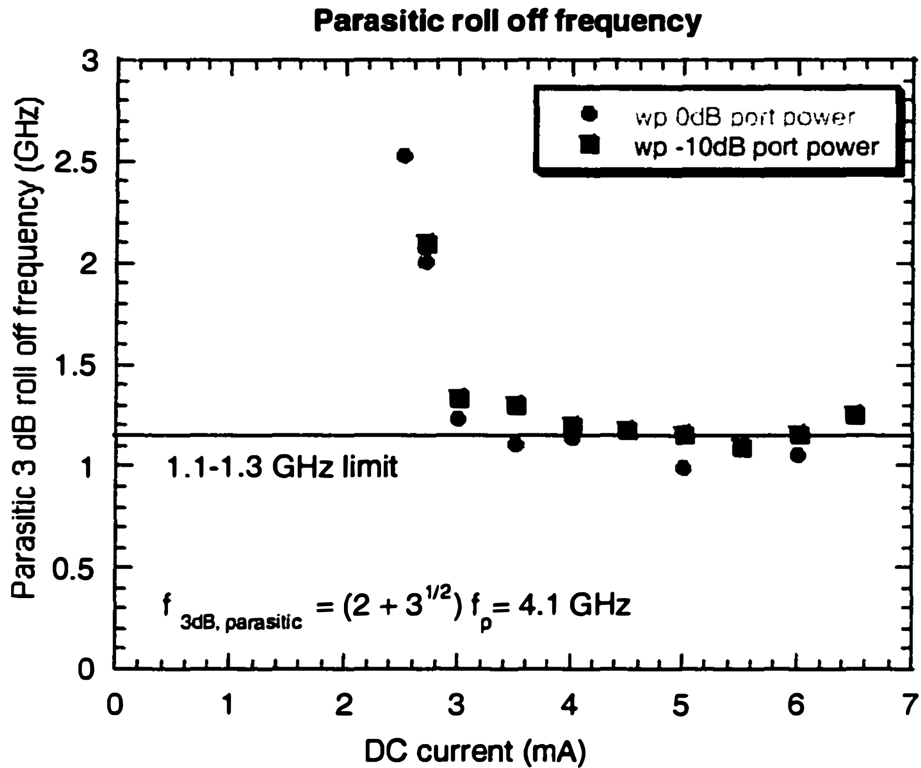

Figure 6.32 The parasitic 3dB rolloff frequency for both 0 dBm and −10 dBm small signal modulation versus DC bias current. The parasitic roll-off frequency is found to be 1.2 GHz and the maximum achievable bandwidth due to parasitics is calculated to be 4.1GHz.

For large resonance frequencies, the K-factor describes the damping of the response. A plct of the damping parameter extracted from the transfer function fit is shown . n Figure 6.33. The K-factor is defined as

$$\gamma = K \cdot f_0^2 + \gamma_0 \tag{6.5}$$

where γ_0 is a constant, and was found by fitting to be 0.486 ns, indicating an intrinsic bandwidth of 18.4 GHz ($f_{max} = 2\pi\sqrt{2}/K$). This bandwidth does not represent issues related to heating of the device but does include issues such as

transport and gain compression. The relatively large K-factor (compared to GaAs-based VCSELs) can be explained by the higher threshold currents, which is related to a high carrier density above threshold. The sublinear dependence of gain on carrier density leads to a reduced differential gain and therefore an increased K-factor[12].

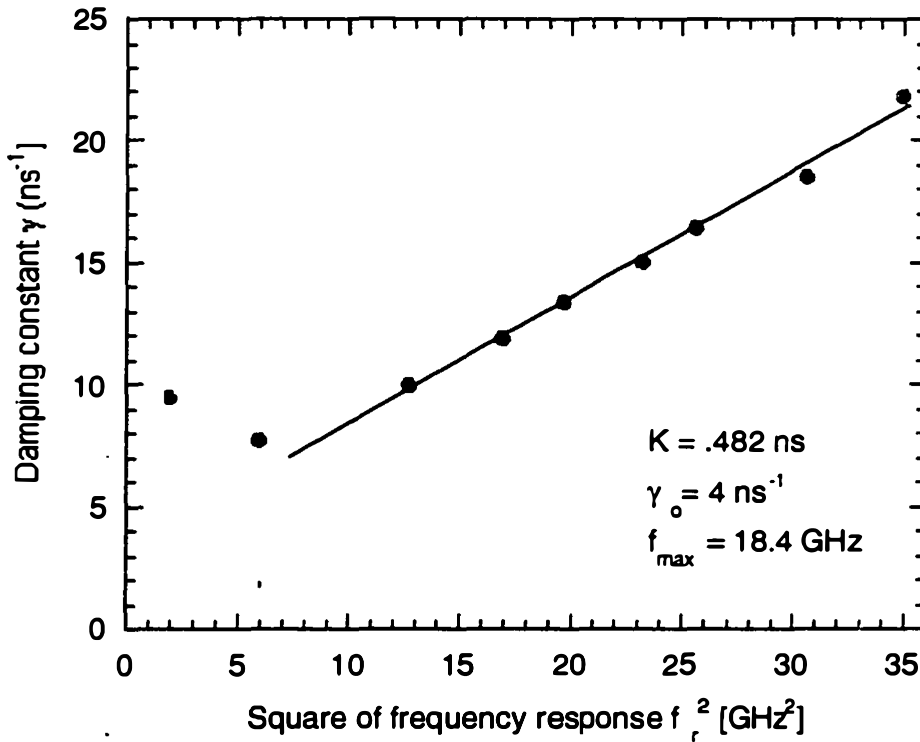

Figure 6.33 Plot of damping constant extracted from transfer function fit as a function of the square of the frequency response. The K-factor is determined to be 0.482 nm, indicating a maximum frequency response of 18.4 GHz.

6.05.2 Device SL3

A plot of the small signal frequency response characteristic of a 1 μm oxide aperture device from the SL3 set is shown in Figure 6.34. A maximum

3dB bandwidth of 3.2 GHz at a current of 5mA is reported. Once again, the response is limited by external parasitics, with a characteristic roll off frequency of 1GHz. A plot of resonance frequency, 3dB bandwidth, and parasitic roll-off frequency is given in Figure 6.35. The maximum achievable bandwidth due to external parasitics is calculated to be 3.8 GHz. The differential resistance of this device is 170 Ohms, yielding a calculated device capacitance of 5.4 pF. This capacitance is quite high, and can be attributed to both the highly doped superlattice and the poor doping profile in the gas source carbon doped mirror.

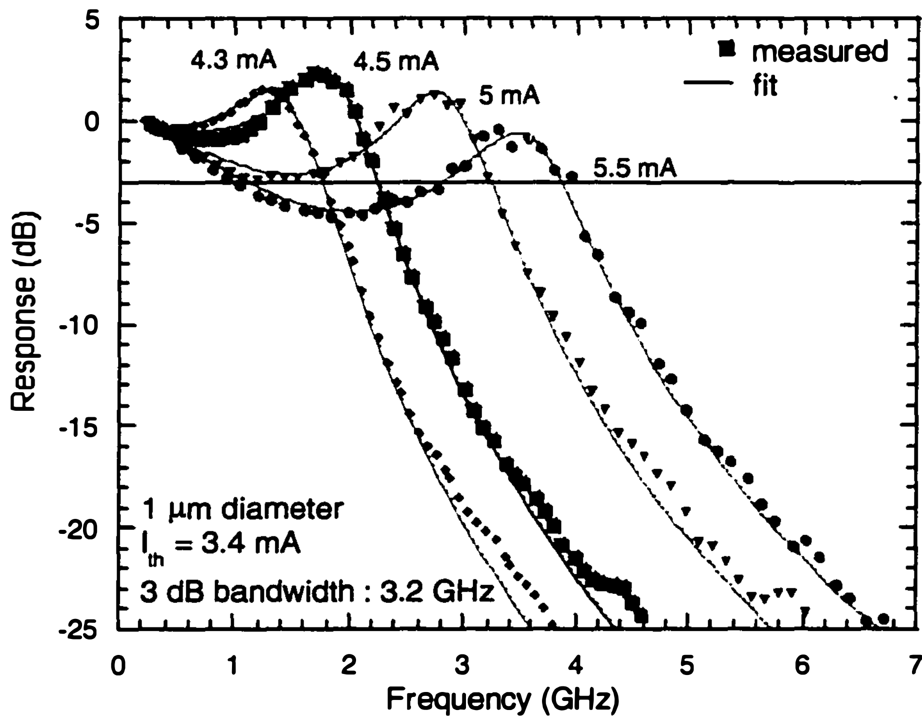

Figure 6.34 Small (0 dBm) signal frequency response of 1 µm aperture opening device from generation SL3. A maximum 3dB bandwidth of 3.2 GHz is reported.

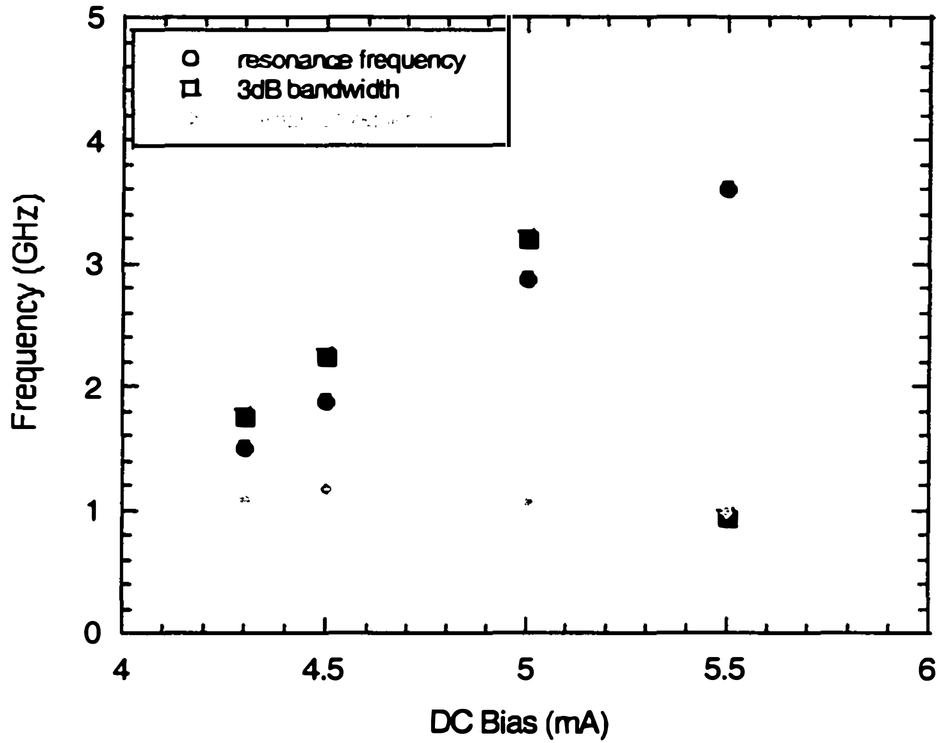

Figure 6.35 Plot of resonance frequency, 3dB bandwidth, and parasitic roll off frequency as a function of DC bias.

In the absence of gain compression and device heating, one would expect the bandwidth of the device to scale as the square root of the current above threshold. Solving the single-mode photon and carrier density rate equations, the resonance frequency can be descibed as:

$$\omega_R = \left[\frac{\Gamma v_g dG(I - I_{th})}{q} \right]^{1/2} \tag{6.6}$$

where ω_R is the relaxation oscillation frequency, dG is the differential gain, Γ is the confinement factor, v_g is the group velocity and q is the electronic charge.

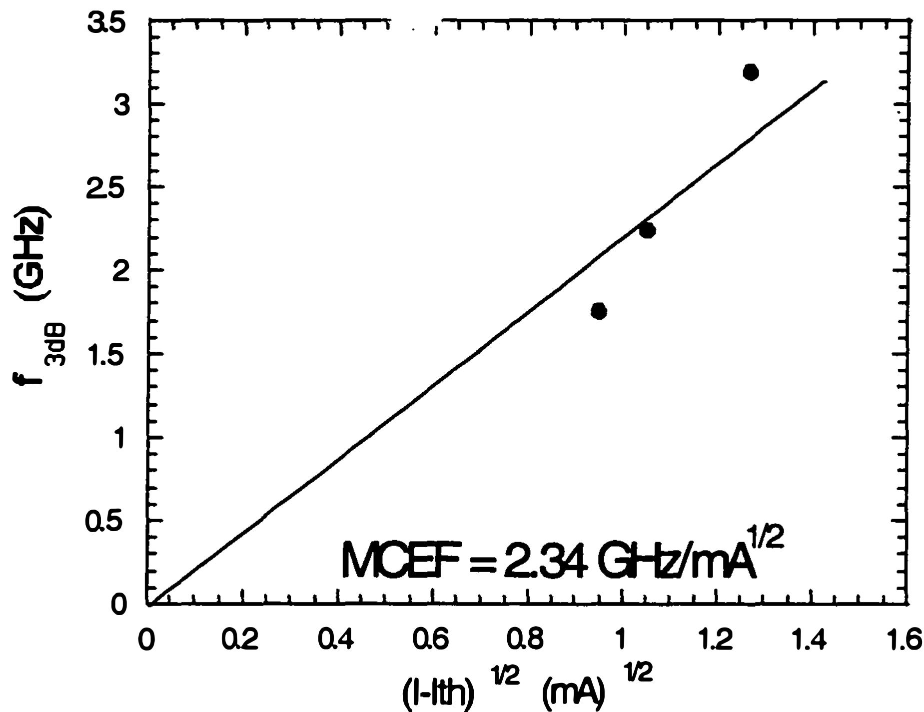

Figure 6.36 The 3dB bandwidth vs. square root of current above threshold is plotted to reveal a MCEF of 2.34 GHz/mA$^{1/2}$.

In Figure 6.36 the 3-dB bandwidth versus the square root of current above threshold is plotted. According to Equation 6.6 the points should fall on a straight line. The slope of this line is called the modulation current efficiency factor (MCEF). This specific laser has an MCEF of 2.34 GHz/mA$^{1/2}$, which is reasonable compared to more typical values of 4 GHz/mA$^{1/2}$ reported for similar lasers in the past [13].

6.05.3 Device 75

Device set 75 is the only set of VCLs fabricated in this thesis with bondpads optimized to reduce the external parasitic capacitance of the VCL.

This bondpad optimization was detailed in the design chapter. It is immediately clear the effect this had on the modulation bandwidth. Two individual VCLs are analyzed in this section; v10 is a 10 μm oxide aperture device and v4 is a 4μm oxide aperture device. The modulation characteristics of v4, a single mode device, is presented first. The small signal response of v4 is shown in Figure 6.37. Immediately apparent is the reduction in parasitic capacitance as compared with former device runs. A record long wavelength VCL -3dB bandwidth of 7.1GHz at 6mA bias is demonstrated.

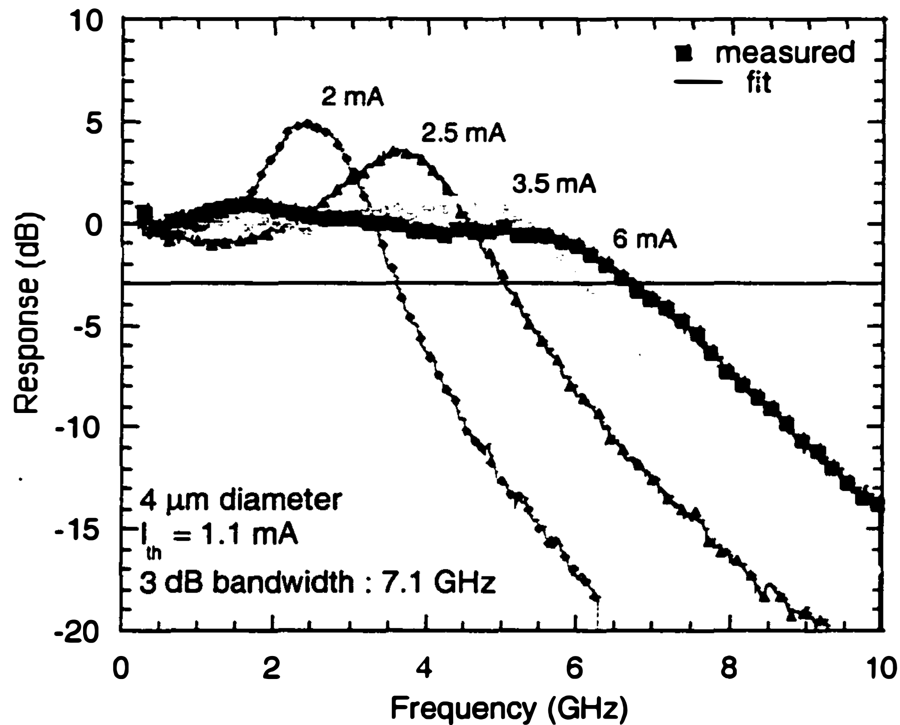

Figure 6.37 Small signal response of device 75. Reduction in bond pad capacitance has lead to demonstration of record modulation bandwidth for long wavelength VCLs of 7 GHz at a DC current of 6 mA.

Performing a curve fit using the general modulation transfer function allows one to extract the capacitance of the device from the RC time constant

to be 0.917 pF; an indication that the bondpad capacitance has been reduced significantly. The device capacitance of v11 is calculated to be 1.15 pF. A plot of the damping factor vs. the square of the resonance frequency is given in Figure 6.38. The K-factor is determined to be .645 ns, implying a maximum intrinsic bandwidth of 13.8 GHz. Figure 6.39 compares the modulation current efficiency of the small and large devices. A linear fit at low biases above threshold reveals MCEF values of 4.125 GHz for v4 and 2.87 GHz for v11. The higher MCEF of v4 is attributed to the fact that v4 is single mode whereas v10 is multi-mode. The deviation from the fit at high bias is thought to be due to gain saturation of the active region.

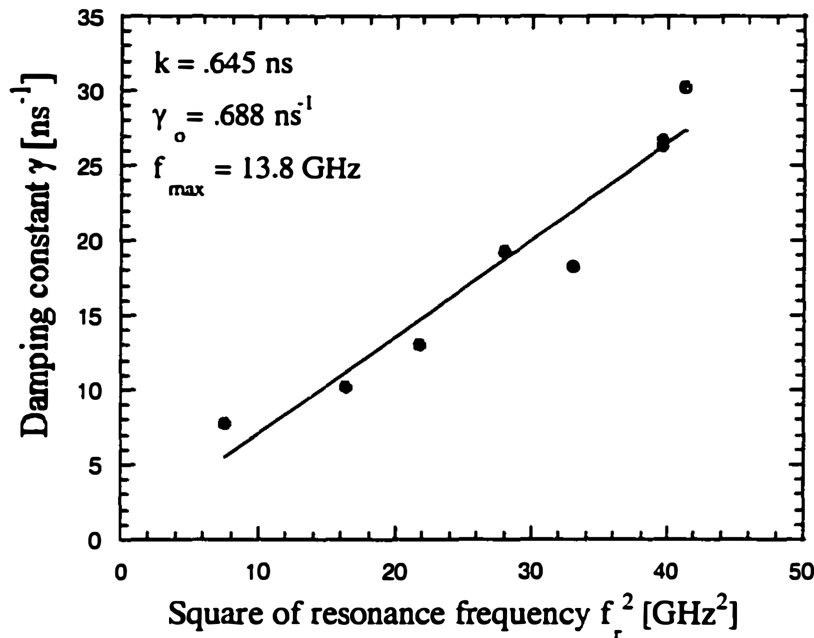

Figure 6.38 Damping constant extracted from transfer function fit vs. square of the resonance frequency for a 4μm capacitance optimized device. The K-factor is determined to be .645 ns, implying a maximum intrinsic bandwidth of 13.8 GHz.

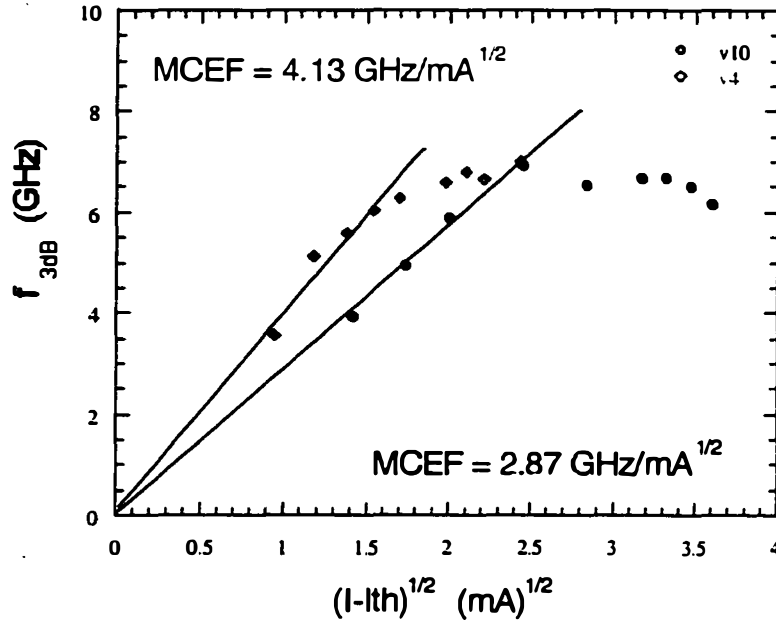

Figure 6.39 3dB bandwidth vs. square root of current above threshold for 4 μm and 10 μm aperture device. A modulation current efficiency of 4.125 GHz/mA$^{1/2}$ is reported for the 4 μm device and a MCEF of 2.87 GHz/mA$^{1/2}$ is reported for the 10 μm device.

Most important to the analysis of this set of lasers is the simple dependence of resonance frequency and 3dB bandwidth on DC applied bias, as shown in Figure 6.40. Both resonance frequency and 3dB bandwidth maintain the relation of

$$f_{3dB,thermal} = \sqrt{(1+\sqrt{2})} \cdot f_{r,max} \qquad (6.7)$$

over the entire range of data collected. However, the resonance frequency ceases to increase with bias current above 8 mA. This is precisely the current at which thermal rollover in the L-I-V characteristic occurs: these VCLs are thermally limited in their response. The calculated thermal limit to the maximum achievable bandwidth for this device is 8.25 GHz.

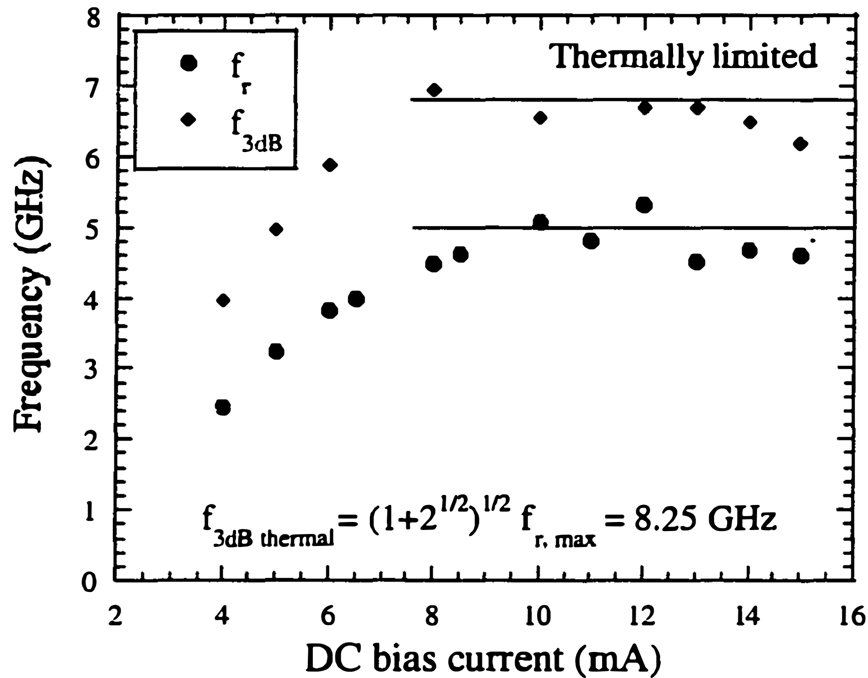

Figure 6.40 Figure of 3dB and resonance frequency versus DC bias. Thermal limitation of the frequency response is demonstrated.

Long wavelength, double fused VCSELs have demonstrated 2.5Gb/s transmission over 200 km of single mode fiber[13]. Optical pumping of our device structures have demonstrated 6Gb/s transmission over 25 km of fiber[14]. In order to carry out future transmission experiments, the frequency response of the double fused VCSEL structure must be understood and optimized. We have demonstrated a record high small signal modulation response of 7.1 GHz simply by reducing the external parasitics via reduced bondpad capacitance. Further reductions in external parasitics can be achieved through smaller diameter pillars and reduction in bondpad area. Additionally, one might consider decreasing the oxidation depth and increasing the oxidation thickness to decrease the contribution of this layer to the device capacitance.

In order to avoid charge build up at the oxide layer completely, an ion implanted device might also be considered. In order to improve the frequency response even further, the thermal performance of the double fused structure must be addressed.

6.06 Summary of device results

Long wavelength VCSELs face many challenges inherent to the physics of low energy gap materials systems. Long wavelength VCSELs fabricated by wafer fusion have consistently defined the state of the art in the field since the very first demonstration. This thesis has explored the wafer fused interface in exhausting detail, and has built upon a greater understanding of the fusion process to develop better VCSELs. In addition to optimization of the mirrors for lowered fused junction resistance, the fusion process itself was optimized to demonstrate record high temperature, sub-milliamp threshold VCSELs. Using the basic design, maximum operating temperatures of 74°C, characteristic temperatures of 132K, and modulation bandwidths in excess of 7 GHz were demonstrated. A better understanding of the fusion process also lead to the development and incorporation of a superlattice defect blocking layer at the fused interface. This feature serves both as a gettering site for defects generated during the fusion process (hence improving the gain of the active material), and as a dopant supplying layer to reduce the fused junction resistance. Unfortunately, due to poor choices in mirror designs, the SL VCSELs were not able to outperform the basic design generations in high temperature performance. However, the persistence of low threshold devices despite unusually high operating voltages is encouraging. Finally, the first selective area fused, under-etched active region VCSEL was demonstrated in an ambitious attempt to demonstrate both current and carrier confinement in a LW-VCSEL. These devices operated in pulsed mode; their *relatively* poor

thermal performance is attributed to damage suffered by the mirrors during the fusion. However, the basic concept was demonstrated, and future work in this area is definitely promising.

In summary, a better understanding of the fusion process, its effects on the materials being fused, and the freedom it affords device designers has lead to the successful demonstration of 7 generations of devices using three distinct VCSEL structures. The uniformity and reliability of the fusion process has been addressed, with nearly 100% device yield on the fused areas (comprising >95% of the sample area). No other technique to develop LW-VCSELs has had so much success. Clearly, wafer fusion is the most immediate and obvious choice for the development of commercial quality LW-VCSELs.

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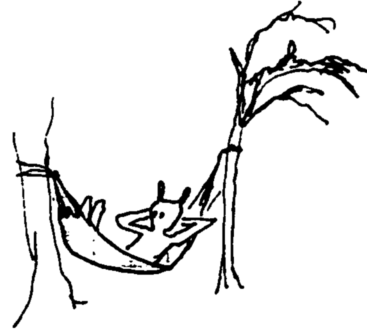

Chapter 7

Conclusions and Future Work

This thesis is an in depth examination of the wafer fused interface: its formation, its structure and chemistry, its effect on electrical and optical properties of the fused materials, and the devices it enables. A deeper understanding of the fused interface is of particular interest to the field as the approach to realizing commercial VCSELs is yet undetermined. A careful analysis of the fused interface has revealed the process to be robust and the interface characteristics to be reproducible. The devices it enables define the state of the art in the field.

Structure and chemistry:

The interface was determined through TEM to be 7 nm thick, amorphous in nature, and with a high degree of intermixing in that region. SIMS revealed the presence of organic contamination, most notably high levels of oxygen and carbon localized to the interface. Hydrophilically terminated surfaces bonded best, demonstrating large scale uniformity of the bond over 1 cm^2 samples. Wet bonding with channels yields the best uniformity, and all surface preparations lead to similar contamination levels at

the fused interface. It is recognized that all wet passivation treatments used in this thesis were aqueous in nature and that a possible improvement in oxygen concentration at the interface may be attained by passivation in a non-aqueous medium such as benzene, while still maintaining the uniformity of the bond. In addition, fusion under UHV conditions with a phosphorous overpressure, to allow for the native oxides to be blown off without surface degradation, is also recommended. Dopant species also aggregate at the fused interface. The diffusion of Zinc towards the fused interface enhances the interdiffusion of all four elements (Ga, In, As, and P).

An analysis of the dislocation structure resulting from fusion revealed the presence of 4 individual dislocation networks that accommodate lattice mismatch, substrate tilt, rotation, and thermal mismatch. The first three networks are localized to the fused interface whereas the dislocations arising from the strain produced by differential contraction upon cooling are volume defects. An analysis of the misfit dislocation network accommodating lattice mismatch indicates that the bonding temperature (~550°C) is lower than the fusion annealing temperature of 630°C. It is recommended that future bonding occur at lower temperatures.

Electrical and Optical Effects:

The impact of the fused interface on the electrical and optical properties of the fused materials was also investigated. Electrical conduction across an n-n junction behaves ohmically whereas conduction across a p-p interface is plagued by a highly reproducible 1.2 V drop. We believe this to result from an n-type interface, creating a p-n-p-n structure when fusing an active region diode to a p-mirror. The exact nature of the n-type charge at the interface is unknown, but it is believed to result from improper removal of surface contamination before fusing. Such a large voltage drop is unlikely to result from defects at the interface. The aforementioned approach to removing

surface oxides under UHV conditions is recommended to reduce this voltage drop. In the meantime, we introduced a dopant (Zn) supplying layer to the InP side of the interface to compensate the n-type charge. With this approach, the voltage drop at the interface was reduced to 300 meV.

The thyristor-type nature of the fused p-p interface is directly responsible for the kink present in fused VCSEL L-I-V characteristics. This kink not only degrades the stability of the near field of the device, but also is the fused VCL's greatest reliability problem. As the temperature of the VCSEL is increased, the kink moves lower in current. When the kink moves lower in current than the threshold of the VCL, a shunt current path is created around the active region of the device, and it becomes nearly impossible to attain the carrier density necessary for lasing. Once again, the remedy for this is found in the removal of the n-type layer at the fused interface.

The impact of the fusion process on the luminescence quality of the materials being fused was investigated through both low and room temperature PL studies. It was found through LT-PL that QWs placed as close as 25 nm on the GaAs side, and 50 nm on the InP side of the junction maintained or improved their luminescence intensity after fusion. It was also noted that the interdiffusion of group III elements is enhanced by the fusion process. Room temperature PL studies of actual doped structures indicated that fusion degrades the luminescence intensity of strained MQW regions 300 nm removed from the fusion surface on average by a factor of 4. However, the interposition of a superlattice defect blocking structure at the fusion surface of the active region lead to a factor of 8 *improvement* in the luminescence intensity of the gain material. For the first time, the fusion process has been demonstrated to be a process *beneficial* to material quality. The electrical impact of the SL layer has yet to be minimized for optimal transport across the junction.

Double Fused Vertical Cavity Lasers:

A better understanding of the fusion process, its effects on the materials being fused, and the freedom it affords device designers has lead to the successful demonstration of 7 generations of devices using three distinct VCSEL structures. The uniformity and reliability of the fusion process has been addressed, with nearly 100% device yield on the fused areas (comprising >95% of the sample area). Sub-milliamp threshold VCSELs were fabricated, achieving a maximum operating temperature of 74°C, characteristic temperature of 132K, and modulation bandwidth in excess of 7GHz. The incorporation of a superlattice defect blocking layer at the fused interface lead to CW operation at 38°C. Finally, the first selective area fused, under-etched active region VCSEL was demonstrated in an ambitious attempt to demonstrate both current and carrier confinement in a LW-VCSEL. These devices operated in pulsed mode; their *relative* poor thermal performance is attributed to damage suffered by the mirrors during the fusion. It is recommended that the fusion pressure be reduced in order to avoid this damage.

To minimize the optical impact of the fused interface, the junction is placed at a null in the standing wave pattern of the VCSEL cavity. The cavity is designed to be 3/2 λ to remove the MQW active region from the fusion surface. However, current spreading before and after the fused junction due to the large potential drop at the fused interface is the largest contributor to current loss. It is therefore recommended that a 1/2 λ cavity be attempted, in an effort to reduce additional current spreading after the fused junction. Until an InP- based oxide aperture is available, this is the recommended way to reduce current spreading after the fused junction in a basic device structure.

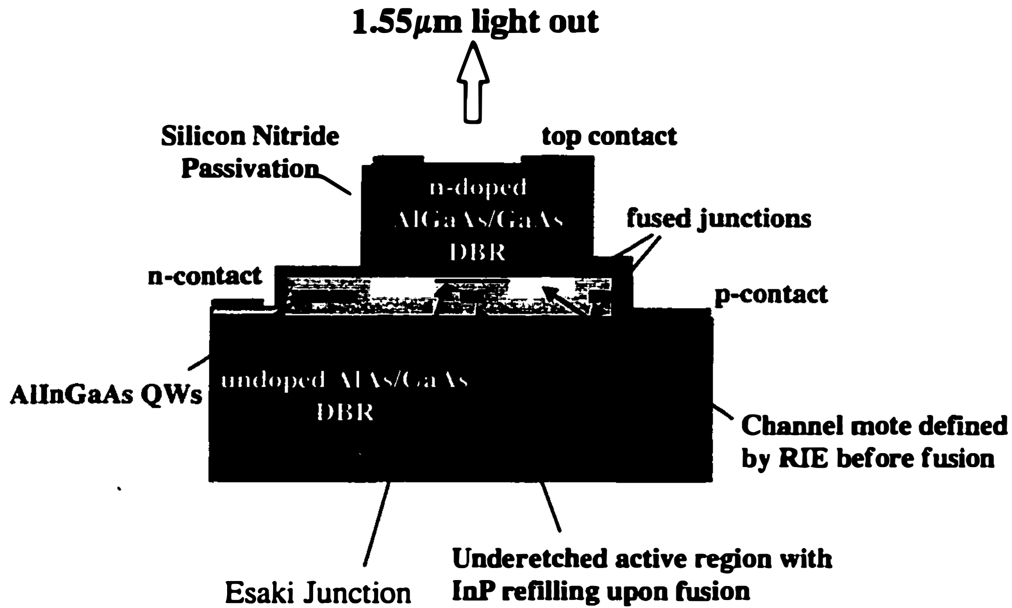

Figure 7.1 The ultimate device design: current is injected through the top n-mirror and conducted ohmically through the n-n fused interface. An Esaki junction, grown by MBE, is incorporated at the surface of the AlInGaAs-based active region. Current (and possibly carrier) confinement are achieved through the selective area fusion, under-etched active region method. The second contact is an n-type intra-cavity contact.

The p-p fused junction voltage drop, and the kink associated therewith, are by no means trivial device features to amend. Without the addition of a UHV fusion station with a phosphorous overpressure to the cleanroom repertoire, it is unlikely that the contamination issues will be resolved. As long as there is a p-p fused junction in the device through which current is passed, a kink will be present and the reliability of the device will be in question. In addition to the electrical problems posed by the p-p fused interface, the optical loss associated with the p-doping of the mirrors is formidable. Since ohmic conduction and lower loss is associated with n-n fused interfaces and mirrors, the obvious direction for LW-VCSEL technology is to abolish the p-p fused interface from

the device design. The only way to do this and still confine the current in the device is to develop an insulating aperture on the InP side of the interface. This thesis has demonstrated such an aperture via selective area fusion. It is therefore recommended that the ultimate device structure could be achieved through the combination of an etched current aperture in combination with a n-n fused junction and an Esaki junction in the active region to allow the intra-cavity contact to be n-type. A figure of the optimal device design is shown in Figure 7.1. Much success has already been demonstrated with the AlInGaAs Esaki junction active regions grown by Kim at UCSB. No other technique to develop LW-VCSELs has had as much success as wafer fusion. Clearly, wafer fused LW-VCSELs are the most immediate and obvious choice for the development devices that will meet commercial requirements in the coming years.

Appendix A

Wafer Fusion Process Flow