

20 GHz high performance planar Si/InGaAs *p-i-n* photodetector

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Planar Si/InGaAs wafer fused *p-i-n* photodetectors were fabricated and measured. They show high internal quantum efficiency, high speed, record low dark current, and no evidence of charge trapping, recombination centers, or a bandgap discontinuity at the heterointerface. © 1997 American Institute of Physics. [S0003-6951(97)00418-X]

The advantages of directly bonding *III-V* and Si wafers to fabricate devices which maximize the advantages of each material are well known.^{1–4} We demonstrate here high performance $\lambda = 1.55 \mu\text{m}$ telecommunication *p-i-n* photodetectors on a Si substrate. These devices are then used to investigate the characteristics of the wafer fused Si/InGaAs interface, which is important for both *p-i-n*'s and avalanche photodiodes (APDs). Recently, a Si/InGaAs APD formed by wafer fusion was demonstrated.^{5,6} This Si heterointerface photodetector advantageously used an InGaAs layer for the absorption of $\lambda = 1.3 \mu\text{m}$ light and a Si layer for the avalanche multiplication region. High bandwidth (BW=9 GHz) and high gain ($G=35$) resulted in a record gain-bandwidth product of 315 GHz. The dark current, however, was substantially higher than is desirable ($I_D = 80 \mu\text{A}$ at $G = 20$). One aim of the present study was to determine if this large I_D was due to intrinsic defects at the heterointerface (e.g., traps, interface charge, recombination centers, dislocations, etc.) or a result of the fabrication technology used (e.g., mesa device isolation, and ion implantation); another goal was to accurately measure the interface and charge transport properties. Thus, in order to analyze these issues planar Si/InGaAs *p-i-n*'s were fabricated.

The Si wafer consisted of a $0.5 \mu\text{m}$ undoped Si epilayer grown on an n^+ substrate using rapid thermal epitaxy.⁷ The *III-V* wafer was grown on an n^+ InP substrate using low pressure metal organic chemical vapor deposition (MOCVD), and consisted of a $0.3 \mu\text{m}$ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (abbreviated InGaAs) stop etch layer, followed by a $0.6 \mu\text{m}$ InP window layer and a $1.0 \mu\text{m}$ InGaAs absorption layer (all undoped). These wafers were fused in an oven at 650°C in flowing H_2 as described previously.⁵ After bonding, the InP substrate and the InGaAs etch stop layer were removed.

Device fabrication began with the deposition of a $0.15 \mu\text{m}$ SiO_2 layer, followed by etching a $22 \mu\text{m}$ circular window down to the InP, diffusing Zn for the *pn* junction (550°C for 45 min resulting in a total depth of $1.0 \mu\text{m}$ and thus, a $0.4 \mu\text{m}$ p^+ InGaAs layer), a second deposition of SiO_2 , opening a $12 \mu\text{m}$ diameter window, etching down to the InGaAs absorption layer, depositing a $30 \mu\text{m}$ diameter

Au:Be *p*-contact metal, and finally making an *n*-contact to the Si substrate by etching a $70 \mu\text{m}$ diameter mesa and depositing Al. The completed structure is shown in Fig. 1.

The dc photocurrent and the reverse dark current were measured as a function of bias voltage from $V_b = 0$ to 10 V (shown in Fig. 2). Note that the photocurrent is constant with V_b even down to zero bias, suggesting that there is no significant charge accumulation or trapping at the interface. Further, the dark current is a record low for Si:*III-V* bonded wafers ($I_D = 100 \text{ pA}$ at $V_b = 4 \text{ V}$), and is in fact comparable to standard InP/InGaAs *p-i-n*'s, again indicating the excellent quality of the interface. To quantify this, we note that from $V_b = 0$ to 4 V the dark current is given by generation recombination and thus we can write⁸ $I_D = A q n_i W / \tau$. Substituting for the area $A = 4.5 \times 10^{-6} \text{ cm}^{-2}$ (the *pn* junction active diameter is $24 \mu\text{m}$ when diffusion is accounted for), $n_i = 10^{12} \text{ cm}^{-3}$ for the intrinsic carrier density in the depletion region, and the depleted InGaAs width $W = 0.6 \mu\text{m}$ at 4 V , one obtains a carrier lifetime of $\tau = 400 \text{ ns}$. This long lifetime again indicates that there are no significant traps or defects in the bulk of the depletion region or at the heterointerface. Additional support for this conclusion is supplied by forward *I-V* measurements, which over the range $V_b = 0.1$ to 0.4 V is given by $I = I_0 \exp(qV/nkT)$, with an ideality factor⁸ $n = 1.1$ to 1.2 . This near unity value of n again shows the lack of recombination centers in the active region. The absolute value of the quantum efficiency $\eta = \eta_i \eta_a$ (where $\eta_a = 1 - e^{-\alpha L}$, is the absorption quantum efficiency, α

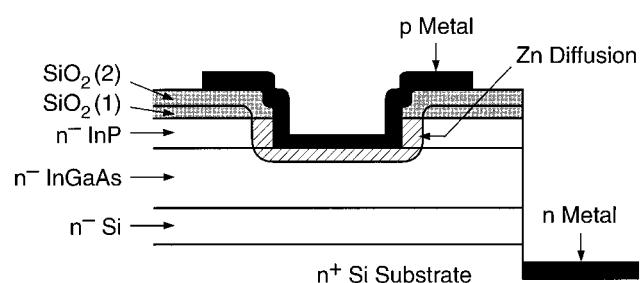


FIG. 1. Structure of back illuminated planar Si/InGaAs *p-i-n* detector.

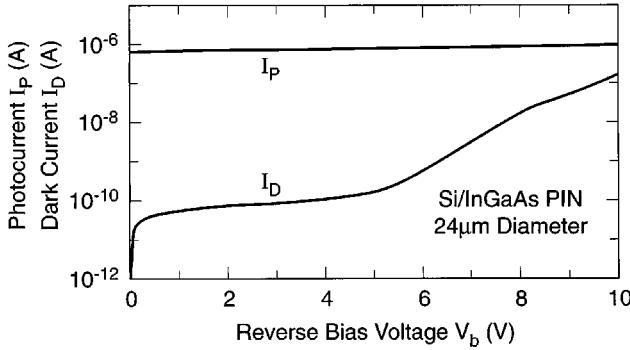


FIG. 2. Photocurrent and dark current for a reverse biased Si/InGaAs *p-i-n*.

is the optical absorption coefficient, and η_i is the internal quantum efficiency, i.e., the fraction of the photogenerated carriers which are collected) was accurately measured at $\lambda = 1.55 \mu\text{m}$ by comparing the photoresponse to that of a calibrated InP/InGaAs *p-i-n*. After correcting for the reflectivity of the incident Si surface, and the thickness of the InGaAs absorption layer, the internal quantum efficiency was determined to be $\eta_i = 100\%$ to within the accuracy of our experiment (5%). This result clearly demonstrates that there is no measurable loss of photogenerated carriers across the Si/InGaAs, further confirming the nearly ideal interface.

The capacitance was measured as a function of voltage, using a high speed probe and a Lightwave Analyzer at 1 GHz. The total measured capacitance $C_m(V_b)$, shows a smooth decrease with increasing V_b , with no indication of a change of slope, demonstrating that there is no excess charge at the interface. This can be seen more quantitatively by using the relation⁸ $C(V_b)/A = [q\epsilon N/2(V_b + V_{bi})]^{1/2}$, where $C(V_b) = C_m(V_b) - C_0$ is the junction capacitance, $C_0 = 50 \text{ fF}$ is the measured fixed stray and pad capacitance, ϵ is the dielectric constant, N is the charge density in the depletion region, and V_{bi} is the built-in voltage. Thus, by plotting $C(V_b)^{-2}$ vs V_b a straight line with a slope of $(2/q\epsilon NA^2)$ should result. Figure 3 shows an excellent straight line, and thus, no indication of any trapped charge at the heterointerface. From the slope and intercept, one obtains $N = 1.4 \times 10^{16} \text{ cm}^{-3}$ for the depletion layer charge density, and $V_{bi} = -0.6 \text{ V}$, consistent with other measurements on our epitaxially grown InGaAs and Si. Furthermore, the junction capacitance, $C = 50 \text{ fF}$ at 10 V, is in excellent agreement with our geometrically calculated value using the $1.1 \mu\text{m}$ depletion width consisting of $0.6 \mu\text{m}$ InGaAs and $0.5 \mu\text{m}$ Si.

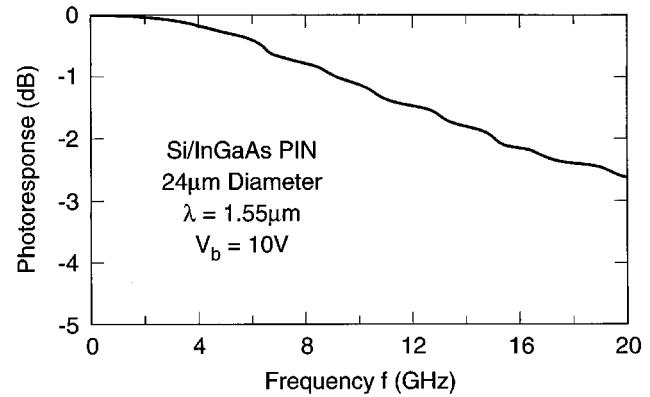


FIG. 4. Frequency response of the Si/InGaAs *p-i-n* photodetector showing a 3 dB response of 21 GHz.

Combining $C_m = 100 \text{ fF}$ (at $V_b = 10 \text{ V}$) with the measured contact resistance $R_c = 40 \Omega$ [i.e., a total circuit resistance of $R = (50 + R_c)\Omega = 90 \Omega$,] results in a calculated RC frequency response of $f_{RC} = 1/(2\pi RC) = 18 \text{ GHz}$, which is expected to dominate the response speed, since the transit time limited frequency is calculated to be $f_T = 38 \text{ GHz}$. A lightwave analyzer and a high speed probe were used to measure the 3 dB bandwidth which was found to be 21 GHz, as shown in Fig. 4. This good agreement with f_{RC} at 10 V as well as at lower biases (e.g., at $V_b = 0 \text{ V}$, $C_m = 280 \text{ fF}$ and both f_{RC} and experiment give 6 GHz), again demonstrate that there is no trapping at the interface due to either defects or a hetero-bandgap ΔE_c discontinuity. Thus, the Si/InGaAs interface seems nearly ideal not only in the lack of any defects or charge trapping, but also in having a small discontinuity $\Delta E_c \approx 0$.

As a final characterization of the interface, we measured the absolute photocurrent noise power⁹ using a noise figure meter at a frequency of 30 MHz and a bandwidth of 4 MHz. Knowledge of this noise behavior is important if the Si/InGaAs junction is to be used in an APD, since receiver sensitivity is critically affected by avalanche noise and any

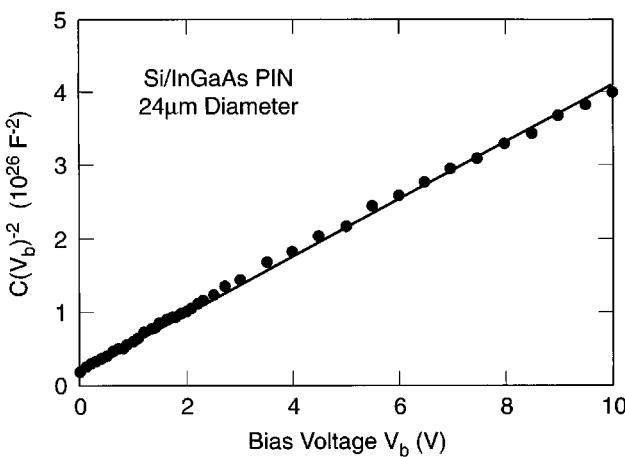


FIG. 3. Plot of the square of the inverse junction capacitance $C(V_b)^{-2}$ vs bias V_b . The circles are the measured data.

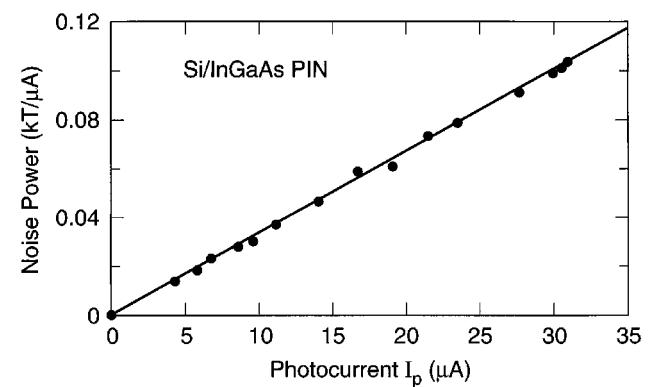


FIG. 5. Measured (circles) photocurrent noise power (in units of $kT/\mu\text{A}$), vs I_p .

excess noise contribution due to traps would be highly detrimental. For this determination, the photocurrent was generated using an incoherent light source to eliminate any spontaneous emission noise which would be produced by a laser. As shown in Fig. 5 the current noise power is linear in I_p , as expected, with a slope of $3.4 \times 10^{-3} \text{ kT}/\mu\text{A}$ in good agreement with the minimum shot noise limit of $2qRI_p/kT = 3.9 \times 10^{-3} \text{ kT}/\mu\text{A}$, (for $R = 50 \Omega$); thus, showing no excess noise and no evidence of traps.

In conclusion, we have fabricated and measured novel planar Si/InGaAs *p-i-n*'s. We find that the photocurrent is flat with voltage down to $V_b = 0$, the reverse bias dark current is extremely low (100 pA at $V_b = 4 \text{ V}$), the forward bias current has an ideality factor n near unity, the capacitance $C(V_b)$ shows no indication of trapped charge at the interface, the internal quantum efficiency is $\approx 100\%$, the high speed response is RC limited at 21 GHz, and the photocurrent noise is close to the minimum shot noise limit. All these measurements demonstrate that there is no significant charge trapping, recombination centers, or bandgap discontinuity ΔE_c at the heterointerface and thus, that the Si/InGaAs in-

terface is nearly ideal. This indicates that record performance, high gain-bandwidth, low dark current APDs can be expected.

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