

8 × 8 × 40 Gbps fully integrated silicon photonic network on chip

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We demonstrate a fully integrated photonic network-on-chip circuit with wavelength division multiplexing transceivers on silicon. The total transmission capacity is up to 8 × 8 × 40 Gbps for intra- and inter-chip interconnections. © 2016 Optical Society of America

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Large-scale photonic integration circuits (PICs) have been demonstrated on InP [1] and Si [2–5] substrates for data communications. Silicon PICs 3D integrated with electronic integrated circuits promise future high-speed and cost-effective optical interconnects to enable Exascale performance computers and datacenters [5]. For realistic intra-chip and inter-chip optical links, the bandwidth density and total power consumption are major challenges. Consequently, full integration of all photonics components on chip, including high-speed modulators and photodetectors, and especially lasers, is needed for scalable and energy-efficient system topology designs. A library of functional devices has been developed on silicon with the heterogeneous integration method, including ultralow loss waveguides, arrayed waveguide grating (AWG) routers, low threshold distributed feedback (DFB) lasers, high-speed electroabsorption modulators (EAMs), semiconductor optical amplifiers (SOAs), and photodetectors (PDs) on silicon [6,7], enabling a large-scale photonic integration implementation. In this Letter we demonstrate a high-speed heterogeneous integrated circuit on silicon for chip level interconnection and network.

A schematic of the photonic circuit is shown in Fig. 1(a). The network-on-chip (NoC) circuit consists of a reconfigurable ring-bus network and eight wavelength division multiplexing (WDM) transceiver nodes, with eight-channel high-speed transmitters and receivers in each node. All transceiver nodes connect to the circular bus waveguide through broadband optical switches. Extra ports are linked to waveguide edge couplers for off-chip fiber coupling. In each transceiver node, the WDM transmitter has eight channels with a single-mode DFB laser [8], monitoring photodetector (MPD), and high-speed EAM on each channel. The corresponding WDM receiver includes eight P-I-N type InGaAs PDs. Some of the nodes have optical preamplifiers. 1 × 8 AWGs are used as a multiplexer and demultiplexer (Mux/DeMux) in the transmitter (Tx)

and receiver (Rx), respectively, with a fixed 200 GHz channel spacing in the C/L bands. Mach–Zehnder interferometer switches are used in the network architecture, with cascaded 3 dB adiabatic couplers (ACs) for broadband switching of all WDM channels.

The ring-bus architecture defines a reconfigurable NoC. Figure 1(b) illustrates three major working modes. A default mode when a node with its optical switch normally *OFF*, the corresponding transmitter only talks to its local receiver for self-configuration. When two of the switches are in *ON* status, the eight-channel signals from one transmitter are routed to the WDM receivers at another node, or to optical fiber coupling for off-chip communication. It can also be defined to be a 1 × *N* broadcasting network with one transmitter and *N* receivers by partially turning on the switches. This reconfigurable network architecture provides great flexibility for the system design for chip level optical interconnects.

The CMOS compatible fabrication of the NoC circuit has two major parts: silicon-on-insulator (SOI) processes—e.g., definition of surface type Bragg grating, silicon waveguide, edge coupler, optical switches, and AWGs with a 4-in. (100 mm) DUV process—and III/V die bonding and III/V processing for active components. Three different III/V epi structures were optimized individually and transferred to designated areas on the SOI wafer for DFB/SOA, EAM, and PD, respectively. All active and passive components were protected with silicon oxide and polymer before metallization to reduce capacitance and improve the RF performance. More than 400 functional components, including passive and active components, were integrated into a system on the NoC chip. The process yield of passive components was close to 100% with

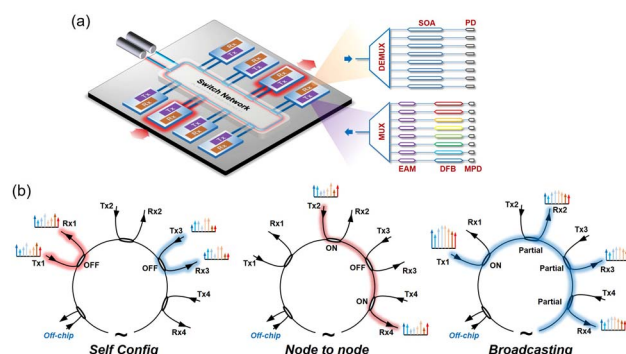


Fig. 1. (a) Architecture of the heterogeneously integrated NoC circuit and (b) some of its reconfigurable working modes.

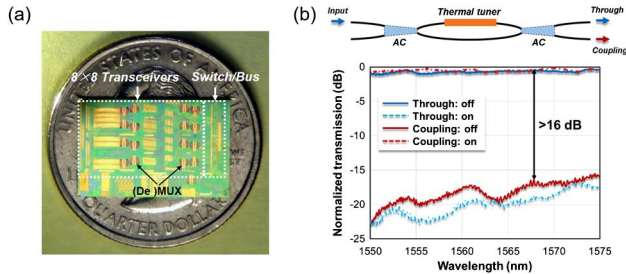


Fig. 2. (a) Photo of the transceiver chip after fabrication and (b) diagram and normalized transmission spectrum of an AC switch.

an overall yield of about 90% counting active and passive elements. A photo of the photonic chip is shown in Fig. 2(a), with the bus waveguide and switch column indicated on the right side. The performance of the AC-MZI switch is shown in Fig. 2(b). By thermally tuning the TiPt heater on one arm, the optical switch has a minimum extinction ratio of 16 dB between the *ON* and *OFF* status across the wavelength from 1550 to 1575 nm, with a low insertion loss below 1 dB.

Figure 3(a) shows the light-current and current-voltage curve of a typical integrated DFB laser with a 400 μm long cavity, 26 μm mesa width, and 1 μm Si waveguide. The laser has a threshold current of 7.5 mA with a threshold current density of 470 A/cm² at 20°C. The inset in Fig. 4(a) shows its single-mode operation above threshold, with a side-mode suppression ratio larger than 55 dB. Eight DFB lasers with wavelength aligned to the corresponding AWG channels are shown in Fig. 3(b). The missing channel was caused by a defective device on the chip. Manual wavelength alignment is performed by adjusting the driving currents of DFBs and the heater array on the AWG. It is noteworthy that the normalized transmission spectrum in Fig. 3(b) is from two 1 \times 8 AWGs back-to-back on one waveguide, representing an ultralow insertion loss below 1.5 dB for each AWG. Each AWG has a footprint of about 1.2 mm² with channel cross talk of -28 dB.

Figure 3(c) shows the transmission spectrum of the integrated 100 μm long EAM under different reverse biases. With a strong quantum-confined Stark effect in the active region with 12 quantum wells centered at 1485 nm, the EAM shows a wide optical bandwidth

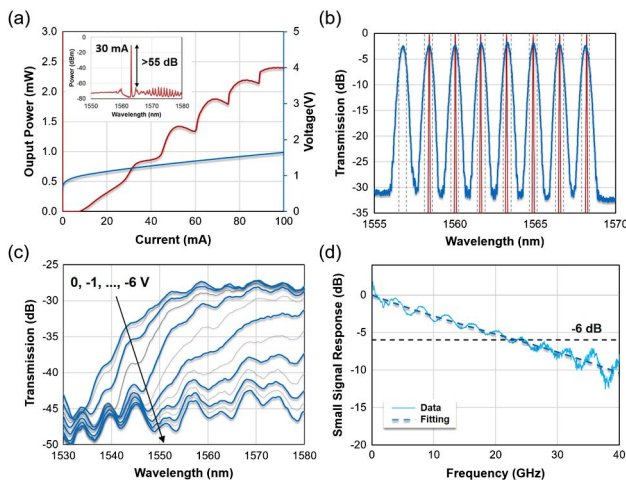


Fig. 3. (a) LIV curve and spectrum of integrated DFB, (b) transmission spectrum of cascaded AWGs with aligned DFB spectrum with normalized power level, (c) transmission spectrum of EAM at various biases, and (d) small signal response of a Tx-Rx channel.

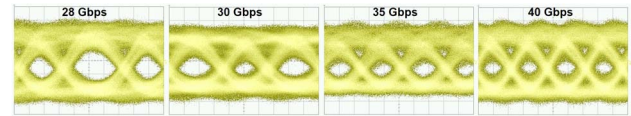


Fig. 4. Eye diagram of on-chip communication from one channel.

from 1550 to 1580 nm, and extinction ratio larger than 5 dB with 1 V_{pp} bias swing at appropriate reverse bias. The small signal response of the on-chip link is shown in Fig. 3(d), including modulator, AWG, and the photodetector in the corresponding receiver. A 6 dB bandwidth of 24 GHz was observed for the EAM-PD link.

Due to the lack of an appropriate driver circuit, only one channel can be tested simultaneously at this moment. The switch array was driven by a multi-pin DC probe card to route the signal among transceivers. The DFB driving current and AWG heaters were adjusted appropriately to align the lasing wavelength to the transceiver channels. The data transmission test was applied with a 40 GHz pattern generator and 2⁷ - 1 pseudorandom binary sequence (PRBS) signal. A data rate of 40 Gbps per channel performance is shown in Fig. 4, with the vertical scale 50 mV/div in the eye diagrams. The result shows a potential large capacity of the transceiver array, with 320 (8 \times 40) Gbps per transceiver node and 2.56 Tbps (8 \times 320 Gbps) for the whole photonic circuit.

In this Letter we show breakthrough results on a fully integrated photonic interconnection circuit on silicon. The advances reported here are enabled by well-controlled heterogeneous integration of all active devices with multiple epitaxial materials on the same silicon PIC with light coupled with a low loss waveguide and low reflection between the different active devices. With such methods, a reconfigurable NoC circuit with large bandwidth transceivers was integrated on a single chip, promising a solution for future low cost and large bandwidth chip level interconnections.

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