

**University of California, Santa Barbara**

**Wafer Bonded 1.55  $\mu\text{m}$   
Vertical Cavity Laser Arrays  
for Wavelength Division  
Multiplexing**

By Adil M. Karim

*A dissertation submitted in partial satisfaction of the requirements for the degree of*

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“No man is an island, entire of itself; every man is a piece of the continent, a part of the main...”

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*Dedicated to my family: past, present and future*

## Vita

### Education

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## **Abstract**

### **Wafer Bonded 1.55 $\mu\text{m}$ Vertical Cavity Laser Arrays for Wavelength Division Multiplexing**

Adil M. Karim

Vertical cavity lasers in the 1.55  $\mu\text{m}$  wavelength band are attractive sources for optical networks. Previous devices have been limited by low output power and poor thermal performance. In this work, novel wafer bonding techniques were developed to create high-performance 1.55  $\mu\text{m}$  vertical cavity lasers and a new class of multiple wavelength vertical cavity laser arrays. Wafer bonding enables the integration of thermally conductive GaAs/AlGaAs mirrors and traditional InP/InGaAsP active regions. A superlattice barrier was used as a buffer layer during bonding to reduce the number of non-radiative recombination centers in the active region. The surface of these superlattice layers was patterned prior to bonding to define multiple wavelength cavities. Continuous-wave operation was achieved at temperatures up to 105°C. This is the highest reported lasing temperature for a 1.55  $\mu\text{m}$  vertical cavity laser. Threshold currents of 0.8 mA were measured. The peak output power at 20°C was 0.7 mW. The peak output power at 80°C was 0.2 mW. Single-mode operation with a side-mode suppression ratio in excess of 40 dB was observed for a 5  $\mu\text{m}$  aperture device. Four-channel arrays were also fabricated. The wavelength span was 1509.1-1524.4 nm with channel spacing of approximately 5 nm. This is the first demonstration of an independently addressable, multiple-wavelength vertical cavity laser array at 1.55  $\mu\text{m}$ . Threshold currents of 1.0 mA and peak output powers of 0.5 mW were measured for array elements. Thermal and optical crosstalk between array elements are negligible, due to the high thermal conductivity of the bottom mirror and large device pitch.

# **1. Introduction**

## **1.1. Overview**

This thesis makes significant contributions in the areas of wafer bonding and long wavelength vertical-cavity surface-emitting laser (VCSEL) development. A superlattice buffer layer was introduced in order to preserve material quality through the bonding process, resulting in improved photoluminescence from bonded quantum well structures. This technique was used to fabricate high performance 1.55  $\mu\text{m}$  VCSELs with the highest continuous wave operating temperatures reported to date. Intracavity tuning layers were patterned prior to bonding in order to define multiple wavelength VCSEL cavities. This approach was used to create the first independently addressable VCSEL array for wavelength division multiplexing at 1.55  $\mu\text{m}$ .

In this chapter, the basic motivation for long wavelength VCSEL fabrication is explored. The favorable aspects of the vertical cavity geometry are presented. Although there are challenges in extending the success of short wavelength VCSELs to longer wavelengths, the need for low cost, high performance sources in optical networks has driven long wavelength VCSEL development. The suitability of 1.55  $\mu\text{m}$  VCSELs and multiple wavelength

VCSEL arrays for local and metropolitan area networks is discussed. Finally, the remaining chapters in the dissertation are outlined.

## 1.2. Vertical Cavity Surface Emitting Lasers

Vertical cavity surface emitting lasers have been studied extensively in recent years for use in fiber optic networks and as optical interconnects. The VCSEL offers many potential advantages when compared to the traditional edge-emitting laser. The most recognized advantage of the VCSEL is compatibility with low cost wafer scale fabrication and testing methods. High volume, low cost manufacturing is of vital importance for the next generation of photonic devices. The VCSEL has several other characteristics that make it well-suited for use in fiber optic systems. These include a circular output beam for high coupling efficiency into optical fiber, high modulation bandwidths at low currents, single mode operation, low power consumption and the potential for producing integrated modules and arrays on wafer.



Figure 1.1 Schematic of edge-emitting and vertical cavity surface-emitting lasers

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Edge-emitting lasers emit light in a direction parallel to the host substrate. The rectangular waveguide supports an elliptical transverse mode. This elliptical beam is not easily coupled into standard optical fiber, resulting in coupling efficiencies of 20-50% for most designs. An additional lens element may be introduced to improve coupling efficiency to above 70%. However, this increases the cost of the laser and complicates packaging. The devices are formed by cleaving the processed wafer into individual devices. The cleaving process determines the size of the laser cavity and defines the laser mirrors formed by the semiconductor-air interface. Typical edge-emitters are less than 10  $\mu\text{m}$  wide and under 1000  $\mu\text{m}$  in length. Cleaving of individual laser die is a time- and labor-intensive process. The limited yield forces prices upward and increases the lead time of new devices. Testing expenses are high due to labor costs, complications associated with handling small device die and inability to select successful devices until after cleaving. Advanced cavity designs such as distributed Bragg reflector (DBR) and distributed feedback (DFB) lasers offer high single-mode powers for increased performance, but require complicated regrowths that further limit production volumes. Despite these manufacturing limitations, edge-emitting lasers are widely used in lightwave systems and are the dominant sources for transmission at the telecommunications wavelengths of 1300 and 1550 nm.

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The vertical cavity geometry found in VCSELs offers significant manufacturing advantages compared to traditional edge-emitting lasers and also has the potential for increased functionality at lower cost. As seen in Figure 1.1, the VCSEL cavity is defined by top and bottom mirrors in a direction perpendicular to the substrate. These mirrors contain a number of quarter-wave layers and are known as distributed Bragg reflectors (DBRs). These multilayer films are required in order to provide the high reflectivities required in a VCSEL, typically greater than 99%. Because the processed wafer contains discrete devices without the burden of an additional cleaving step, devices may be tested with a probe card on wafer prior to packaging. This streamlines the production and testing processes compared to those used for edge-emitting lasers. Light-emitting diodes (LEDs) have similar manufacturing advantages, but are limited to low-speed, short distance optical links due to poor frequency response and large spectral width. The VCSEL geometry allows for close packing of devices, with up to 30,000 conservatively spaced devices possible on a 2" wafer. This density may be increased even further for applications such as laser printing and optical storage.

If VCSEL wafers are cleaved into individual devices, some of the same difficulties are encountered as with edge-emitting devices. However, one of the

principal VCSEL advantages lies in the simple formation of one and two-dimensional arrays. These arrays significantly reduce packaging costs by integrating multiple devices on a single die without any manual assembly. Etched cylindrical waveguides may easily be introduced on the VCSEL wafer to produce a circular spot for efficient coupling into standard single-mode or multi-mode fiber. Coupling efficiencies of 90% for multimode fiber and 80% for single-mode fiber have been reported using simple butt-coupling without additional optics[1-3]. The selective lateral oxidation of a layer in the VCSEL structure may be used to provide transverse electrical and optical confinement[4]. The oxide aperture funnels the current into a small area for efficient lasing by providing local electrical isolation. The aperture also provides lateral optical confinement by acting as an intracavity lens, reducing optical losses due to scattering and diffraction[5]. This technique of index guiding can be used to control the output mode profile[6]. Current confinement may also be achieved through the use of ion implantation[7]. By confining the injected current, the lasing action is limited to a small area by gain guiding. In this case, thermal lensing is the primary contributor to lateral index guiding[8].

The active region volume in a VCSEL is typically smaller than that of an edge-emitting laser, leading to reduced threshold currents[9]. This lower modal

volume permits high modulation bandwidths at low current levels[10-13]. Optoelectronic integrated circuits (OEICs) featuring VCSELs and transistors fabricated from a common epitaxial structure have been reported[14-16]. These low cost modules have several potential applications in optical communications. Arrays of VCSELs can be used for parallel signal processing[17]. VCSELs may also be integrated with photodetectors[18, 19] for bi-directional optical interconnects.

### **1.3. Long Wavelength VCSELs**

Rapid progress in VCSEL development over the last decade has allowed 850 and 980 nm devices to be deployed in optical networks. The use of ion implantation for current confinement has permitted the manufacture of highly efficient planar devices[20]. The selective oxidation of AlGaAs alloys[21] has enabled major advances in threshold current and wallplug efficiency[22]. In short-haul applications such as Fibre Channel and Gigabit Ethernet (GbE), the efficiency and high speed at low power of 850-980 nm GaAs-based VCSELs have made them the light source of choice. However, for longer reach applications, long wavelength (1.3-1.6  $\mu\text{m}$ ) laser diodes are required. Using 1.3 and 1.55  $\mu\text{m}$  sources over single-mode fiber significantly reduces attenuation and dispersion in optical links. It can be seen in Figure 1.2 that long wavelength lasers at 1.3 and

1.55  $\mu\text{m}$  permit higher bit rates over longer distances than lasers emitting at 0.85 or 0.98  $\mu\text{m}$ . The graph shown below assumes an input power of 1 mW and uses common parameters for single-mode and graded-index fiber. The model includes attenuation and dispersion, but non-linear effects such as chirp have been neglected.

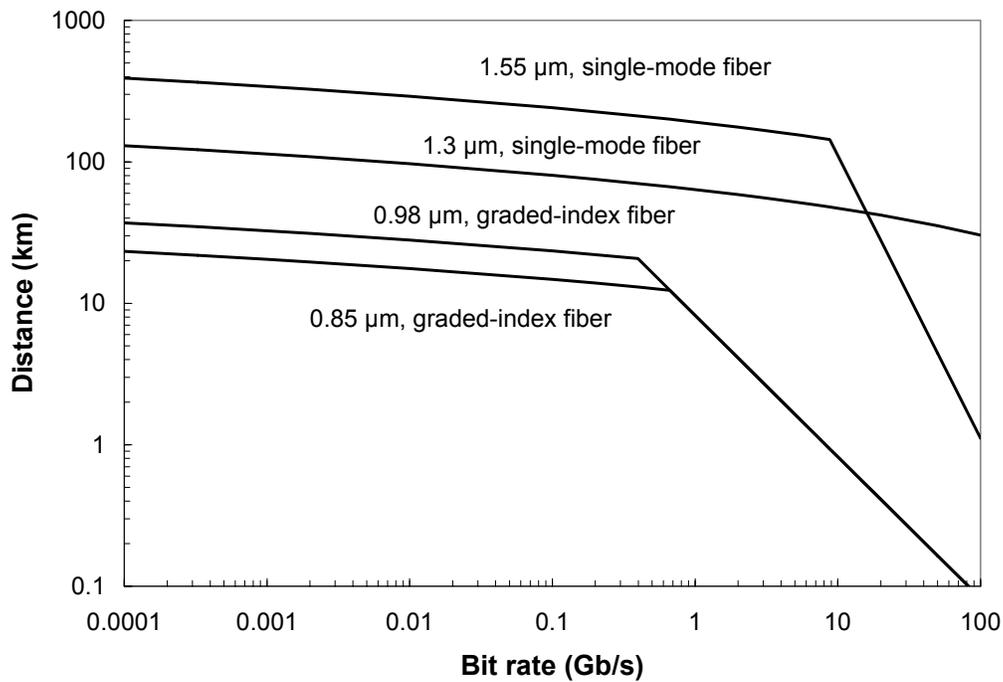


Figure 1.2 Fiber optic transmission limits for 1.55, 1.3, 0.98, and 0.85  $\mu\text{m}$

Emerging standards such as 10 Gigabit Ethernet (10 GbE) are expected to drive the market for low-cost optical transceivers capable of high-speed

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transmission over distances of more than 10 km. It is expected that 10 GbE will find acceptance in local area networks (LANs), metropolitan area networks (MANs) and even wide area networks (WANs). This developing standard will specify protocols for a new generation of optical Ethernet. Applications such as LAN to LAN interconnects, broadband virtual private networks (VPNs) and high speed Internet access will see dramatic performance improvements as products based on 10 GbE become available. 10 GbE traffic may be offered with asynchronous transfer mode (ATM), frame relay (FR) and other services, and transported directly over existing synchronous optical network (SONET) links. This helps to ensure efficient use of bandwidth. 10 GbE can itself be used to combine slower access links at the WAN interface.

These new services will become particularly crucial in metropolitan area networks. Although high-performance optical transport solutions have become more common in recent years, these systems are more relevant for long haul transmission and are not generally cost-effective for MANs. The high traffic demands at the metropolitan core include services such as digital subscriber line (DSL), cable modems and streaming video. Multiple wavelengths may be used in order to circumvent fiber exhaust. The highly aggregated nature of metropolitan core traffic requires that these services be provided at full data rates. These new

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metropolitan services may be provided over dedicated wavelengths or shared wavelengths, using time-division multiplexing (TDM). The first draft of the 10 GbE standard calls for four different physical interfaces, but other interfaces may also eventually be ratified by the expected completion date of 2002. Current standards call for 850, 1310 and 1550 nm serial sources, as well as a four-channel multiwavelength option in the 1310 nm band, summarized in Table 1.1. Maximum distances will likely be limited by chirp due to direct or integrated modulation.

<b>Description</b>	<b>Minimum distance, multimode fiber</b>	<b>Minimum distance, single mode fiber</b>
850 nm serial	300 m	Not supported
1310 nm serial	Not supported	10 km
1550 nm serial	Not supported	40 km
1310 nm, four channel	Not supported	10 km

**Table 1.1 10 GbE physical interfaces and minimum distances**

The 1310 and 1550 nm physical interfaces address medium and long reach single mode fiber applications, including metropolitan services and connections to

optical networks. Inexpensive sources such as long wavelength VCSELs are ideal for enabling this next generation of access and backbone technology.

Long wavelength VCSELs are anticipated as sources in other networks as well, including intrasystem links, VSR (very short reach) SONET interfaces, and cable television (CATV) distribution. High performance, single mode devices are slotted for insertion into long haul and metropolitan fiber spans. 1.55  $\mu\text{m}$  VCSELs in the local and metropolitan area network offer the additional benefit of interoperability with the 1.55  $\mu\text{m}$  networks used for long haul transmission. These improvements in performance will be made more accessible by the VCSEL fabrication advantages discussed earlier. In addition, higher signal powers will be permitted due to reduced eye safety risks, since source wavelengths have been pushed further into the infrared. This extends both the reach and functionality of optical modules. Lower voltage operation should also be possible due to the narrower bandgap of long wavelength materials. This reduces power consumption, allowing for simpler drive circuitry and packaging.

#### **1.4. Obstacles to Development**

Despite the obvious commercial incentives, long wavelength VCSELs have been slower to develop than their short wavelength counterparts. The main

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limitation has been unsatisfactory mirror performance. Distributed Bragg reflectors (DBRs) with high thermal conductivity, high reflectivity, and, in the case of current injection through the DBR, high electrical conductivity have proven difficult to fabricate on InP. Poor mirror performance results in low output power and unsatisfactory high temperature operation. Only a limited number of designs have been shown to lase continuous-wave at room temperature. Maximum ambient operating temperatures of 70-85°C are specified by Telcordia for sources in fiber optic networks. In order for VCSELs to maintain their cost advantage over edge-emitting lasers, they must be able to operate at these elevated temperatures without thermoelectric coolers.

The most common materials used for 1.3 and 1.55  $\mu\text{m}$  lasers are InP and InGaAsP, grown on InP substrates. Inherent material qualities of InP/InGaAsP such as low characteristic temperatures, high Auger recombination rates and high intervalence band absorption[23] have slowed long wavelength VCSEL development. The lack of a robust aperturing technique on InP similar to the lateral oxidation of AlGaAs on GaAs has also limited the operating efficiency.

A number of novel designs have been developed to overcome the limitations of the traditional InGaAsP material system. These include AlInGaAs

active regions on InP[24], GaInNAs active regions on GaAs[25-27], quantum dot active regions on GaAs[28], metamorphic GaAs mirrors grown on InP[29, 30], multiple active regions[31], antimonide DBRs[32, 33] and integrated optical pumping[34]. The best high temperature results to date at 1.55  $\mu\text{m}$  were achieved during the research of this dissertation using wafer bonded GaAs/AlGaAs mirrors in electrically pumped devices[35]. The optical, electrical and thermal properties of these bonded DBRs enable significantly improved performance relative to other designs. Published historical temperature data is shown below in Figure 1.3.

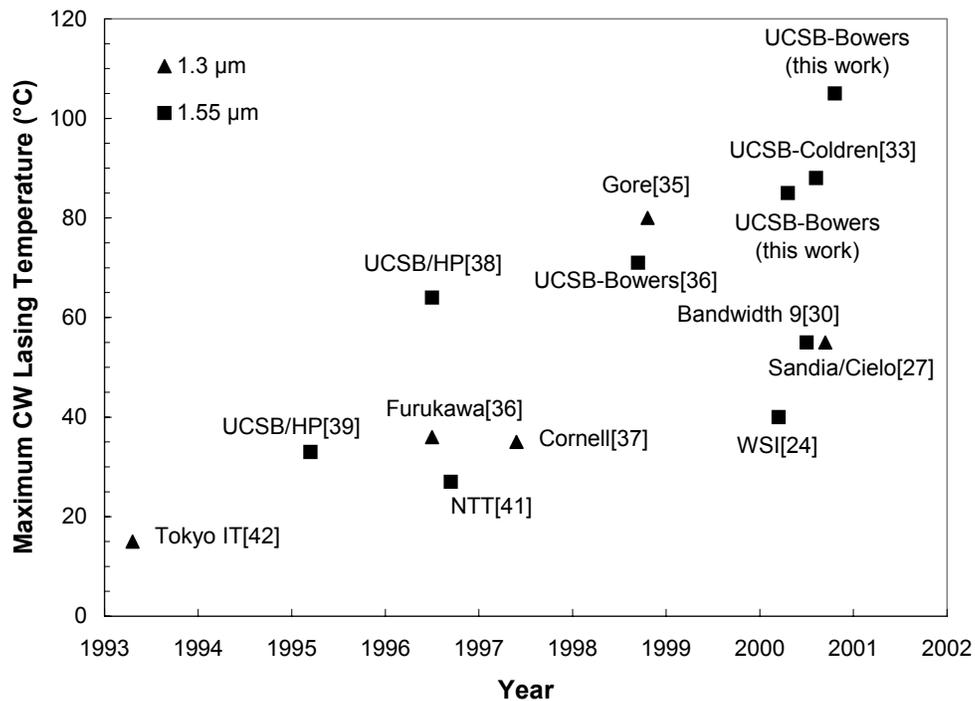


Figure 1.3 Historical continuous-wave lasing temperatures for 1.3 and 1.55  $\mu\text{m}$  VCSELs

## 1.5. Wavelength Division Multiplexing

An explosion in consumer demand for bandwidth has forced many service providers to cope with fiber exhaust. Wavelength division multiplexing (WDM) permits the increase of transmission capacity by using multiple channels operating at different wavelengths. This allows for increased transmission rates without the time and expense of installing additional fiber spans. Sending multiple signals on different wavelengths down a single fiber allows improved bandwidth management, including wavelength routing and reconfiguration. An illustration of the WDM process is shown in Figure 1.4.

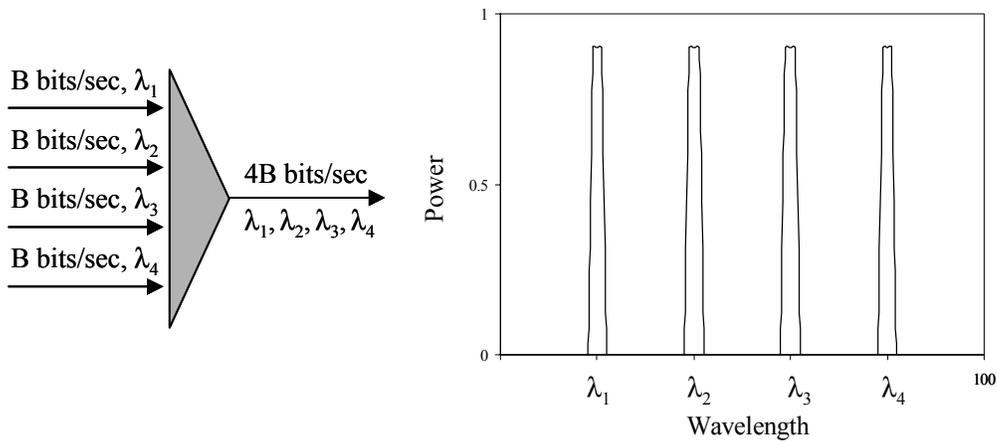
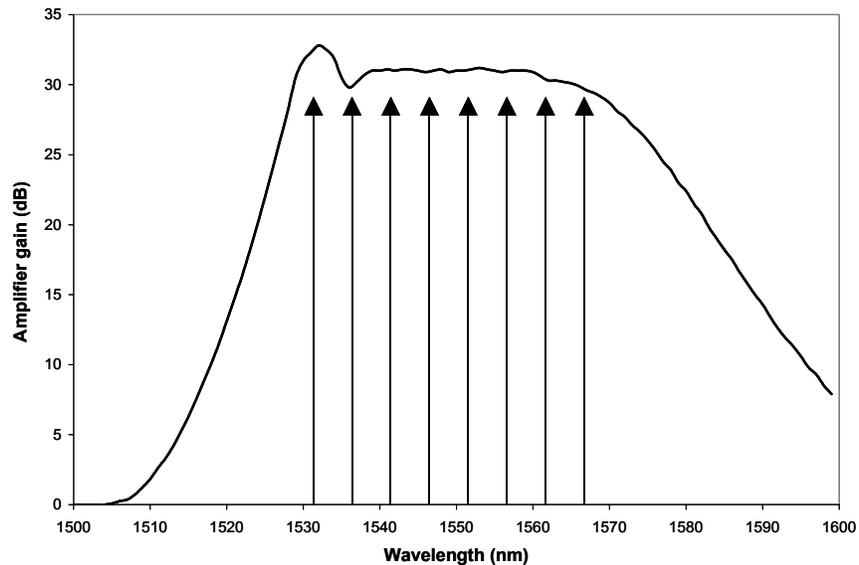


Figure 1.4 Wavelength division multiplexing with four channels

WDM transmission systems utilizing 40 wavelengths at 10 Gb/s are commercially available. Capacities of 6.4 Tb/s (160 channels x 40 Gb/s) have been demonstrated in research laboratories[43]. WDM systems have been deployed in a number of different applications, including undersea, interexchange and local-exchange networks. The 1.55  $\mu\text{m}$  wavelength band is used in order to take advantage of erbium-doped fiber amplifiers (EDFAs). These optical amplifiers can provide in excess of +30 dB gain over a 30 nm bandwidth, as shown in Figure 1.5. One amplifier can simultaneously amplify several WDM signals, without the need for any wavelength-specific components. These high performance, all-fiber amplifiers significantly extend the reach and functionality of 1.55  $\mu\text{m}$  sources beyond the limits shown in Figure 1.2.



**Figure 1.5** Representative schematic of EDFA gain. Arrows indicate eight potential lasing wavelengths in the gain band.

Multiple laser wavelengths are required to launch signals in WDM systems. Channel spacing can range from greater than 10 nm for coarse WDM (CWDM) to less than 0.2 nm for dense WDM (DWDM). These sources are typically individual edge-emitting DFB lasers, packaged together as a module. Using VCSELs as sources in WDM networks would reduce transmitter cost and complexity. The VCSEL fabrication advantages described in Section 1.1 could be used to lower the cost of each individual laser. However, a multiple-wavelength VCSEL array fabricated on a single substrate would further reduce costs by eliminating the complex assembly of individual lasers in WDM transmitter modules. This becomes even more critical as WDM systems extend their reach to metropolitan and local area networks, where cost concerns are paramount. Considering both cost and performance, one and two dimensional multiple-wavelength VCSEL arrays emitting in the 1.55  $\mu\text{m}$  wavelength region are highly attractive sources for low cost WDM networks.

## **1.6. Overview of Dissertation**

This dissertation describes the design, processing and testing of wafer bonded 1.55  $\mu\text{m}$  VCSELs and WDM VCSEL arrays. The wafer bonding technique is used in order to integrate high quality GaAs-based mirrors with conventional InP-based active regions. Theory, design and results from two

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different device generations are presented. This work makes contributions in a number of areas, including wafer bonding, fabrication of 1.55  $\mu\text{m}$  VCSELs and multiple wavelength VCSEL arrays, and wavelength division multiplexing.

Chapter 2 analyzes the distributed Bragg reflectors (DBRs) used as mirrors in 1.55  $\mu\text{m}$  VCSELs. Optical, electrical and thermal characteristics are considered. Experimental results are compared with theory. The use of GaAs/AlGaAs DBRs is motivated by the demonstrated need for high reflectivity, low optical loss, low electrical resistance and high thermal conductivity.

Chapter 3 describes the wafer bonding process used to integrate GaAs/AlGaAs DBRs with InP/InGaAsP active regions. A summary of bonding results from UCSB and other institutions is presented. The bonding process itself is described in detail. The electrical, optical and structural impacts of wafer bonding are considered. The introduction of a superlattice barrier is shown to reduce lattice defects and non-radiative recombination in bonded active regions. Patterned bonding for the definition of multiple wavelength VCSEL cavities is characterized.

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Chapter 4 considers VCSEL device structure and fabrication. Basic VCSEL design philosophy is presented. Different cavity designs and contacting schemes are compared, taking optical and electrical considerations into account. The VCSEL fabrication processes used during the course of this dissertation are described.

Chapter 5 analyzes the characteristics of fabricated single-wavelength and multiple-wavelength device structures. Parameters of interest include threshold current, output power, and differential efficiency. Size and temperature dependence are studied. Thermal and optical crosstalk are considered theoretically and compared with experimental results. Current spreading and carrier leakage are identified as performance-limiting mechanisms.

Chapter 6 summarizes the progress made during the course of this dissertation. The emerging long wavelength VCSEL market is discussed. Future work aimed at continued device development and optimization of existing devices is proposed.

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## **2. Distributed Bragg Reflectors for Long Wavelength VCSELs**

### **2.1. Introduction**

Distributed Bragg reflectors (DBRs) for long wavelength VCSELs must simultaneously satisfy optical, electrical and thermal performance requirements. The conditions imposed on these mirrors are even more stringent than those for short wavelength devices. Long wavelength active regions typically have lower material gain for a given carrier density than short wavelength active regions. As a result, higher mirror reflectivities are required for low threshold currents and low round trip loss. These mirrors must have large optical bandwidths to allow for suitable growth tolerances, wavelength drift with temperature and multiple wavelength operation. Low electrical resistance is required for high-speed operation and reduced device self-heating. Unfortunately, the doping levels used to achieve low electrical resistance contribute to optical loss, particularly in p-type material where loss coefficients at 1.3 and 1.55  $\mu\text{m}$  are significantly higher than in n-type material. An optimized doping scheme must be selected in order to satisfy both electrical and optical concerns. Thermal considerations are particularly critical in long wavelength VCSEL design. Long wavelength active region materials such as InGaAsP are plagued by high Auger recombination rates and poor electron confinement. These problems are even more pronounced at elevated

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temperatures. Device self-heating further exacerbates this situation. In order to maintain a cost advantage over edge-emitting lasers, long wavelength VCSELs must operate efficiently without active cooling. This necessitates the use of DBR materials with high thermal conductivity in order to effectively dissipate the heat generated by resistive and lasing processes.

In this chapter, long wavelength VCSEL DBRs are explored in detail. Three different fabrication methods are discussed: dielectric deposition, epitaxial growth and wafer bonding. Optical, thermal and electrical properties of DBR materials are presented and analyzed. The use of GaAs/AlGaAs DBRs is motivated based on the satisfaction of criteria in all three areas, particularly high thermal conductivity.

### **2.2. Fabrication Methods**

Three viable methods for fabricating long wavelength DBRs have emerged in recent years: epitaxial growth, dielectric deposition and wafer bonding.

#### *2.2.1. Epitaxial growth*

All-epitaxial designs are standard for short wavelength VCSEL structures

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and are used by numerous commercial vendors in high volume manufacturing facilities. However, adapting these techniques to long wavelength VCSELs has proven to be a difficult task. The most common substrate for long wavelength laser growth is InP. There are three major families of epitaxially grown DBRs lattice-matched to InP: InGaAsP/InP[1, 2], AlInGaAs/AlInAs[3] and AlGaAsSb/AlAsSb[4-6]. All have been used to achieve continuous-wave lasing in 1.55  $\mu\text{m}$  VCSELs. Metamorphic GaAs/AlGaAs DBRs have also been grown directly on InP[7, 8]. The principal advantage of epitaxially grown DBRs is that they are directly integrated with the active region similar to GaAs-based, short wavelength VCSELs. This allows for simplified manufacturing processes. These mirrors can be made conductive by doping. Unfortunately, most epitaxial mirrors on InP have poor optical and thermal properties, as will be discussed in sections 2.3 and 2.4. For materials with low index contrast such as InGaAsP/InP and AlInGaAs/AlInAs, exceptionally long growths are required to achieve suitable reflectivities. This requires a high degree of control over growth rates. The mixing of group V elements such as As/Sb has yielded improved index contrast. For these newer materials such as AlGaAsSb/AlAsSb, further efforts in the areas of dislocation control and dopant grading schemes are required. A VCSEL structure with two epitaxial DBRs is shown in Figure 2.1.

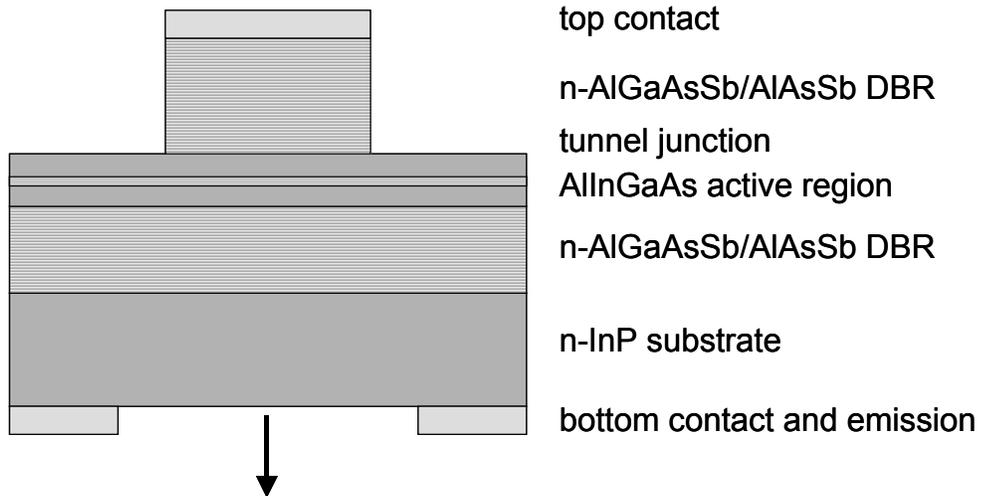


Figure 2.1 1.55  $\mu\text{m}$  VCSEL with two epitaxial AlGaAsSb/AIAsSb DBRs[6]

Other potential methods for the growth of long wavelength epitaxial DBRs have been investigated, including the use of ternary InGaAs[9] and compliant substrates[10, 11]. It should be mentioned that recent developments in the growth of 1.3  $\mu\text{m}$  InGaAsN[12, 13] and InGaAs quantum dot active regions[14, 15] on GaAs have enabled the use of lattice-matched, epitaxially grown GaAs/AlGaAs DBRs in long wavelength VCSEL structures. However, the development of 1.55  $\mu\text{m}$  VCSEL active regions using InGaAsN or other materials on GaAs is an uncertain proposition at this time due to poor radiative efficiency. The discussions in this chapter and in this dissertation are focused on 1.55  $\mu\text{m}$  VCSELs, although many of the conclusions drawn are valid for 1.3  $\mu\text{m}$  VCSELs as well.

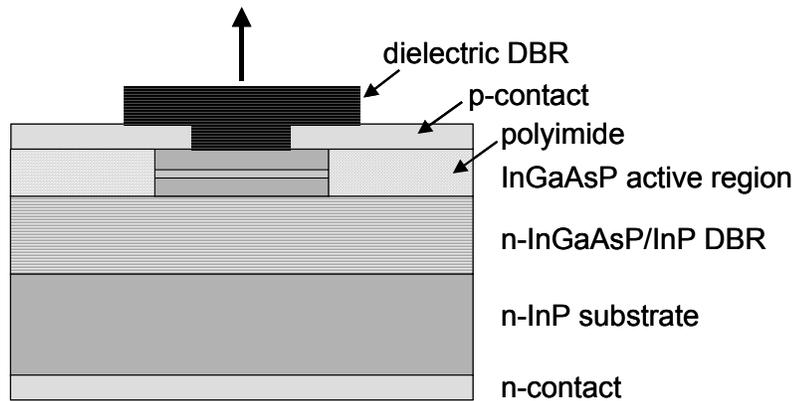
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### *2.2.2. Dielectric deposition*

The first VCSEL of any wavelength was demonstrated with two AuZn metal mirrors on both sides of an InP active region and substrate[16]. The original threshold current of 0.9 A (!) was reduced by the use of dielectric mirrors. Early research on long wavelength VCSELs focused on devices with two dielectric mirrors[17] or one dielectric and one epitaxial (InGaAsP/InP) mirror[18]. Contemporary designs with improved performance have featured improved thermal conductivity and increased index contrast[19]. Dielectric mirrors may be deposited by electron-beam evaporation, sputtering, or plasma-enhanced chemical vapor deposition. Common layer materials include a-Si (amorphous silicon), SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, MgO and MgF. These insulating mirrors typically have large refractive index contrast and require only a few periods to reach reflectivities above 99%. The large index contrast also allows for high optical bandwidths. However, the optical losses in amorphous semiconductors can be significant. The absorption tail of a-Si extends deep into the bandgap[20]. This limits maximum reflectivity for 1.3 and 1.55  $\mu\text{m}$  DBRs, although the problem is more severe at 1.3  $\mu\text{m}$ . Stress in the deposited films makes practical realization of these mirrors a challenge. As the thickness increases, residual stress may lead to cracking, increasing optical loss and compromising the mechanical stability of the device.

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These mirrors typically have poor thermal conductivities, although more thermally conductive materials such as MgO and Al<sub>2</sub>O<sub>3</sub> have been used with improved results[21, 22].



**Figure 2.2** 1.55  $\mu\text{m}$  VCSEL with one dielectric and epitaxial (InGaAsP/InP) DBR

Devices using insulating dielectric mirrors require a more complicated current injection scheme, as shown in Figure 2.2. These ring contacts on thin resistive layers lead to current crowding at the edge of the active region[23]. This results in poor overlap between the optical mode and the injected carriers that provide gain. As a result, unexpectedly high carrier concentrations are required to reach threshold. This contributes to an undesirable feedback effect at elevated temperatures. As the temperature increases, the available material gain decreases. This causes an increase in the carrier concentration required to reach threshold.

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However, increasing the injected current creates even greater non-uniformity in the carrier distribution, reducing field-gain overlap and further increasing the threshold current. This limits the possibility of high-temperature, continuous-wave operation, even more so in devices with high thermal resistance[24].

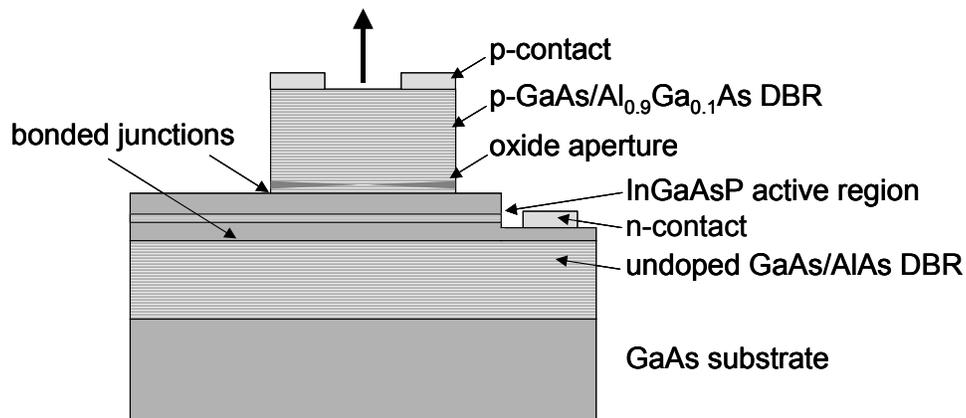
Integration of a dielectric mirror as a bottom mirror is a difficult process requiring substrate holing. Contemporary designs use only a single dielectric mirror, often in conjunction with integrated heat sinking to lower thermal resistance[25].

### *2.2.3. Wafer bonding*

The first report of VCSELs fabricated using wafer bonded DBRs was made by Dudley in 1992[26]. Electrically pumped lasing was demonstrated in 1994[27]. Wafer bonding permits the integration of non-lattice matched materials such as GaAs and InP in a single device. Separate epitaxial wafers are combined under appropriate temperature and pressure conditions. The process usually includes substrate removal to expose the bonded layers for processing. In VCSELs, wafer bonding is motivated by the desire to use mature, high performance GaAs/AlGaAs DBRs with traditional InP based active regions. The qualities of GaAs/AlGaAs DBRs that make them an attractive option for long wavelength VCSEL DBRs will be discussed later in this chapter. Heteroepitaxy of lattice-mismatched materials requires thick buffer layers that would degrade

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VCSEL performance. Threading dislocations in heteroepitaxial structures may have an adverse impact on device reliability. This is also true of devices fabricated using metamorphic growth techniques. Numerous TEM studies[28-30] of bonded GaAs/InP interfaces have shown that that any resulting crystal dislocations are mechanically stable edge dislocations, which should not have an impact on device lifetime. This allows the reliable integration of two semiconductors with different lattice constants. Wafer bonding generally refers to a direct bond formed between two semiconductors, without the use of an intermediate layer. The interface can be electrically and thermally conductive while maintaining optical transparency. Devices have been fabricated with one bonded and one epitaxial mirror[31], one bonded and one dielectric mirror[32], and two wafer bonded mirrors as shown in Figure 2.3[33-36]. The wafer bonding process will be discussed in greater detail in Chapter 3.



**Figure 2.3** 1.55  $\mu\text{m}$  VCSEL with two wafer bonded GaAs/AlGaAs DBRs

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The bonding process is similar to that widely used in the silicon industry for silicon-on-insulator technologies. The process has also become commercially accepted in the manufacture of vertical cavity lasers[37] and light-emitting diodes[38]. Semiconductor wafer bonding has been used to fabricate a number of novel optoelectronic devices, including vertical cavity amplifiers[39], short wavelength VCSELs on silicon substrates[40] and photodetectors[41, 42].

### **2.3. Optical Properties**

In this section, optical properties of relevant DBR materials are presented and design rules are summarized. Previously derived expressions for peak reflectivity and optical bandwidth are applied to the materials under consideration. Further details on the derivation of these formulas can be found in the relevant literature[43-46].

#### *2.3.1. Reflectivity*

Due to the short gain length of the cavity, VCSEL mirrors must have high reflectivities. The required reflectivities, usually greater than 99%, are obtained by alternating quarter wavelength layers of high and low refractive index materials. Quarter wavelength layers are used so that the multiple reflections add in phase to provide a high total reflectivity over a particular stopband. These

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mirror stacks are known as distributed Bragg reflectors, or DBRs. The peak reflectivity of a DBR in the absence of optical loss,  $R_0$ , is given by[46]:

$$R_0 = \frac{(1 - qap^{m-1})^2}{(1 + qap^{m-1})^2}$$

Equation 2.1

where  $q$ ,  $a$  and  $p$  are refractive index ratios that characterize the incident, mirror and exit media and have values less than 1. These factors and the optical properties of the DBR depend on the sign of the index step between the incident and mirror media, as shown in Figure 2.4. The number of mirror layers (not periods) is given by  $m$ .

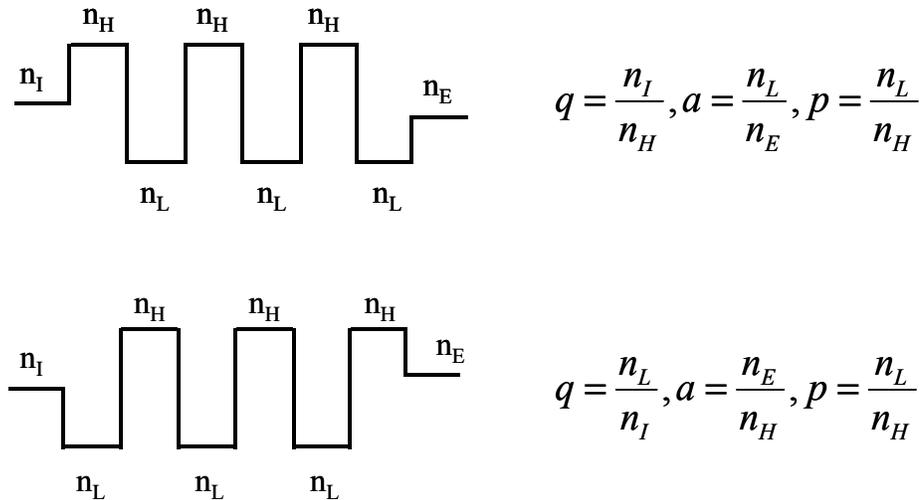


Figure 2.4 Refractive index ratios used in Equation 2.1

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However, the expression for peak reflectivity given above is not complete. The maximum reflectivity must be modified to include the effects of absorption loss, including weak scattering that may be present. The expressions given below are accurate when absorption is low, which is true for VCSEL mirrors. For small loss, we assume that the reflectivity,  $R$ , can be approximated by:

$$R = R_0(1 - A)$$

**Equation 2.2**

where  $A$  is the absorptance. The absorptance is the ratio of power dissipated in the mirror and the power incident on the mirror. The value of  $A$  depends on whether the first mirror medium (index =  $n_1$ ) is the high index layer ( $n_H$ ) or the low index layer ( $n_L$ ):

$$A_{n_1=n_H} = \frac{\lambda n_I (\alpha_L + \alpha_H)}{2 (n_H^2 - n_L^2)}$$

**Equation 2.3**

$$A_{n_1=n_L} = \frac{\lambda \alpha_L n_H^2 + \alpha_H n_L^2}{2 n_I (n_H^2 - n_L^2)}$$

**Equation 2.4**

where  $\lambda$  is the free-space center wavelength of the DBR.  $n_I$ ,  $n_H$ , and  $n_L$  are the refractive indices of the incident, high index and low index media, respectively.

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The absorption coefficients in the high and low index media are given by  $\alpha_H$  and  $\alpha_L$ . Substituting Equations 2.3 and 2.4 into Equation 2.2, the complete expressions for peak mirror reflectivity are given by

$$R_{n_1=n_H} = \frac{(1 - qap^{m-1})^2}{(1 + qap^{m-1})^2} \left(1 - \frac{\lambda}{2} \frac{n_I(\alpha_L + \alpha_H)}{(n_H^2 - n_L^2)}\right) \quad \text{Equation 2.5}$$

$$R_{n_1=n_L} = \frac{(1 - qap^{m-1})^2}{(1 + qap^{m-1})^2} \left(1 - \frac{\lambda}{2} \frac{\alpha_L n_H^2 + \alpha_H n_L^2}{n_I(n_H^2 - n_L^2)}\right) \quad \text{Equation 2.6}$$

The maximum reflectivity of a DBR is limited by index contrast and optical loss. This loss is principally due to absorption, though weak scattering effects may also be considered. Table 2.1 shows optical properties for several different 1.55  $\mu\text{m}$  VCSEL mirror materials. The high index material is named first in the left hand column. The high loss in a-Si is due to bandtail absorption. Optical loss values are assumed to be negligible for undoped material. The effects of doping will be considered later in this chapter. In practice, all materials show some optical loss due to absorption and scattering. Alloy compositions are chosen so that the bandgap energy exceeds that of the design wavelength. This is done in order to limit absorption. The final column shows the number of periods required

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for 99% power reflectivity. These values were collected[47] from a number of prior works[48-52].

DBR Composition	$n_H$	$\alpha_H$ ( $\text{cm}^{-1}$ )	$n_L$	$\alpha_L$ ( $\text{cm}^{-1}$ )	N for 99%
a-Si/SiO <sub>2</sub>	3.60	300	1.45	-	4
a-Si/MgO	3.60	300	1.71	-	5
a-Si/Al <sub>2</sub> O <sub>3</sub>	3.60	300	1.74	-	5
GaAs/AlAs	3.37	-	2.89	-	17
Al <sub>0.15</sub> Ga <sub>0.85</sub> As <sub>0.56</sub> Sb <sub>0.44</sub> /AlAs <sub>0.56</sub> Sb <sub>0.44</sub> ( $\lambda_g = 1.4 \mu\text{m}$ )	3.47	-	3.10	-	22
In <sub>0.68</sub> Ga <sub>0.32</sub> As <sub>0.69</sub> P <sub>0.31</sub> /InP ( $\lambda_g = 1.4 \mu\text{m}$ )	3.45	-	3.17	-	29
AlInGaAs( $\lambda_g = 1.4 \mu\text{m}$ )/Al <sub>0.48</sub> In <sub>0.52</sub> As	3.47	-	3.21	-	29

**Table 2.1 Optical properties of 1.55  $\mu\text{m}$  VCSEL DBRs**

Figure 2.5 compares peak reflectivity versus number of DBR periods for four different 1550 nm VCSEL mirrors from Table 2.1. The four mirror systems shows are a-Si/SiO<sub>2</sub>, GaAs/AlAs, AlGaAsSb/AlAsSb, and InGaAsP/InP. A small uniform loss level of  $10 \text{ cm}^{-1}$  is introduced in the final 3 DBRs in order to illustrate the dependence of saturated reflectivity on index contrast.

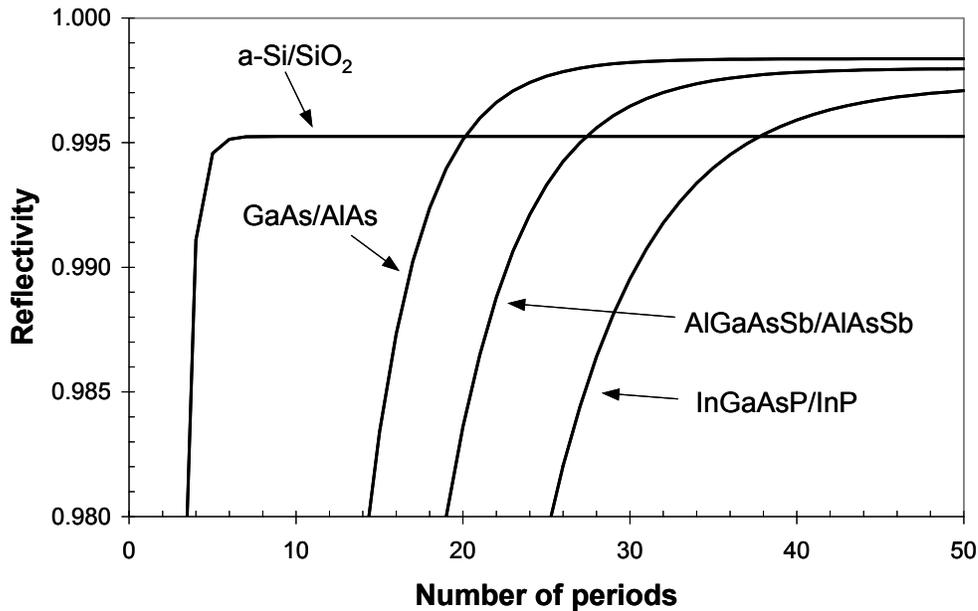


Figure 2.5 Peak reflectivity versus number of mirror periods for different DBR materials

The a-Si/SiO<sub>2</sub> DBR reaches peak reflectivity with a small number of mirror periods, but this value is limited by absorption. This curve is typical of dielectric mirrors. This low reflectivity limits a dielectric DBR to serving as the transmissive mirror in a VCSEL structure. The epitaxial DBRs require a higher number of mirror periods to reach saturation, but are capable of reaching higher peak reflectivities than dielectric DBRs due to lower material absorption. The InGaAsP/InP system is the most commonly grown on InP, but is limited by low index contrast. Long growths are required to reach reasonable reflectivity levels.

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The same is true of AlInGaAs/AlInAs DBRs, not shown in the figure. The AlGaAsSb/AlAsSb system has been studied extensively for DBR applications on InP[4, 53]. This system features significantly higher index contrast than other epitaxial mirrors grown on InP. GaAs/AlAs DBRs have slightly higher index contrast than Sb-based DBRs, requiring fewer periods to reach a given reflectivity.

### *2.3.2. Optical Bandwidth*

The optical bandwidth of a DBR is also an important characteristic. A large bandwidth allows for relaxed growth tolerances, increasing yield. If multiple wavelength or tunable operation is desired, the stopband must be sufficiently wide to provide the desired reflectivity at each operating wavelength. It has been shown that the fractional bandwidth of a mirror is related to the refractive indices by Equation 2.7[54]. The terms  $\Delta\lambda$  and  $\lambda_0$  are illustrated in Figure 2.7.

$$\frac{\Delta\lambda}{\lambda_0} = \frac{4}{\pi} \sin^{-1} \left( \frac{1 - \frac{n_L}{n_H}}{1 + \frac{n_L}{n_H}} \right) \quad \text{Equation 2.7}$$

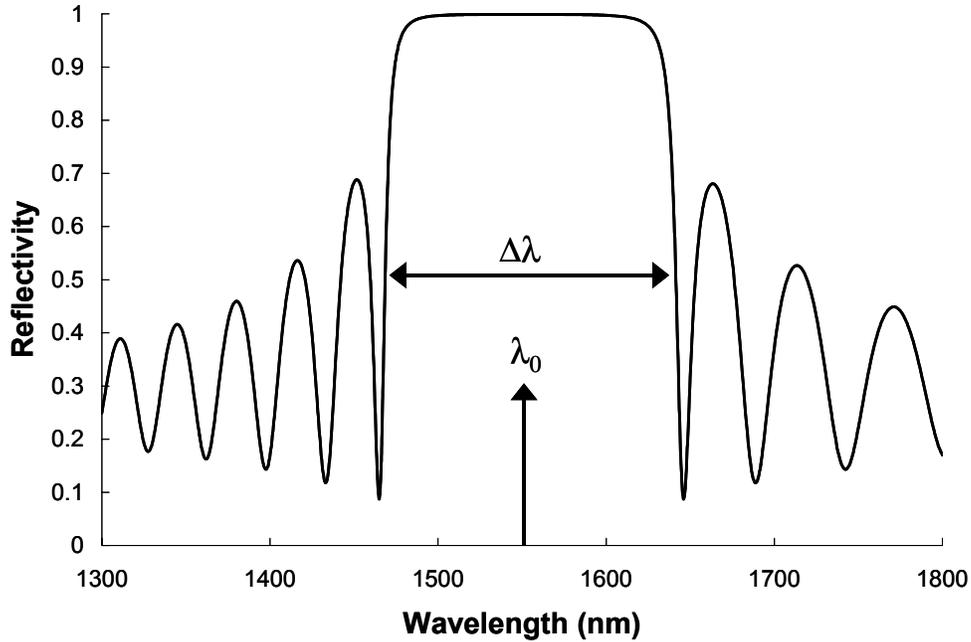


Figure 2.7 Bandwidth and center wavelength of DBR

$\lambda_0$  is the center wavelength of the DBR. It should be noted that that  $\Delta\lambda$  is the full width at half maximum (FWHM) of the DBR stopband. Although the reflectivity is no longer high enough to support lasing near the FWHM endpoints, the fractional bandwidth is still a useful qualitative figure of merit for comparing different DBR media. Table 2.2 shows indices of refraction, fractional bandwidth and bandwidth for common 1.55  $\mu\text{m}$  DBR materials.

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DBR Composition	$n_H$	$n_L$	$\Delta\lambda/\lambda_0$	$\Delta\lambda$ (nm)
a-Si/SiO <sub>2</sub>	3.60	1.45	0.560	868
a-Si/MgO	3.60	1.71	0.463	718
a-Si/Al <sub>2</sub> O <sub>3</sub>	3.60	1.74	0.453	702
GaAs/AlAs	3.37	2.89	0.098	151
Al <sub>0.15</sub> Ga <sub>0.85</sub> As <sub>0.56</sub> Sb <sub>0.44</sub> ( $\lambda_g = 1.4 \mu\text{m}$ )/AlAs <sub>0.56</sub> Sb <sub>0.44</sub>	3.47	3.10	0.072	111
In <sub>0.68</sub> Ga <sub>0.32</sub> As <sub>0.69</sub> P <sub>0.31</sub> ( $\lambda_g = 1.4 \mu\text{m}$ )/InP	3.45	3.17	0.054	83
AllnGaAs ( $\lambda_g = 1.4 \mu\text{m}$ )/Al <sub>0.48</sub> In <sub>0.52</sub> As	3.47	3.21	0.049	77

**Table 2.2** Indices of refraction and bandwidth for 1.55  $\mu\text{m}$  DBR materials

The mirror loss in a laser due to transmission is proportional to  $\ln(1/R)$ . A small decrease in  $R$  can lead to a large increase in threshold gain. Therefore, a large bandwidth is critical to ensure reliable operation over a range of operating conditions. The dielectric mirrors have exceptionally large bandwidths due to their high index contrast. The epitaxial DBRs have lower bandwidths, with GaAs/AlAs and AlGaAsSb/AlAsSb as the only two systems offering a suitable range for robust single and multiple wavelength operation. In fact, the GaAs/AlAs DBR may have suitable bandwidth for simultaneous operation in the EDFA C-band (1530-1560 nm) and L-band (1570-1600 nm). This makes these DBRs particularly desirable for use in next generation VCSELs.

### 2.3.3. Penetration Depth and Diffraction Loss

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The effective penetration depth of the optical field into the DBR is approximated by  $\lambda/4\Delta n$ , where  $\Delta n = n_H - n_L$ [43]. It is apparent that high index contrast reduces the effective penetration depth of the optical field into the DBR. This results in reduced material and free carrier absorption. The calculations above assume incident plane waves and neglect diffraction loss. The effects of diffraction loss have been calculated previously[55]. Diffraction loss increases with the penetration depth. Recent devices feature lateral index guiding for mode confinement, reducing diffraction and scattering losses. This index guiding may be achieved through regrowth, or more commonly with a lateral dielectric aperture. The lateral oxidation of AlGaAs alloys has enabled the fabrication of short wavelength VCSELs with low optical loss[56]. This aperture may also be used to provide current confinement. At this time, a similarly robust aperturing technology on InP is not available, although efforts have been made in selective lateral etching and in the oxidation of Al containing compounds[57, 58].

### *2.3.4. Summary*

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Dielectric DBRs offer reasonably high reflectivities for output mirrors with a short number of mirror periods. However, these DBRs are not sufficiently reflective to serve as the non-transmissive mirror and are difficult to integrate as a bottom mirror in a practical device. Mechanical reliability is also a concern. Traditional epitaxial DBRs on InP are plagued by low index contrast and require arduously long growths to reach desired reflectivity levels. These thick mirrors lead to increased diffraction losses. The recent use of AlGaAsSb as a mirror material has improved optical performance. However, it will be shown that DBRs based on ternary and quaternary alloys have poor thermal conductivity, limiting the prospects for high temperature operation. GaAs/AlAs DBRs may be used as either the transmissive or reflective mirror in a VCSEL, depending on the number of periods. These DBRs offer high reflectivity with reduced thickness compared to DBRs grown on InP. In addition to these favorable longitudinal optical characteristics, the lateral oxidation of AlGaAs compounds may be used to provide transverse optical confinement, further reducing diffraction losses. This aperture may also be used for current confinement. GaAs/AlAs DBRs have sufficient optical bandwidth to support single and multiple channel operation over a wide temperature range.

### **2.4. Thermal Properties**

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The thermal properties of DBRs are of paramount importance. The DBRs comprise the bulk of the VCSEL and must be able to effectively dissipate heat from resistive and lasing processes. This is particularly crucial for long wavelength VCSELs, due to the low characteristic temperature of InP active regions. Dielectric mirrors typically exhibit low thermal conductivities, though materials such as MgO and Al<sub>2</sub>O<sub>3</sub> have been introduced with improved results[21]. The thermal conductivity of epitaxially grown DBRs depends greatly on alloy composition. Ternary and quaternary alloys generally have lower thermal conductivities than binary mirrors, due to alloy scattering[59].

To dissipate heat from the active layer, heat flow must occur through or around the DBRs. Thermal conductance in the radial and longitudinal directions may be calculated knowing the thicknesses and thermal conductivities of the constituent material. It is appropriate to consider radial coordinates due to the cylindrical symmetry of most VCSELs. The following analysis was used by Dudley[60]. Consider a periodic combination of two different material with thicknesses  $d_1$  and  $d_2$ , and thermal conductivities  $\kappa_1$  and  $\kappa_2$  as shown in Figure 2.8.

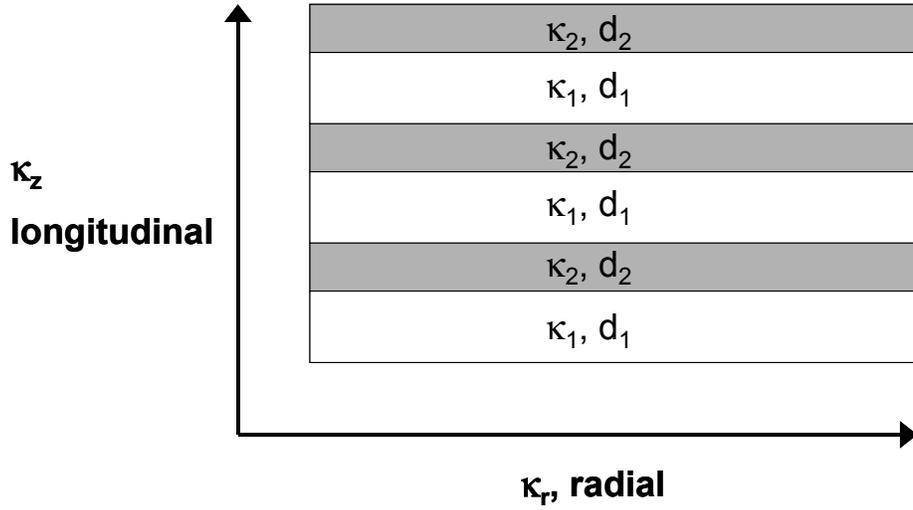


Figure 2.8 Radial and longitudinal thermal conductivity in a DBR

The radial and longitudinal thermal conductivities are given by

$$\kappa_r = \frac{\kappa_1 d_1 + \kappa_2 d_2}{d_1 + d_2} \quad \text{Equation 2.8}$$

$$\kappa_z = \frac{\kappa_1 \kappa_2 (d_1 + d_2)}{\kappa_1 d_2 + \kappa_2 d_1} \quad \text{Equation 2.9}$$

These expressions can be simplified further by considering the optical properties of the DBR. The thickness of each layer,  $d_i$ , is given by  $d_i = \lambda_i / 4n_i$ , where  $n_i$  is the refractive index of the layer. Making this substitution, the thermal

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conductivities in each direction can be written in terms of the refractive indices and the thermal conductivities of each layer.

$$\kappa_r = \frac{\kappa_1 n_2 + \kappa_2 n_1}{n_1 + n_2} \quad \text{Equation 2.10}$$

$$\kappa_z = \frac{\kappa_1 \kappa_2 (n_1 + n_2)}{\kappa_1 n_1 + \kappa_2 n_2} \quad \text{Equation 2.11}$$

The average thermal conductivity for both directions can be calculated by taking the geometric mean of the radial and longitudinal thermal conductivities.

$$\kappa_{avg} = \sqrt{\kappa_r \kappa_z} = \sqrt{\frac{\kappa_1 n_2 + \kappa_2 n_1}{\kappa_1 n_1 + \kappa_2 n_2} (\kappa_1 \kappa_2)} \quad \text{Equation 2.12}$$

The thermal resistance of a DBR depends on the device geometry and any additional materials in the structure. Thermal conductivities in DBRs are significantly reduced from the expected bulk material values by phonon scattering, since the distance between material interfaces is on the order of a mean free phonon length. However, the approximations given above are useful for comparing the relative thermal merits of different DBRs based on their intrinsic material properties. Table 2.3 lists the individual, radial and longitudinal thermal

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conductivities for different DBR materials[47, 59, 61]. The first material listed is referred to with the subscript 1.

DBR Composition	$\kappa_1$ (W/cm K)	$\kappa_2$ (W/cm K)	$\kappa_r$ (W/cm K)	$\kappa_z$ (W/cm K)	$\kappa_{avg}$ (W/cm K)
a-Si/SiO <sub>2</sub>	0.026	0.012	0.016	0.014	0.015
a-Si/MgO	0.026	0.53	0.368	0.073	0.164
a-Si/Al <sub>2</sub> O <sub>3</sub>	0.026	0.36	0.251	0.069	0.132
GaAs/AlAs	0.44	0.91	0.693	0.609	0.650
Al <sub>0.15</sub> Ga <sub>0.85</sub> As <sub>0.56</sub> Sb <sub>0.44</sub> /AlAs <sub>0.56</sub> Sb <sub>0.44</sub>	0.062	0.057	0.059	0.059	0.059
In <sub>0.68</sub> Ga <sub>0.32</sub> As <sub>0.69</sub> P <sub>0.31</sub> /InP	0.045	0.68	0.376	0.088	0.182
AllnGaAs/Al <sub>0.48</sub> In <sub>0.52</sub> As	0.045	0.045	0.045	0.045	0.045

**Table 2.3 Individual, directional and average thermal conductivities for DBR materials**

It should be noted that the thermal conductivity for a-Si is far lower than that of crystalline silicon. The poor thermal conductivity of traditional dielectric mirrors such as a-Si/SiO<sub>2</sub> is apparent. Improved dielectric designs have thermal conductivities similar to that of InGaAsP. The a-Si/SiO<sub>2</sub>, AlGaAsSb/AlAsSb and AllnGaAs/AllnAs combinations behave as thermal insulators. Epitaxial DBRs fabricated using ternary and quaternary alloys generally have low thermal conductivities compared to the binary GaAs/AlAs mirrors. Most of the DBRs that do conduct heat will behave as heat spreaders, since  $\kappa_r \gg \kappa_z$ . Only GaAs/AlAs DBRs allow effective heat transport through the mirror.

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In practice,  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  alloys are used in the formation of DBRs, typically with  $x \geq 0.9$ . This allows the selective oxidation of alloys with  $x \geq 0.98$ . Despite increased alloy scattering in the ternary,  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  maintains a high thermal conductivity over the range of interest, illustrated in Figure 2.9 [62].

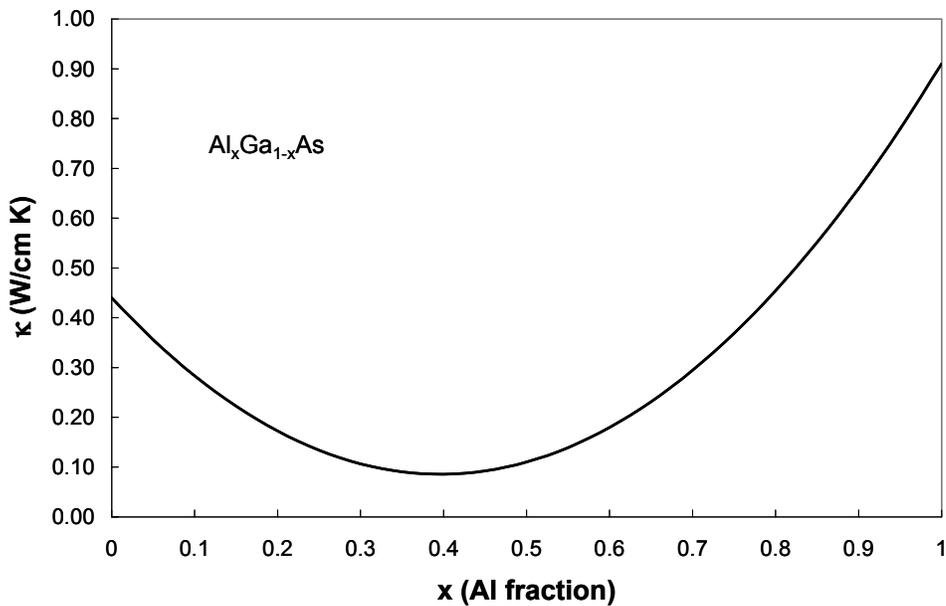


Figure 2.9 Thermal conductivity of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$

### 2.5. Electrical Properties

Current supply through semiconductor DBRs is the simplest and most uniform way to inject carriers into the VCSEL active region. However, doping

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semiconductor mirrors for current transport also increases optical loss, limiting peak reflectivity. A balance must be struck between high reflectivity and low electrical resistance. The voltage across a DBR is determined by the resistance of each mirror period and the potential difference across each of the large number of heterobarriers. The resistance of p-type DBRs is much greater than that of comparable n-type DBRs, due to lower hole mobility and large valence band offsets. In this section, the electrical characteristics of p-GaAs/AlGaAs DBRs are explored. The optical and thermal properties of these DBRs presented in earlier sections indicate their suitability for 1.55  $\mu\text{m}$  VCSELs. Design of p-type DBRs is a greater challenge than n-type due to higher resistance and increased free carrier absorption. The impact of electrical design improvements on optical properties is discussed. One-dimensional simulations of current transport are used to compare different doping schemes.

The resistance of both p- and n-type DBRs have been reduced by choosing appropriate interface grading and doping schemes for flat band structures[63, 64]. The doping levels must be chosen carefully, taking into account the free carrier absorption introduced at the design wavelength. These losses are particularly severe in p-type material. In p-GaAs, the absorption coefficient dependence on hole concentration at 1550 nm is approximately linear and given by  $d\alpha/dp = 29 \times$

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$10^{18} \text{ cm}^2$ , where  $p$  is the hole concentration in  $\text{cm}^{-3}$ [34]. The loss dependence in n-type GaAs is much smaller, with  $d\alpha/dn = 5 \times 10^{18} \text{ cm}^2$ , where  $n$  is the electron concentration in  $\text{cm}^{-3}$ . Interface grading schemes have met with considerable success in long wavelength DBRs at lower doping levels than those used in short wavelength DBRs. In particular, parabolic grading[65] has been used to fabricate low resistance p-DBRs. Parameters for two different p-mirror designs are shown in Table 2.4 and schematically in Figure 2.10. The layers used are GaAs and  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$ . Bi-parabolic grades are formed by two parabolic grades joined in the center of the interface. Uni-parabolic grades are formed by a single parabola.

#	p-GaAs doping	Grade to AlGaAs	p-AlGaAs doping	Grade to GaAs
1 High	6.0E17	uniparabolic, 210 Å 6.0E18	8.0E17	biparabolic, 280 Å, 3.0E18/0.0E18
2 Low	3.0E17	uniparabolic, 210 Å, 1.0E18/3.0E18/1.0E18	4.0E17	biparabolic, 280 Å, 1.0E18/undoped

**Table 2.4 Doping and grade parameters for two p-GaAs/AlGaAs DBRs**

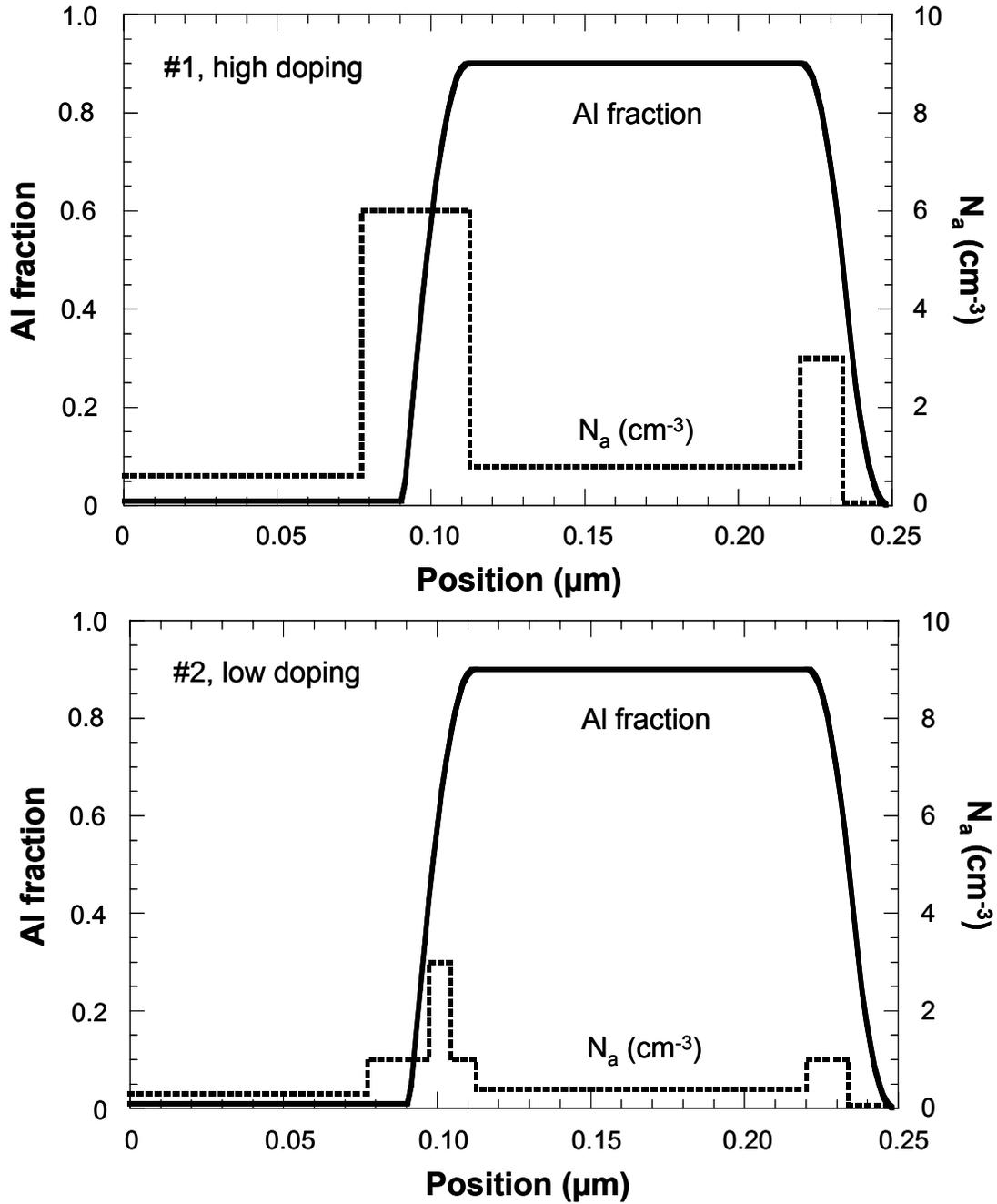
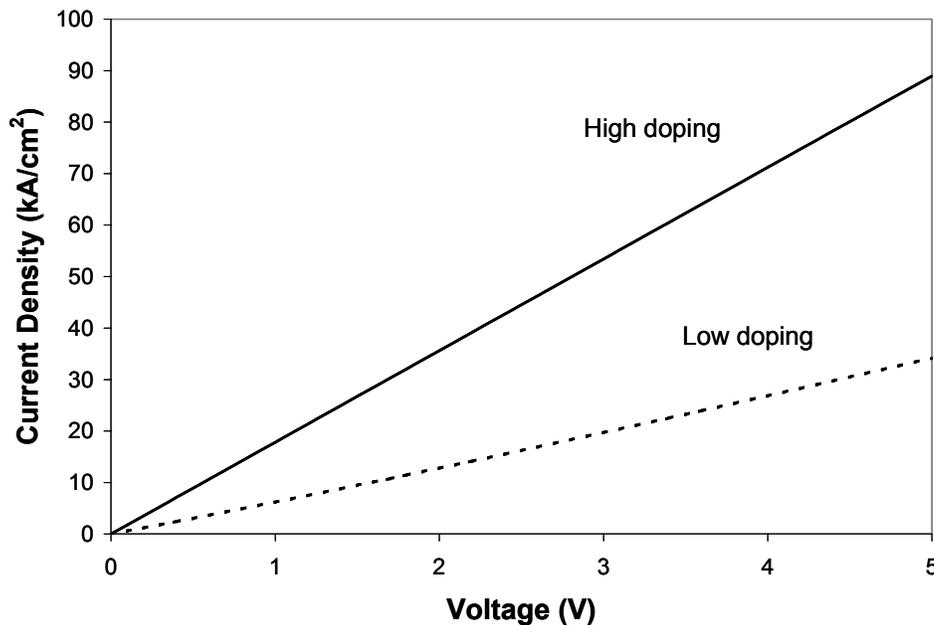


Figure 2.10 Composition and doping profile of graded p-DBRs

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The first design features higher doping in the periods and at the GaAs/AlGaAs interfaces. A common feature to both designs is increased doping in AlGaAs relative to GaAs. This is intended to compensate for the reduced hole mobility in AlGaAs compared to GaAs. The interface doping is higher at the transition from GaAs to AlGaAs. This portion of the DBR is located at a null in the cavity standing wave. As a result, doping can be increased without incurring excessive loss. Cavity design and standing wave patterns will be explored more thoroughly in Chapter 4. Results from a one-dimensional current transport simulation[66] are shown in Figure 2.11 for a 23 period DBR of each type.



**Figure 2.11** Voltage-current density characteristic for high and low doping designs

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As expected, the second mirror is far more resistive. The highly doped mirror passes  $18 \text{ kA/cm}^2$  at 1 V and the low doped mirror passes  $6 \text{ kA/cm}^2$  at 1 V. The eventual design used for portions of this dissertation used 15 highly doped periods far from the active region (where the standing wave intensity is weak) and 8 lowly doped periods close to the active region (where the standing wave intensity is higher). This combination was used to reduce the loss-resistance product, which is an appropriate figure of merit for a conducting mirror. A more complete description of mirror interface grading and the loss-resistance product may be found in work by Hegblom[67]. The cavity and mirror design will be examined more thoroughly in Chapter 4. A 23 period mirror consisting of 15 highly doped and 8 lowly doped periods will pass approximately  $10 \text{ kA/cm}^2$  with a potential drop of 1 V. This current density far exceeds the threshold current density required in long wavelength VCSELs, which is typically on the order of  $1\text{-}4 \text{ kA/cm}^2$ , depending on device size. Although a p-DBR is more resistive than an n-DBR, it is apparent that this p-GaAs/AlGaAs DBR is suitable for VCSEL current injection. It is important to minimize the resistive contribution of the DBR to reduce device self-heating and increase intrinsic bandwidth.

It remains to be seen what the optical properties of this graded, doped DBR will be. Factor  $p$  from Equation 2.1 must be modified to consider non-abrupt

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interfaces. The change in factor  $p$  at the DBR center wavelength for a graded DBR is determined by the following expression[45]:

$$p = \left( \frac{n_L}{n_H} \right)^f \quad \text{Equation 2.13}$$

where  $f$  is the ratio of the fundamental Fourier series coefficient of the index profile with grading to that without grading. The reflectivity spectrum can be calculated using the 1-D transfer matrix method, with standing wave effects considered to calculate the loss contributions at different points in the DBR[43, 68]. Combining electrical and optical calculations, the following result is obtained, where R, T and L denote power reflection, transmission and loss, respectively.

DBR	# of periods	Resistance ( $\Omega \mu\text{m}^2$ )	R (%)	T (%)	L (%)
p-GaAs/Al <sub>0.9</sub> Ga <sub>0.1</sub> As	23	9470	99.39	0.27	0.34

**Table 2.5 Summary of calculated p-GaAs/Al<sub>0.9</sub>Ga<sub>0.1</sub>As DBR properties**

The calculated resistance should be divided by the device area to determine the actual resistance. These results indicate a good balance between electrical and optical properties. The reflectivity is appropriate for a 1.55 VCSEL

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output DBR. The reflective DBR will either be n-doped or undoped in the case of an intracavity contact. In general, higher resistance and optical loss make design of the p-DBR a greater challenge than design of undoped or n-DBRs. A detailed analysis of gain and loss in the optical cavity will be presented in Chapter 4. For a device with a cross-sectional area of  $1000 \mu\text{m}^2$  (diameter =  $36 \mu\text{m}$ ), the expected resistance of the p-DBR is less than  $10 \Omega$ . The measured mirror resistance for this diameter is  $19 \Omega$ , in reasonable agreement with a 1-D calculation. The discrepancy may be attributed to the high lateral mobility in structures grown using carbon as a p-dopant. The low resistance indicates that the mirror will not be a significant contributor to device self-heating and that it is suitable for use in a high-speed structure.

### **2.6. Summary**

In this chapter, the optical and thermal properties of  $1.55 \mu\text{m}$  VCSEL DBRs were considered. The GaAs/AlGaAs system was shown to have suitable qualities, including high reflectivity, high thermal conductivity and low electrical resistance. These DBRs can serve as a transmissive or reflective VCSEL mirror. An oxide aperture may be introduced for lateral index guiding. GaAs/AlGaAs mirrors have been shown to provide the most effective path for heat dissipation among long wavelength DBRs. The electrical characteristics of doped, graded p-

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GaAs/AlGaAs DBRs were found to be suitable for high-speed, low power operation. Effective current transport may be achieved without compromising the optical properties of the DBR. The reliability and robust fabrication of these mirrors have been demonstrated in commercial short wavelength devices. The next chapter discusses the concept of wafer bonding as a method for integrating GaAs/AlGaAs DBRs with InP-based active regions.

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## **3. Wafer Bonding**

### **3.1. Introduction**

In the previous chapter, the optical, thermal and electrical qualities of GaAs/AlGaAs DBRs were shown to be favorable for use in long wavelength VCSELs. However, the most common materials for long wavelength active regions are InGaAsP and AlInGaAs on InP substrates. Conventional growth techniques are limited to strained layer growth of GaAs on InP, with a critical thickness of 1 nm according to the Matthews-Blakeslee criteria[1]. Films beyond this thickness have an unacceptably high density of threading dislocations and are not suitable for device fabrication. Metamorphic growth of GaAs on InP has been demonstrated[2, 3]. However, it is expected that these structures will contain threading dislocations, potentially compromising device reliability.

Reproducibility and stability under thermal cycling are also areas of concern.

Wafer bonding allows the heterogeneous integration of materials with different lattice constants. A direct chemical bond is established at the heterointerface between two semiconductor materials. This allows the fabrication of devices with optimized material qualities, rather than those dictated by a particular lattice constant. The lattice mismatch is accommodated by non-mobile misfit dislocations that are not expected to affect device reliability. There is no evidence

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of threading dislocations. This technique enables a host of integration possibilities for the fabrication of optoelectronic devices including InGaAs:Si photodetectors[4], AlInGaP:GaP light emitting diodes[5] and GaAs:InP vertical cavity lasers[6].

In this chapter, the process of wafer bonding is discussed. The principal focus is GaAs:InP bonding for integration of GaAs/AlGaAs DBRs with InGaAsP/InP active regions, motivated by the favorable optical, thermal and electrical properties of GaAs-based DBRs presented in Chapter 2. The bonding process used in the course of this dissertation is described in detail. Structural, optical and electrical characteristics of bonded materials are summarized. Two unique contributions to the field of wafer bonding are introduced. The first is the introduction of a superlattice barrier layer to prevent defect propagation during the bonding process. The second is the use of those superlattice layers to define multiple wavelength cavities.

### **3.2. Process**

In direct wafer bonding, the surfaces under consideration are bonded without the use of an intermediate layer such as metal or adhesive. The ultimate goal is an atomically bonded junction. This is required for an electrically

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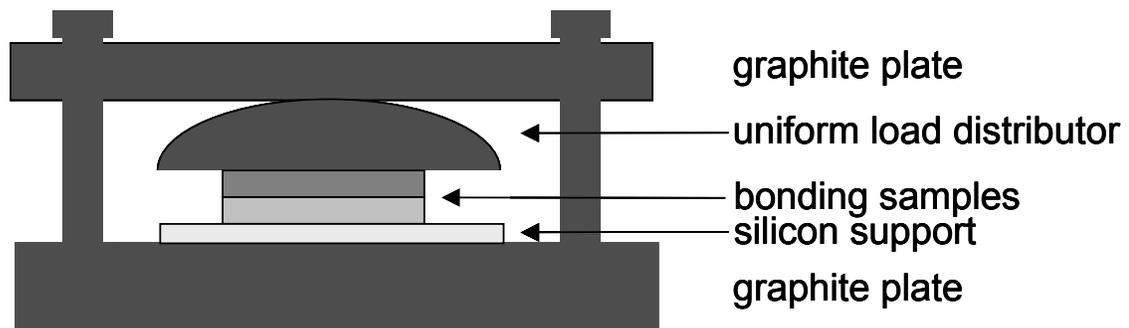
conductive and optically transparent interface. It is critically important to have surfaces free from oxides and organic contaminants. To this end, a thorough cleaning process is used prior to bond formation. One of the surfaces is patterned and etched with a grid-like pattern of channels prior to bonding[7]. These allow for the escape of trapped gas and liquid during a later thermal anneal stage. A channel pitch of 250  $\mu\text{m}$  in both directions and a depth of 1000  $\text{\AA}$  have proven to be suitable. The channel itself is 5-10  $\mu\text{m}$  in width. This channel layer contains alignment marks used in later lithographies. Surface morphology is also a relevant issue. Using smooth surfaces with low defect densities reduces the number of voids in bonded structures.

After solvent cleaning with acetone and isopropanol, the wafers are dried and heated to desorb any excess solvent. Great care was taken to ensure that the patterned surface was free of photoresist residue after solvent cleaning. An oxygen plasma was used to remove volatile hydrocarbons from the wafers. The surface oxide formed was etched away using a reducing solution. A thorough analysis of surface roughness and interface contamination caused by various reducing agents was performed by Black[8]. Based on that work,  $\text{NH}_4\text{OH}$  was used to benignly remove the oxide formed by the plasma. A second oxidation step is performed in order to incorporate all possible surface contaminants into an

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oxide that can be easily removed. This second oxidation was carried out using ultraviolet ozone[9]. After this step was completed, the resulting oxide was removed using dilute HF and then  $\text{NH}_4\text{OH}$ .

After the cleaning steps are complete, the wafers are pressed together in a graphite fixture and thermally annealed. The wafers are kept in  $\text{NH}_4\text{OH}$  and then a non-oxidizing solvent such as methanol until they are placed in contact and inserted into the fixture. A schematic of the fixture is shown in Figure 3.1.

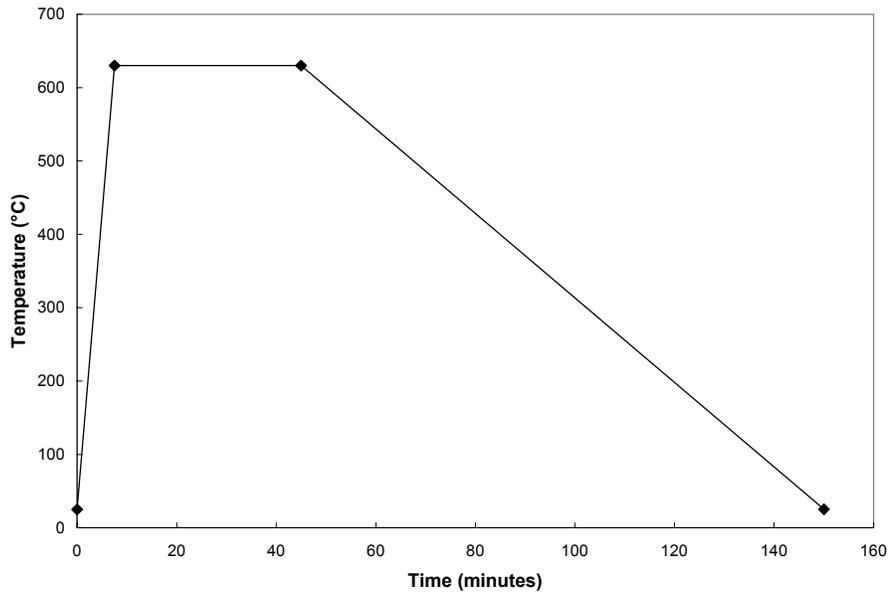


**Figure 3.1** Schematic of graphite bonding fixture. Pressure is applied by controlling torque on top screws (three or four). Dome piece is used for even load application. Silicon support provides a rigid, flat surface during the bonding process.

The torque applied to each screw determines the bonding pressure. Typical pressures used were between 1 and 3 MPa, calibrated using a strain gauge. Uniform pressure application is essential to the bonding process. The

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hemisphere is used to evenly distribute the applied load. Bonding temperatures ranged from 580 to 640°C in a quartz tube furnace filled with a nitrogen ambient. Anneals at or near the growth temperature are required for the formation of a rugged covalent bond. The furnace temperature is elevated to the anneal temperature at a rate of 85°C per minute. The wafers are held at the maximum temperature for 30-40 minutes. The wafers are then cooled at 5-10°C per minute to avoid cracking due to mismatch between thermal expansion coefficients. A typical temperature profile is shown in Figure 3.2. Sample sizes used in this work were typically 1 cm x 1 cm. It should be noted that this size limitation was largely imposed in order to conserve material. In fact, 2” wafer bonding processes are used in the fabrication of commercial optoelectronic devices[5, 10].



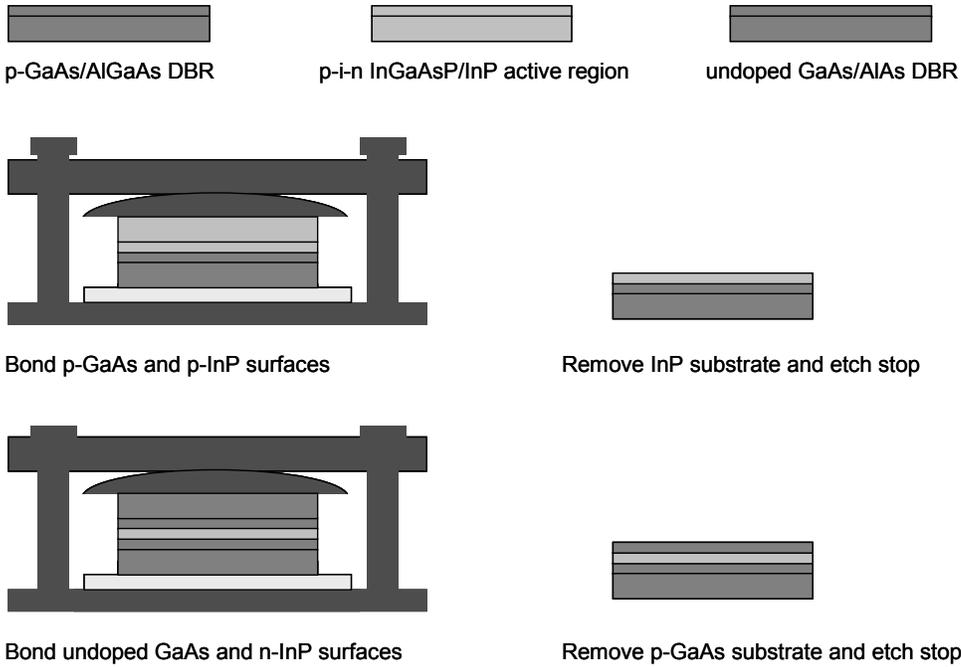
**Figure 3.2** Typical temperature profile used during bonding process

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Following the thermal anneal, one of the substrates must be removed in order to facilitate further processing. An etch stop layer is included in the epitaxial structures so that substrate removal terminates at the desired point. InP substrates are removed using a 3:1 HCl:DI (deionized water) solution. This solution has an etch rate of  $\sim 8 \mu\text{m}$  per minute and will stop on InGaAs/InGaAsP layers. These etch stops are removed using 3:1:50  $\text{H}_3\text{PO}_4\text{:H}_2\text{O}_2\text{:DI}$  which stops on InP. GaAs substrates are removed using a spray etcher[11] and a 30:1  $\text{H}_2\text{O}_2\text{:NH}_4\text{OH}$  solution that stops on high Al content AlGaAs layers ( $x > 0.7$ ). This etch stop is removed using 1:10 HF:DI, leaving a GaAs surface exposed. In the case of a double wafer bonded VCSEL structure, the bonding process is repeated after InP substrate and InGaAsP etch stop removal. After the second bond, a GaAs substrate is removed. The double bonding process is illustrated in Figure 3.3, leaving an InP epitaxial film between two GaAs epitaxial films on a GaAs substrate.

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Start with three wafers:



**Figure 3.3** Double bonding process, leaving InGaAsP/InP active region between two GaAs/AlGaAs DBRs on a GaAs substrate

The wafer bonding process for compound semiconductors was initially proposed by Liao[12]. The process summarized above was developed at UCSB and applied to the fabrication of bonded VCSELs by numerous researchers, including Dudley, Babic, Margalit and Black. Further details on the bonding

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process and analysis of the bonded junction can be found in their publications and dissertations [13-16].

### 3.3. Structural Analysis

Scanning electron microscopy (SEM) was used to obtain information about void density and interface quality. An image of a double-bonded VCSEL structure is shown below. The bonded junctions appear smooth and no deformation of the mirror periods is observed.

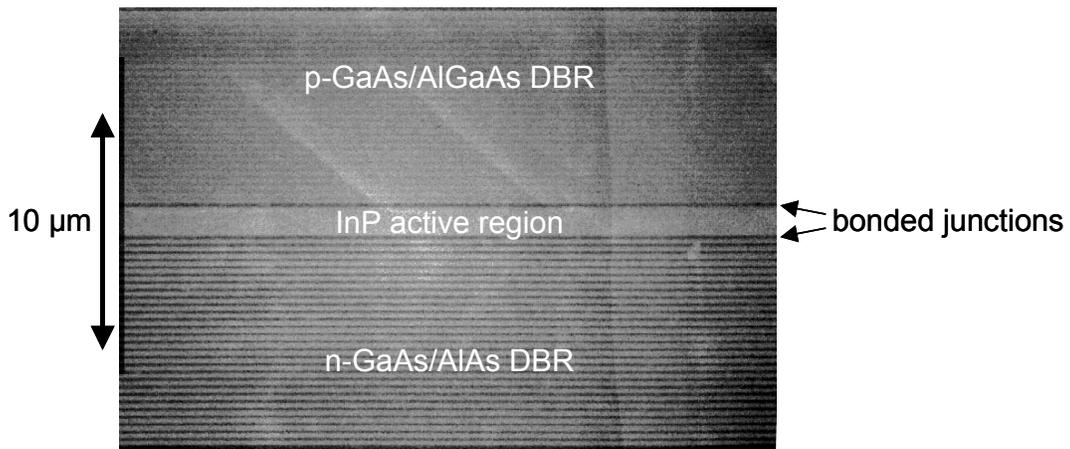
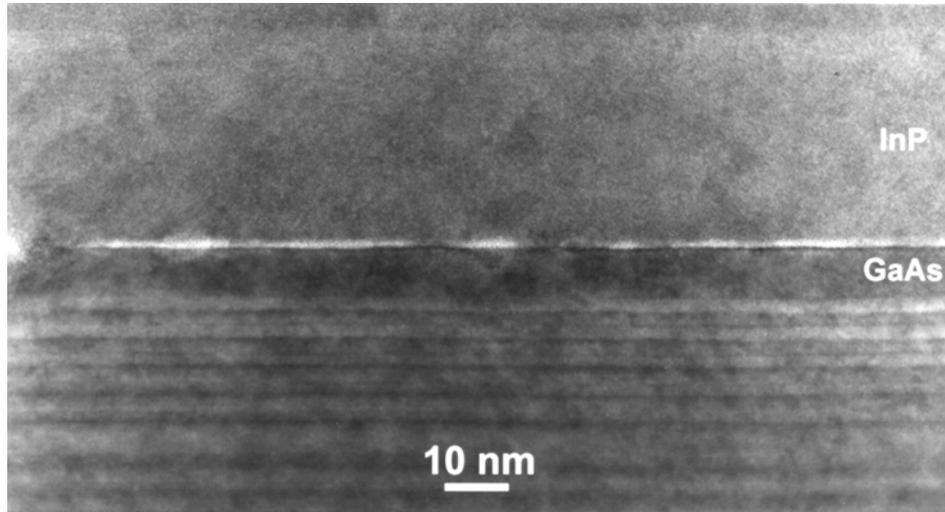


Figure 3.4 Scanning electron microscopy (SEM) image of double bonded structure

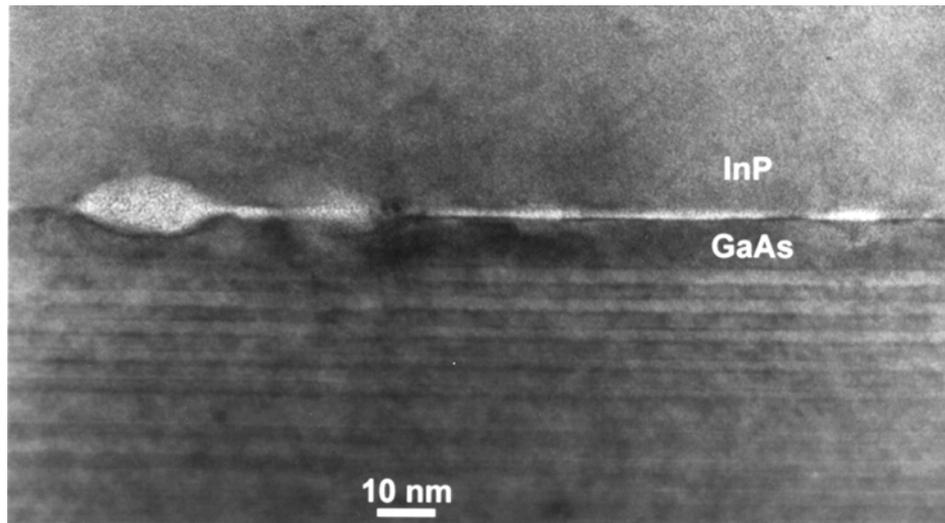
### *Chapter 3: Wafer Bonding*

However, more rigorous techniques are required in order to thoroughly evaluate the bonding process. Recent collaboration between UCSB and Jin-Phillipp at MPI-Stuttgart has resulted in a more complete understanding of bond formation[19]. Analysis tools used by Jin-Phillipp included high-resolution transmission electron microscopy (HRTEM) and energy dispersive x-ray spectroscopy (EDS). During the bonding process, an edge dislocation network is formed to relieve strain, accommodating lattice mismatch at the bonding temperature and tilt misorientation. A third dislocation network forms during cooling to relax thermal misfit due to the difference in thermal expansion coefficients between GaAs and InP. Bonding at lower temperatures would reduce the density of these dislocations. No evidence of threading dislocations was found, confirming the observations of other authors[17, 18, 20]. TEM images of the bonded interface are shown in Figures 3.5a and 3.5b.

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**Figure 3.5a** TEM image of GaAs:InP bonded junction, courtesy of N-Y. Jin-Phillipp. Interface is of high quality with no intermediate layer.



**Figure 3.5b** TEM image of GaAs:InP bonded junction, courtesy of N-Y. Jin-Phillipp. Interface contains thin amorphous layer.

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In some cases, the interface contains a thin amorphous layer as shown in Figure 3.4. Analysis of the diffraction pattern indicates that the crystalline phase may be  $\alpha$ -Ga<sub>2</sub>O<sub>3</sub>. Amorphous native oxides of Ga are known to form crystalline islands during high temperature anneals[21]. The amorphous layer is likely due to incomplete removal of native oxide prior to the bonding process. Due to equipment limitations, the final bond is performed in atmospheric conditions. This inevitably results in the formation of a thin native oxide prior to bonding. Secondary ion mass spectroscopy analysis performed by Charles Evans and Associates confirms high oxygen content and also suggests high levels of carbon and hydrogen, perhaps as a result of solvent cleaning or immersion in solvent prior to bonding[8]. Although this interface layer is quite thin, it is thought to affect the electrical characteristics of the bonded junction, as will be discussed later in this chapter. Mobile dopants such as Zn and Be also accumulate at the bonded interface. Significant interdiffusion of Ga, As, In, and P is observed in EDS measurements. In diffuses deeper into GaAs layers than P and As diffuses more deeply into InP than Ga. During the thermal anneal, group V elements P and As dissociate from InP and GaAs, then diffuse toward the interface. Diffusion of In is enhanced by the presence of Zn dopant. It is thought that Zn dopant atoms may occupy In atomic sites and promote In diffusion toward and across the

interface. Mass transport during the high temperature process smoothes the junction and joins separated half-planes.

### **3.4. Optical Analysis**

The optical impact of wafer bonding is important in two respects. The optical loss introduced by the bonded junction must be low in order to maintain an optically transparent interface in the VCSEL structure. Additionally, the bonding process should not degrade the optical properties of DBR and quantum well structures. Measurements by Liu indicate that the optical loss due to the bonded junction is no greater than  $0.5 \text{ cm}^{-1}$ [22]. Considering the short interaction length, the expected round trip loss contribution from the junction in a VCSEL structure can be neglected. Cavity designs used in the course of this work placed the bonded junctions at nulls in the standing wave pattern, further reducing possible optical losses. The surface roughness of bonded films is comparable to that of conventionally grown epitaxial layers, resulting in negligible scattering losses[20]. The optical properties of wafer bonded GaAs/AlGaAs DBRs are maintained through the bonding process, with no meaningful impact from thermal or strain induced disordering[23]. Depth-resolved photoluminescence measurements by Black[16] show that luminescence from both GaAs and InP quantum well structures are reasonably well-preserved through the bonding

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process, although there is some loss in luminescence for quantum wells and strained quantum wells within 300 nm of the bonded junction. This material degradation may be reduced by the use of group V (P, As) overpressure during the bonding process. A shift in peak photoluminescence wavelength is observed. Thermal cycling using the bonding conditions results in a blueshift. However, the bonding process introduces a competing redshift. These effects result from a complex combination of atomic interdiffusion, strain relaxation and defect diffusion. The use of a superlattice barrier between quantum well regions and the bonded junction to reduce the number of non-radiative recombination centers will be discussed in Section 3.6 along with further details on the effects of bonding quantum well structures.

### **3.5. Electrical Analysis**

Carrier transport across bonded heterojunctions is also an area of interest. Long wavelength VCSELs require low electrical resistance in order to reduce device self-heating. This self-heating reduces carrier confinement and shifts the optical gain peak with respect to the longitudinal cavity mode. The electrical properties of bonded InP:GaAs junctions have been studied using current-voltage characteristics (I-V), capacitance-voltage characteristics (C-V), admittance spectroscopy and electron beam induced current (EBIC) measurements. Ohmic

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conduction has been achieved for n-GaAs:n-InP bonded junctions. Admittance spectroscopy[23] and the fitting of experimental curves to thermionic emission models[18] indicate a conduction band offset ( $\Delta E_c$ ) of 0.3-0.4 eV at the n-n bonded junction. These figures are in reasonable agreement with theoretical predictions[24, 25]. A value of 0.05 eV has been calculated for the valence band offset ( $\Delta E_v$ ), although the corresponding value for  $\Delta E_c$  is not in agreement with those given above[26]. A turn-on voltage of 1-2 V is observed for p-GaAs:p-InP bonded junctions at the current densities required to support a practical device (1-10 kA/cm<sup>2</sup>), with high resistance for hole transport. A typical I-V characteristic for a p-GaAs:p-InP bonded junction is shown below.

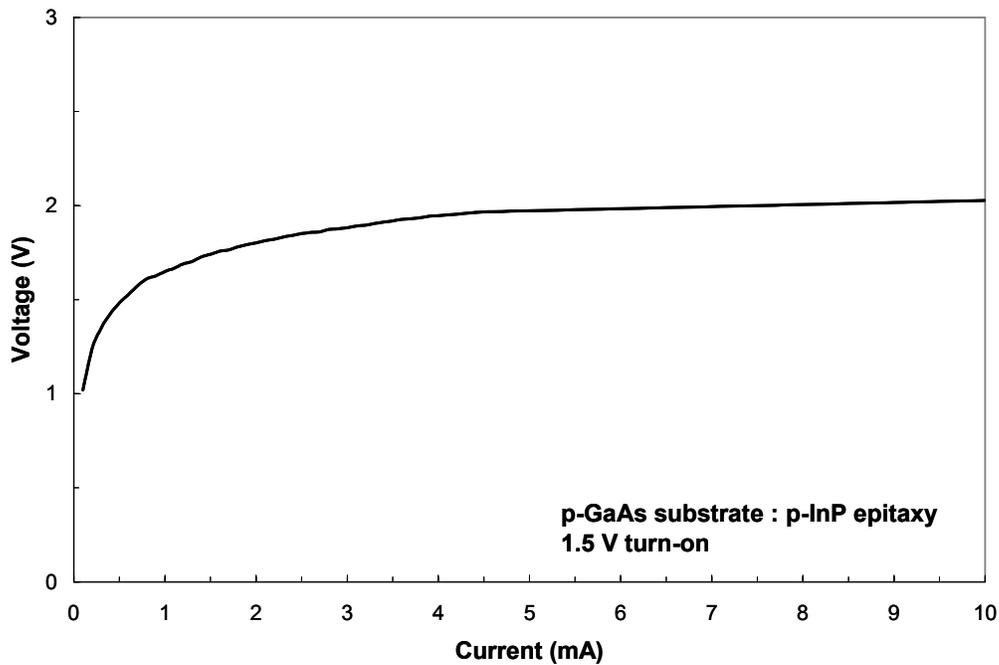


Figure 3.6 Typical I-V characteristic for a p-p bonded junction with no active region

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This turn-on behavior is consistent with the formation of an interface donor charge layer with density greater than  $10^{12}/\text{cm}^2$ . These charges may be due to an interface layer, dangling bonds or a combination of the two. The calculated donor charge density is on the same order as the expected dangling bond density. The precise nature of carrier interaction with this charge layer is unknown. I-V curves suggest that low mobility holes encounter a resistive barrier. The turn-on voltage was present in all p-GaAs:p-InP junctions fabricated, regardless of surface preparation, doping, or contamination levels. This suggests that the contamination levels in all fabricated devices exceed those required for improved conduction or that the voltage drop is independent of the contamination level. A schematic band diagram at 2 V forward bias is shown in Figure 3.7.

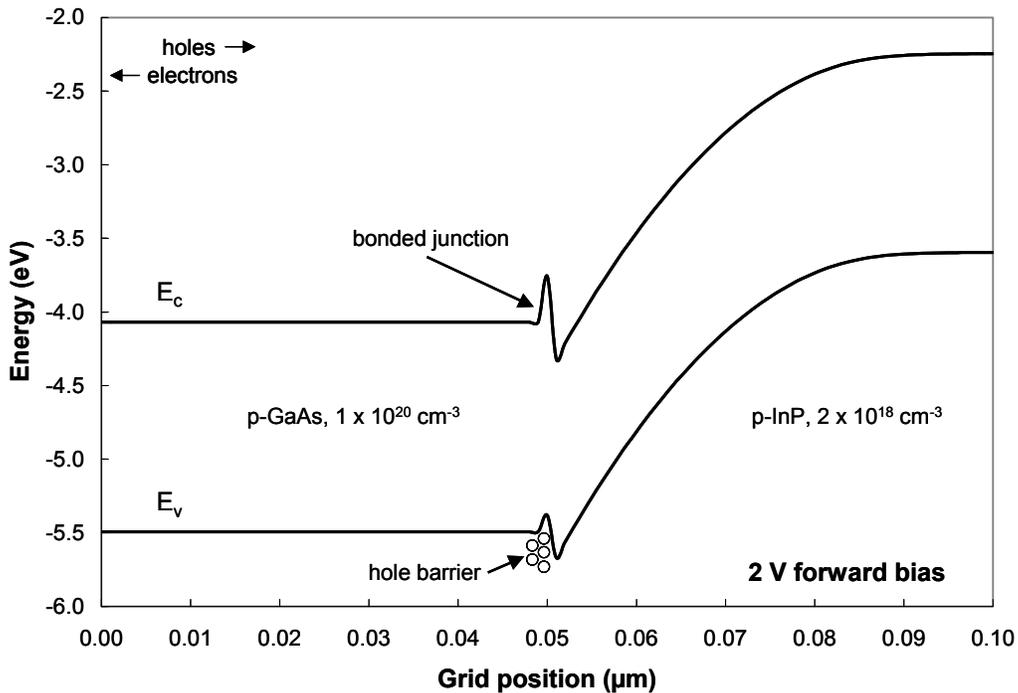


Figure 3.7 Representation of band diagram at p-GaAs:p-InP bonded junction

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The interface charge layer creates a barrier to hole transport. In p-p bonded junctions, this barrier contributes to high turn-on voltage and resistance. In bonded VCSEL structures, the p-p junction may serve as a significant non-radiative recombination site, due to electron overshoot of the active region. High p-type doping or implantation may compensate the interface charge or disorder any interface layer. In theory, perfect in-phase bonding should reduce the interface charge density and forward voltage[27, 28]. Attempts were made to bond p-GaAs and p-InP in orientations with matched dangling bond densities. However, the rough surface morphology of these off-axis growths resulted in poor bonding and a high turn-on voltage. In practice, the voltage-current characteristics of [001] GaAs on [001] InP are orientation independent and no special care is taken to align wafers in a particular orientation prior to bonding.

EBIC analysis has been used to measure the location and density of electrically active defects in bonded diode structures[23]. Locally generated electrons and holes are swept out by the built-in electric field and collected at the device contacts. Although dark-line defects were observed at the bonded junction, a negligible dark-line density was observed at a distance of 0.4  $\mu\text{m}$  from the interface. This suggests that the bonding process does not degrade InP structures at a distance of 0.4  $\mu\text{m}$  from the bonded interface. The VCSEL structures

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fabricated during the course of this dissertation had gain regions positioned at an appropriate distance from the bonded junction to reduce the likelihood of degradation during bonding. In addition, a superlattice barrier was introduced to reduce the number of non-radiative recombination centers in bonded InP active regions.

#### **3.6. Superlattice Barrier**

The dislocations generated during the bonding process are not mobile at ordinary device operating temperatures. However, these dislocations may initially be established in unfavorable locations. Defects in the InP cladding may result in non-radiative recombination, limiting laser efficiency. Defects residing in the quantum well region reduce available gain and could prevent device operation altogether. Although previous analysis showed limited defect propagation, further methods of controlling defect generation and propagation during the bonding process are desirable. To this end, a superlattice barrier was added to the p-InP cladding, shown in Figure 3.8.

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**Figure 3.8 InGaAsP/InP p-i-n active region with superlattice cap**

The highly strained nature of the bonding GaAs:InP interface makes it a favorable sink for dopants and defects. However, the VCSEL active region also contains strained interfaces at the well-barrier boundary. Strained active regions are used to lower the current density required for transparency and enhance the differential gain[29]. These strained interfaces are also favorable sinks for dopants and defects. Misfit dislocations generated during the bonding process may reside in the InP cladding, or more significantly in the quantum well region. It is thought that imposing a superlattice buffer between the bonded junction and the InP active limits defect propagation, reducing the number of non-radiative recombination centers in the cladding and quantum wells. The use of superlattice buffer layers for epitaxial dislocation control is well known and has been studied in a number of material systems[30-32]. A superlattice barrier was first incorporated into

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bonded InP active regions in 1999 at UCSB[33]. Results from this and subsequent work with superlattice barrier active regions are summarized below.

During the high temperature bonding process, significant dopant and defect diffusion takes place. Zinc is an exceptionally mobile species and diffuses along with point defects from the active region. Strain relaxation and thermal effects contribute to atomic interdiffusion at the well-barrier interfaces. The bonding process introduces additional strain relaxation effects and potential dislocations in the active region. The combination of these thermal and stress effects can be harmful to the quality of the bonded active region.

Photoluminescence spectra from a highly strained active region without a superlattice cap are shown in Figure 3.9. The solid line shows luminescence from the as-grown active region. The dotted line shows luminescence from the same active region after being thermally cycled under the temperature profile used for bonding. No pressure was applied. A loose GaAs substrate was placed over the sample to provide group V overpressure and prevent surface degradation. The dashed line shows luminescence from the structure after wafer bonding to GaAs. The InP substrate and InGaAsP etch stop have been removed. The same active region structure was used for all three measurements.

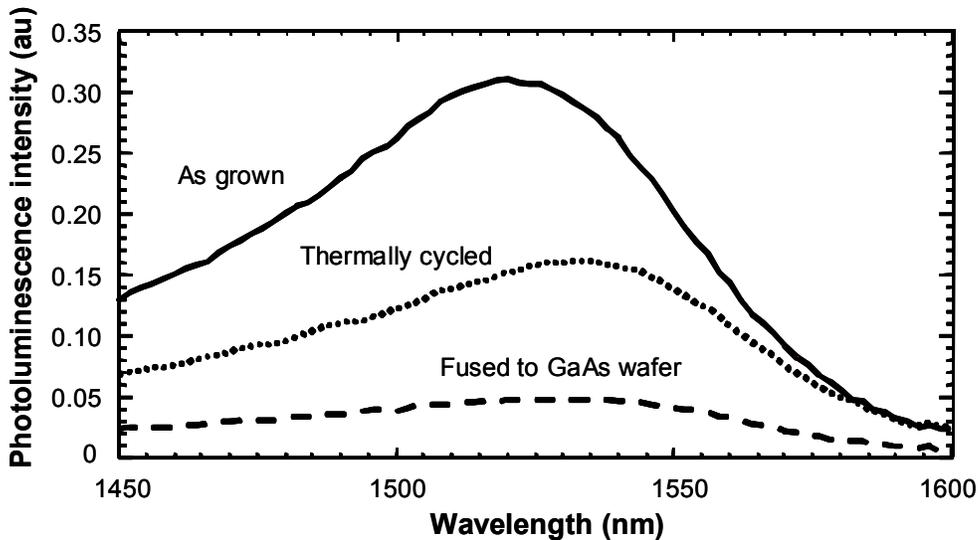


Figure 3.9 Photoluminescence intensity from as-grown, thermally cycled and bonded active regions. The active region contained 6 strained InGaAsP quantum well between a Zn-doped p-InP cladding and a Si-doped n-InP cladding.

Thermal cycling diminishes and wavelength shifts quantum well luminescence by encouraging atomic interdiffusion at the well-barrier interface. Zinc diffusion through quantum wells also compromises active region integrity. Photoluminescence from the bonded active region is severely degraded relative to both the as-grown and thermally cycled cases. It should be noted that this was a highly strained active region and that the degradation encountered was not typical. It may be inferred that the decreased luminescence in the bonded active region is not entirely due to thermal processes, since the thermally cycled active region shows a smaller reduction in luminescence intensity. The remaining decrease is attributed to strain relaxation processes and the possible introduction of dislocations into the active region. The use of an intracavity superlattice was

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initially motivated by the multiple wavelength design discussed in Section 3.7. However, it was discovered that bonded active regions with a superlattice barrier had enhanced luminescence compared to as-grown active regions. Results for active regions with and without superlattice caps bonded to undoped GaAs substrate are shown in Figure 3.10. The cap consisted of four periods of p-InP/p-InGaAsP ( $\lambda_g = 1.3 \mu\text{m}$ ). Each layer was 7.5 nm thick. The peak luminescence wavelength for the superlattice was at 1270 nm. Residual luminescence near 1270 nm after superlattice removal is due to the InGaAsP etch stop layer. For samples without a cap, the superlattice was removed using selective wet etches. Quantum well luminescence peak is not affected by etching off the superlattice periods.

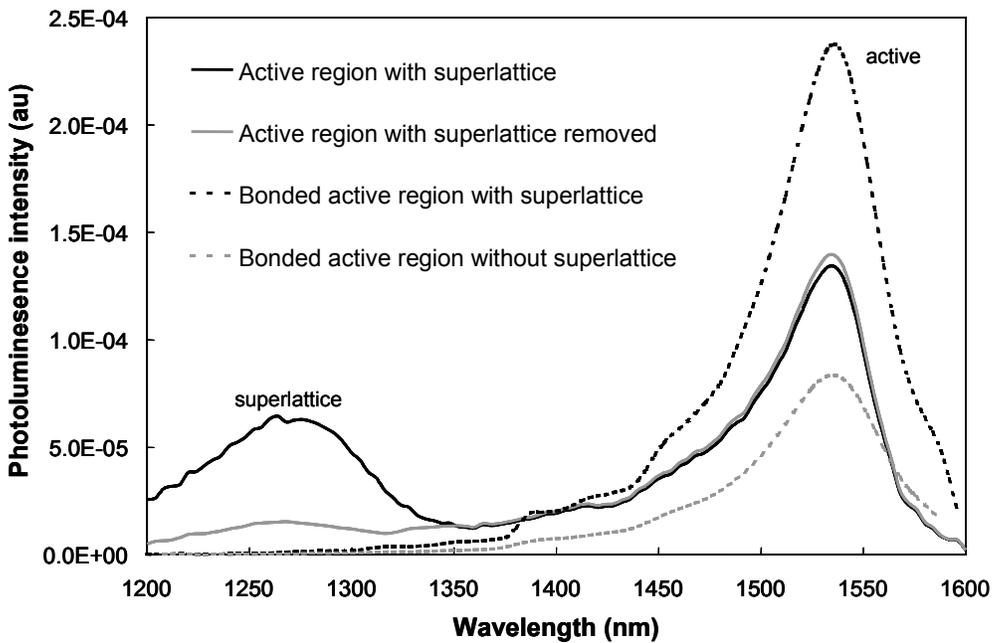


Figure 3.10 Photoluminescence from active region with superlattice and with superlattice removed. Solid lines show PL intensity prior to bonding. Dashed lines show PL intensity after bonding and substrate removal.

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Active region luminescence is not only preserved by the addition of an intracavity superlattice; it is enhanced! It is believed that the superlattice acts as a defect-blocking layer. Although misfit dislocations are still generated by the bonding process, the superlattice blocks their propagation into the InP cladding and active region. The concept of strain relaxation and defect accumulation in the superlattice layers is supported by the decreased luminescence from the bonded superlattice. Under thermal cycling, the strained well-barrier interfaces are the most favorable sink for dopants and active region defects. During bonding, the highly strained GaAs:InP interface is also a highly attractive gettering center. Without a superlattice barrier, the bonding junction acts as a net source for defects, gettering active region defects but generating misfit dislocations. With a superlattice barrier, the propagation of misfit dislocations is blocked and the bonding junction behaves as a net defect sink, increasing active region photoluminescence. The enhanced luminescence suggests that bonded VCSELs fabricated with superlattice-capped active regions will have fewer non-radiative recombination centers, resulting in higher internal and differential efficiencies. These expectations were confirmed in multiple generations of devices[34]. VCSEL design and results will be discussed extensively in Chapters 4 and 5.

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Although experiments were conducted with superlattices at both bonding interfaces, the superlattice is thought to be more relevant during the first bonding than the second. Intuitively, the first bond is less forgiving than the second since roughly equal amounts of material with dissimilar lattice constants are being bonded. However, the second bond is performed under more elastic conditions, with only a thin layer of mismatched material between GaAs substrates and unstrained epitaxial layers. These conditions are thought to be less conducive to dislocation formation, particularly after the strain relaxation processes that take place during the first bond.

It is possible for the superlattice structure to be further optimized. Due to material limitations, only the four period superlattice described above was used in bonding experiments and VCSEL fabrication. Varying the superlattice composition or number of periods could yield improved results. Strained-layer superlattices (SLS) have been used extensively as buffer layers in mismatched heteroepitaxy[35] and may be effective during the bonding process as well. These SLS structures create a strain field, causing impinging dislocations to be bent along the superlattice interface planes. Further investigation should include varying superlattice conditions and probing of the bonded superlattice and surfaces to confirm defect accommodation.

### **3.7. Multiple Wavelength Cavity Definition**

The intracavity superlattice discussed above may also be used to define multiple cavity wavelengths prior to bonding. Different numbers of superlattice periods are removed in adjacent regions using selective wet etches. This creates a physical cavity length difference between neighboring cavities that results in different lasing wavelengths for neighboring devices. This tuning method was proposed by Jayaraman and used to fabricate optically pumped, multiple wavelength VCSEL arrays by depositing dielectric mirrors over the patterned surface and bottom DBR[36]. Although these were 1.55  $\mu\text{m}$  VCSEL arrays, external optical pumping is undesirable for low cost sources as it adds cost and complexity. The primary contribution of this dissertation is the fabrication of electrically pumped, directly modulated multiple wavelength VCSEL arrays using an intracavity superlattice tuning layer prior to wafer bonding. The array elements share the same active region and DBRs.

Due to the short cavity length, only a small perturbation is required to shift the cavity mode. The amount of the shift is determined by the effective cavity length of the VCSEL and the optical path length of the material removed. In this work, a  $3\lambda/2$  active region was used. This thickness was chosen in order to

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distance the quantum well region from the bonded junction while still providing a low loss cavity. Using the one-dimensional transfer matrix method[39], the expected shift in cavity wavelength for removal of InP and InGaAsP ( $\lambda_g = 1.3 \mu\text{m}$ ) material from this active region was calculated. The nominal cavity wavelength was 1550 nm. Results are plotted below. The change in slope between the two curves is due to the difference in refractive index between the two materials. The curvature of the shift characteristic is due to the greater perturbation caused by removal of a given amount of material in a shorter cavity.

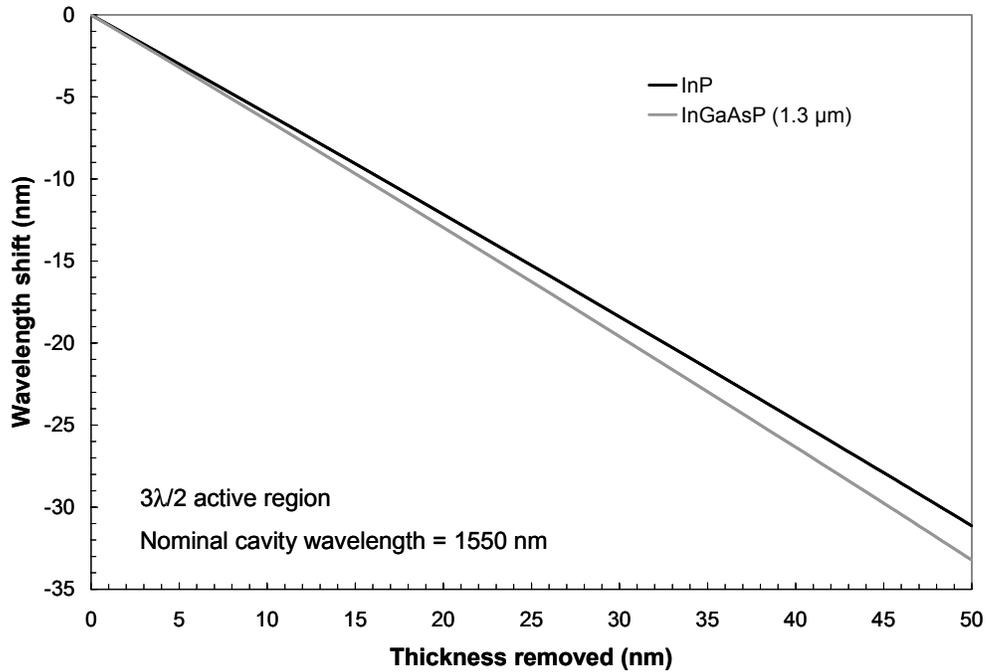


Figure 3.11 Wavelength shift versus thickness of InP or InGaAsP material removed

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The cladding etch depth may be controlled in a repeatable manner by using an InP/InGaAsP superlattice cap. The superlattice layers ensure a reproducible etch depth and smooth etch stop surface for wafer bonding. An interesting feature of this type of surface patterning is that  $N$  lithography and etch steps are used to define  $2^N$  different wavelengths. The number of superlattice layers etched in each step controls the wavelength separation. A local schematic of a stepped active region surface is shown in Figure 3.12. In this case, two etch steps are used to define four wavelengths. The first etch step removes two layers (InP + InGaAsP) and the second etch step removes one layer (InP).

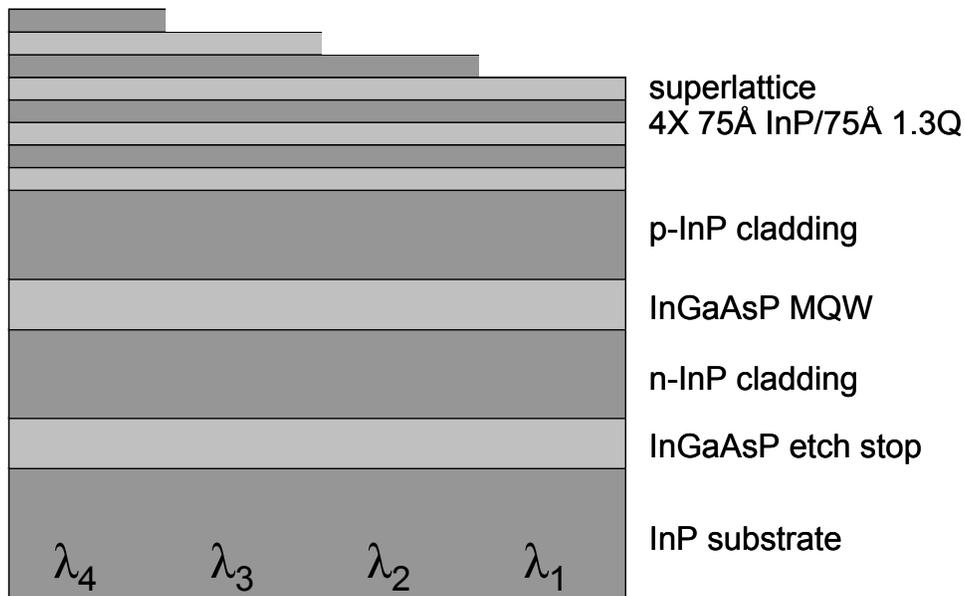


Figure 3.12 Patterned intracavity superlattice for multiple wavelength cavity definition

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The superlattice layers may be removed using selective wet etches. The etch chemistry of the InGaAsP/InP system has been well characterized[37]. InP may be etched in  $\text{H}_3\text{PO}_4:\text{HCl}$ . The etch rate as a function of the  $\text{H}_3\text{PO}_4:\text{HCl}$  ratio is shown in Figure 3.13

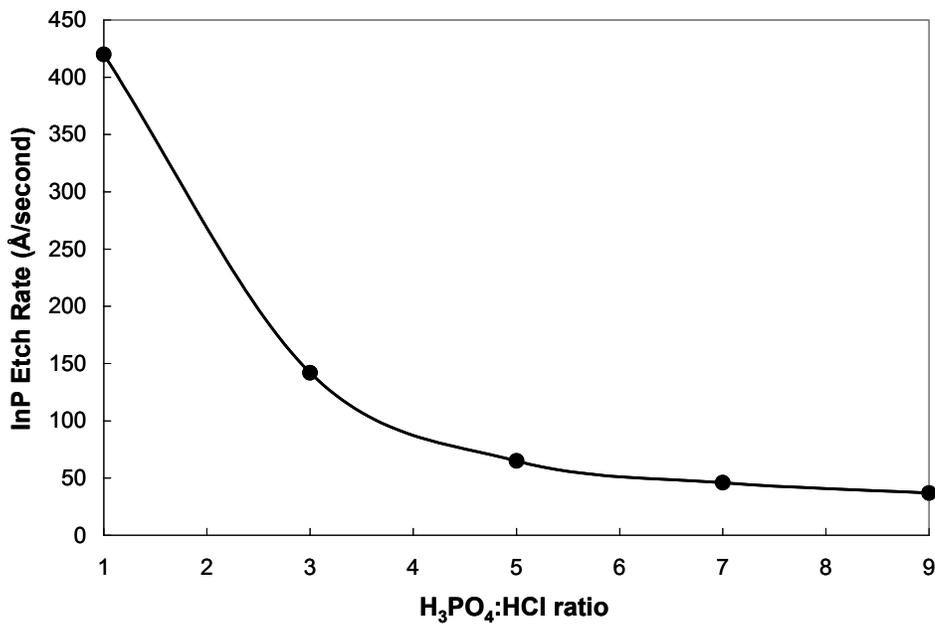


Figure 3.13 Etch rate of InP in  $\text{H}_3\text{PO}_4:\text{HCl}$  solutions

No etch rate was observed for InGaAsP in these solutions for times up to 20 minutes. Low  $\text{H}_3\text{PO}_4:\text{HCl}$  ratio solutions may etch too quickly and punch through the thin InGaAsP layers. High  $\text{H}_3\text{PO}_4:\text{HCl}$  ratio solutions are quite viscous and may not rinse cleanly. For device fabrication, the 75 Å InP layers

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were etched with 5:1  $\text{H}_3\text{PO}_4$ : $\text{HCl}$  solution for 10-20 seconds. The over etch is used to ensure that all traces of InP are removed. The InGaAsP layers may be etched with  $\text{H}_2\text{SO}_4$ : $\text{H}_2\text{O}_2$ :DI. The etch rate of 1.3  $\mu\text{m}$  InGaAsP as a function of  $\text{H}_2\text{SO}_4$  concentration is shown in Figure 3.14. The x-axis indicates the  $\text{H}_2\text{SO}_4$  concentration, X, in an X:1:30 solution of  $\text{H}_2\text{SO}_4$ : $\text{H}_2\text{O}_2$ :DI.

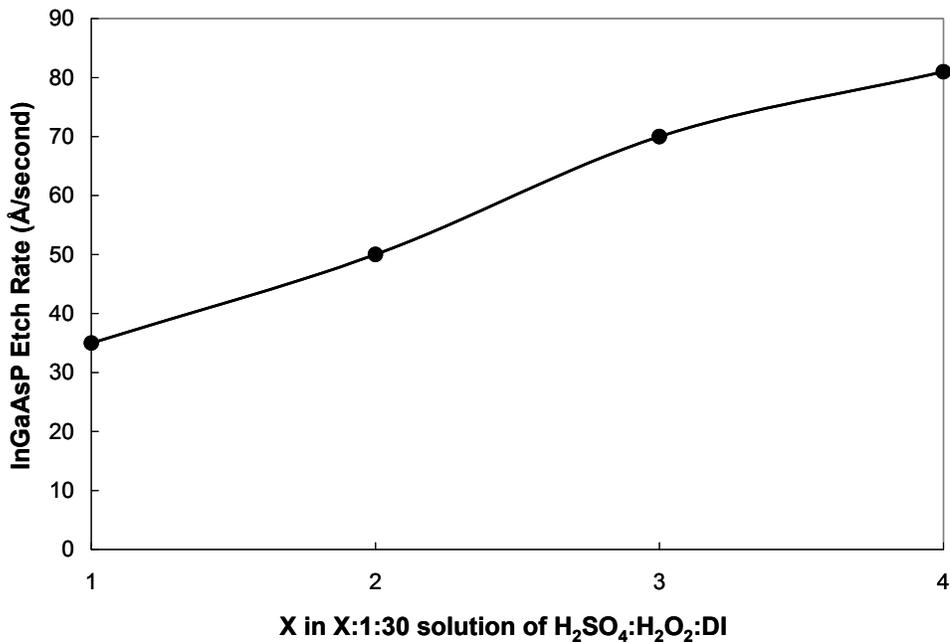


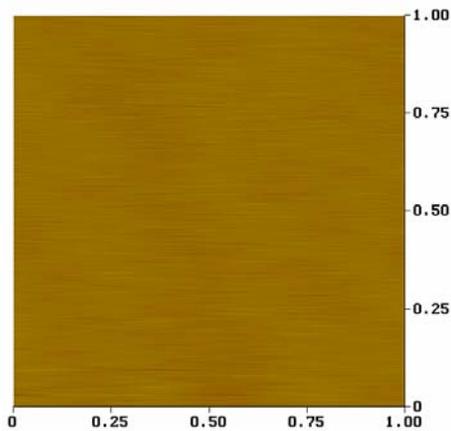
Figure 3.14 Etch rate of InGaAsP in X:1:30 solution of  $\text{H}_2\text{SO}_4$ : $\text{H}_2\text{O}_2$ :DI

An InP etch rate of less than 0.1  $\text{\AA}/\text{second}$  was measured over 20 minutes in a 3:1:30 solution. The InGaAsP etch rate is extremely sensitive to the  $\text{H}_2\text{O}_2$  concentration. A moderate etch rate is desirable in order to avoid etching InP. For

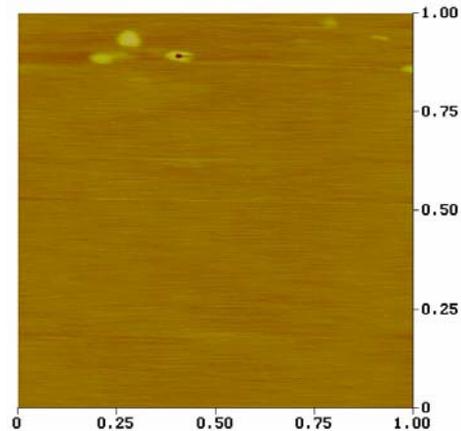
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device fabrication, the 75 Å InGaAsP layers were etched in 2:1:30 H<sub>2</sub>SO<sub>4</sub>:H<sub>2</sub>O<sub>2</sub>:DI for 10-15 seconds.

Atomic force microscopy images of as-grown and etched surfaces are shown in Figures 3.15a-b. Figure 3.15a is an image of the as-grown InP surface and figure 3.15b shows the InP surface exposed after etching one complete period of InP/InGaAsP using the conditions described above. The root mean square roughness values are 0.114 nm for the as-grown sample and 0.126 nm for the etched sample. This is a statistically insignificant change and both surfaces are suitable for wafer bonding. Both the InP and InGaAsP etches produce surface morphology comparable to that of the as-grown epitaxial layers.



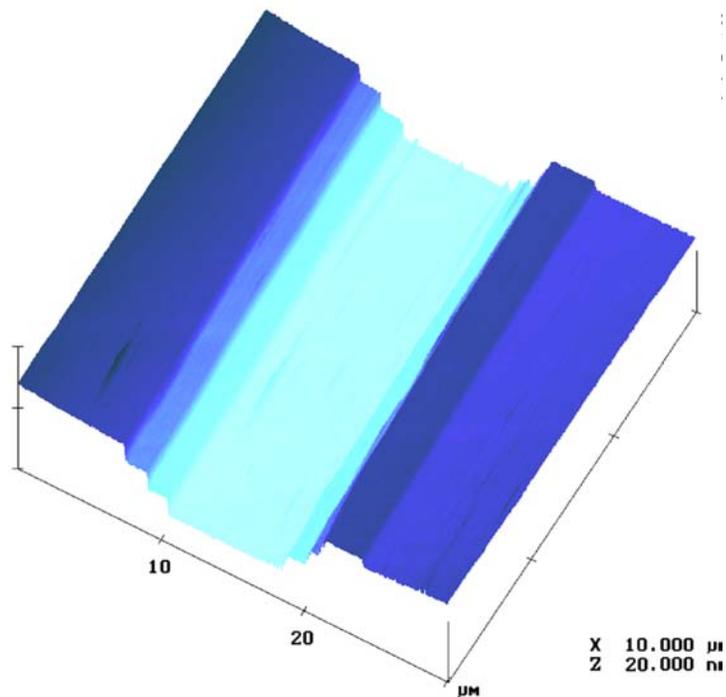
**Figure 3.15a** AFM image of as-grown InP surface



**Figure 3.15b** AFM image of InP surface exposed after superlattice etch

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An AFM image of an etched trough is shown in Figure 3.16. The etch depth is 15 nm, corresponding to one superlattice period. The individual layers were etched after separate lithographic steps. This accounts for the ripple near the trough sidewall. Both the top and bottom surfaces appear smooth and featureless, providing confirmation of the etch depth and quality.



**Figure 3.16** AFM image of 15 nm deep trough etched in superlattice layers

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After surface patterning, the active region is bonded as described in Section 3.2. The etched channel grid is used as an alignment layer for the step height etch. The first bond is to the patterned p-cladding surface. After InP substrate removal, the rest of the bonding process proceeds normally. Although the surface appears to be highly non-planar in the exaggerated schematic of Figure 3.12, the actual bowing of the bonded DBR is quite small. The lateral pitch is chosen as 250  $\mu\text{m}$  to facilitate fiber coupling using standard components. Choosing a step height of 150  $\text{\AA}$  between devices and assuming that any bowing is evenly distributed over the 250  $\mu\text{m}$  distance yields a bowing angle of  $6.0 \times 10^{-5}$  radians. In the worst-case scenario, it is assumed that the entire step height is accounted for over an etched channel of width 10  $\mu\text{m}$ . This assumption yields a bowing angle of  $1.50 \times 10^{-3}$  radians. These angles are quite small and are not expected to alter the expected DBR reflectivity or cavity wavelength.

The expected shift in wavelength for cavities containing different numbers of superlattice periods may be calculated using the one-dimensional transfer matrix method[38]. The difference in refractive index between InP and 1.3  $\mu\text{m}$  InGaAsP at 1550 nm is sufficiently small that the additional reflections introduced are insignificant. The wavelength shift versus number of layers removed is shown in Figure 3.17. The cavity is  $3\lambda/2$  in length, with cladding

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lengths of 309 nm and an MQW region length of 102 nm. The thickness of the p-cladding depends on the number of superlattice periods etched. The layer index on the x-axis begins with InP. The first layer removed is InP, the second layer removed is InGaAsP, the third layer removed is InP and so on.

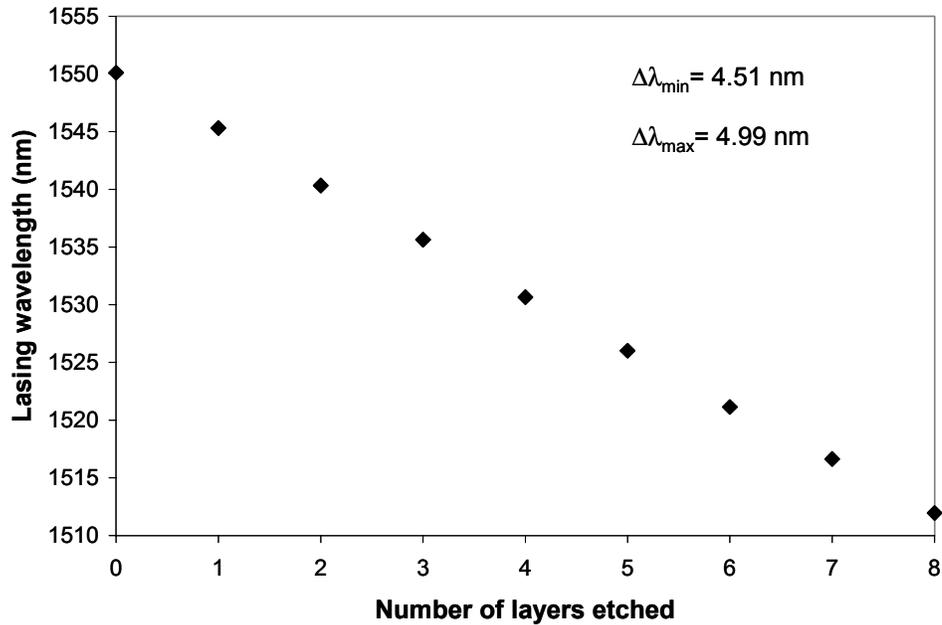


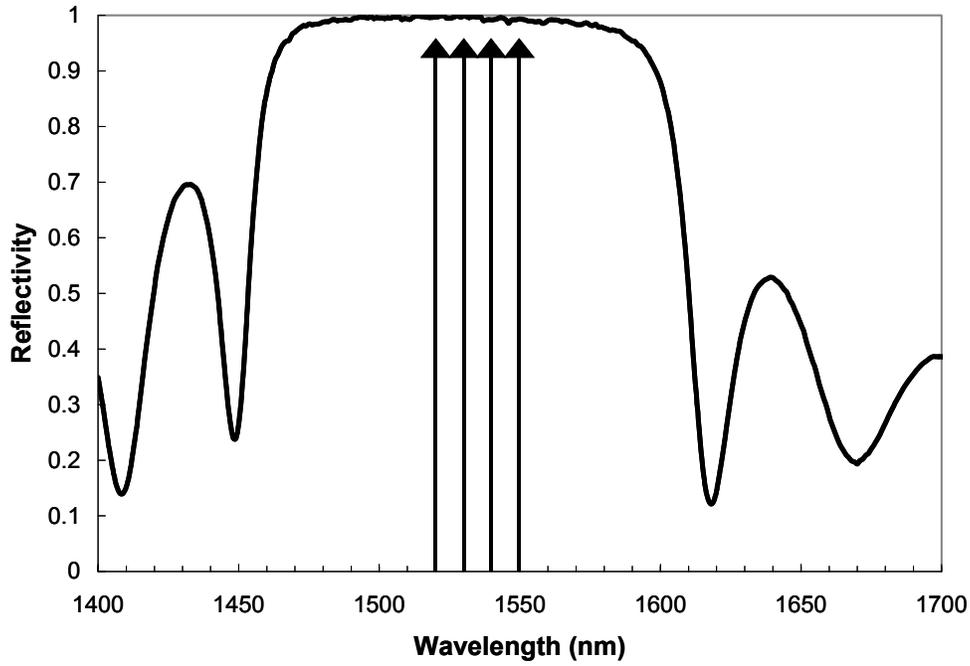
Figure 3.17 Lasing wavelength versus number of tuning layers etched. Odd numbered layers are InP, even numbered layers are InGaAsP.

The wavelength spacing is nearly independent of the layer number being removed. Although there is some slight variation, the wavelength consistency is still suitable for a coarsely spaced WDM scheme. The index difference between InP and InGaAsP is small enough and the cavity is long enough so that the

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changes made to round trip optical path length by each layer are roughly equal. For this cavity length and tuning structure, an additional 5 Å in each InP layer would be required to exactly equalize the wavelength shift caused by etching an individual layer. This is an unreasonable growth tolerance. A finer degree of control may be achieved more practically by using thicker cladding layers. This would permit the use of thicker tuning layers to achieve the same wavelength shift that required thinner layers previously. Growth tolerances on these thicker layers would be sufficient to allow equalization of wavelength spacing for odd and even layer number removals.

In order to support multiple wavelength operation, VCSEL DBRs must have sufficient bandwidth to provide peak reflectivity for all channels. The large bandwidth of GaAs/AlGaAs DBRs at 1.55 μm was discussed in Section 2.3.2. In Figure 3.18, four cavity modes at 1520, 1530, 1540 and 1550 nm are superimposed on the measured reflectivity spectrum of a 25.5 period GaAs/Al<sub>0.9</sub>Ga<sub>0.1</sub>As DBR.



**Figure 3.18** Reflectivity spectrum of 25.5 period GaAs/Al<sub>0.9</sub>Ga<sub>0.1</sub>As DBR. Mode positions at 1520, 1530, 1540 and 1550 nm are indicated by arrows.

All four wavelengths are comfortably within the DBR stop band. This allows each wavelength to utilize the DBR at near-peak reflectivity with minimal phase contribution. Although the DBR bandwidth is approximately 150 nm, the usable portion of the bandwidth is limited by thermal wavelength drift of 0.1 nm/°C. As lasing wavelengths move toward the edge of the stop band, mirror reflectivity becomes more sensitive to environmental fluctuations. In order to reliably and uniformly operate all wavelengths, it is desirable to limit the wavelength span to 60 nm or less. Active cooling would allow for operation over

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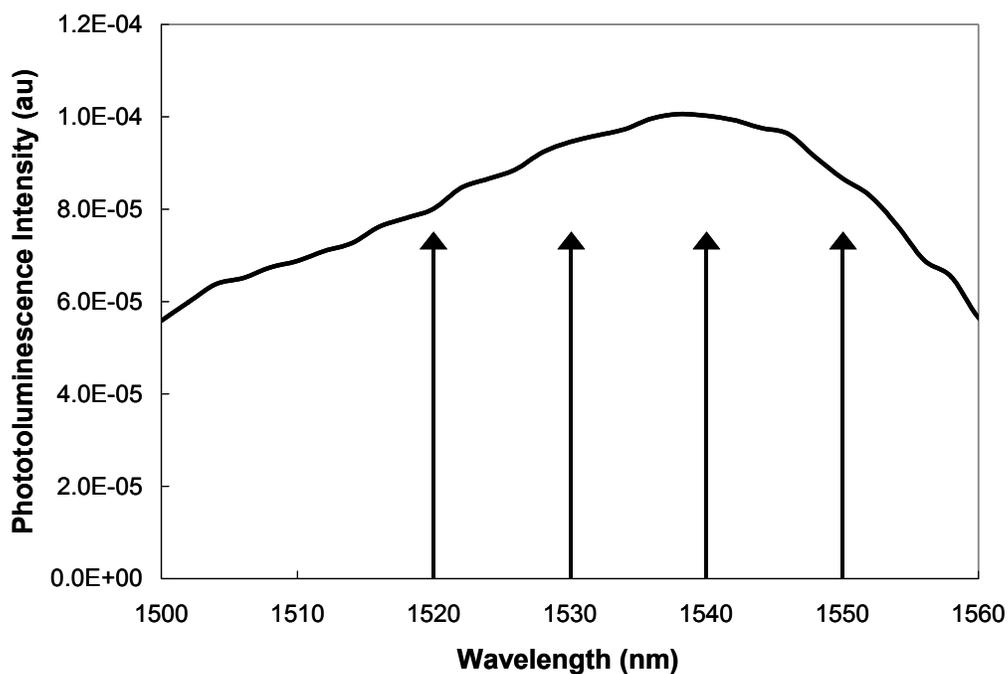
a wider wavelength range. Although all four channels appear to have high reflectivities in the figure above, it should be emphasized that this is only a qualitative examination of DBR reflectivity versus wavelength. A more rigorous evaluation of mode detuning, reflectivity reduction and the corresponding change in threshold current will be presented in Chapter 4.

The material gain of InGaAsP quantum well active regions over the desired wavelength span must also be considered. Similar active regions grown at UCSB have supported tuning spans of more than 70 nm in sampled grating DBR lasers without separate amplification[39]. External cavity InGaAsP multi-quantum well lasers have been used to demonstrate 200 nm tuning[40]. Although these geometries are not identical to the VCSEL structure considered in this work, they are representative of the wide gain bandwidth available in the InGaAsP system. Quantum well lasers are particularly well-suited for operation over a wide wavelength span. Multiple quantized states can provide nearly constant gain over an extended spectral range provided that the current density is sufficiently high[41]. Since elements of the array will lase with different mode-gain offsets, some non-uniformity is expected. However, the broad gain peak of InGaAsP MQW regions is expected to minimize these effects. Figure 3.19 shows the photoluminescence spectra from an active region with six strained quantum wells

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with four cavity modes at 1520, 1530, 1540 and 1550 nm indicated by arrows.

The photoluminescence spectrum is representative of the material gain as a function of wavelength.



**Figure 3.19** Active region photoluminescence intensity. Arrows indicate potential mode positions at 1520, 1530, 1540 and 1550 nm.

It is expected that all channels will see sufficient material gain to lase at room temperature, based on past experience fabricating single-wavelength devices with a wide variety of mode-gain offsets. The cavity wavelength may be changed at will by altering the physical path length. However, VCSEL active regions are typically quite short, on the order of a wavelength. The modal gain

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will be significantly reduced if there is no longer sufficient spatial overlap between the optical field and the quantum well region. A thorough analysis of gain, loss, standing wave effects and mode detuning will be presented in Chapter 4.

The WDM VCSEL array described in this chapter has similar loss levels for each channel, limited by standing wave non-uniformity. Tunable diode lasers typically require the introduction of additional cavity loss to shift the lasing wavelength. This necessitates the use of complicated gain and phase control schemes. Although multiple wavelength VCSEL arrays don't have the same functionality as tunable lasers, reduced fabrication and control costs should make them attractive alternatives for low cost WDM systems.

### **3.8. Electrical Characteristics**

In consideration of the terraced bonding surface, it must be determined if current transport is possible at all four step heights and what degree of uniformity is attainable. A key element in successful bonding of the patterned active region is determining the proper pressure to apply. If the applied force was too high, the wafers were adversely impacted, including cracking or degradation of quantum

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well luminescence. If the applied force was too low, device yield was limited by microscopic and macroscopic voids, even more so than during a planar bonding process. It was found that applied pressures of 2-3 MPa were appropriate for bonding patterned active regions. These pressures are 25-50% higher than those used to join unpatterned surfaces at UCSB. In order to evaluate the diode turn-on voltage and series resistance, a patterned active region was bonded to a p-GaAs epitaxial layer on a p-GaAs substrate, as shown in Figure 3.20.

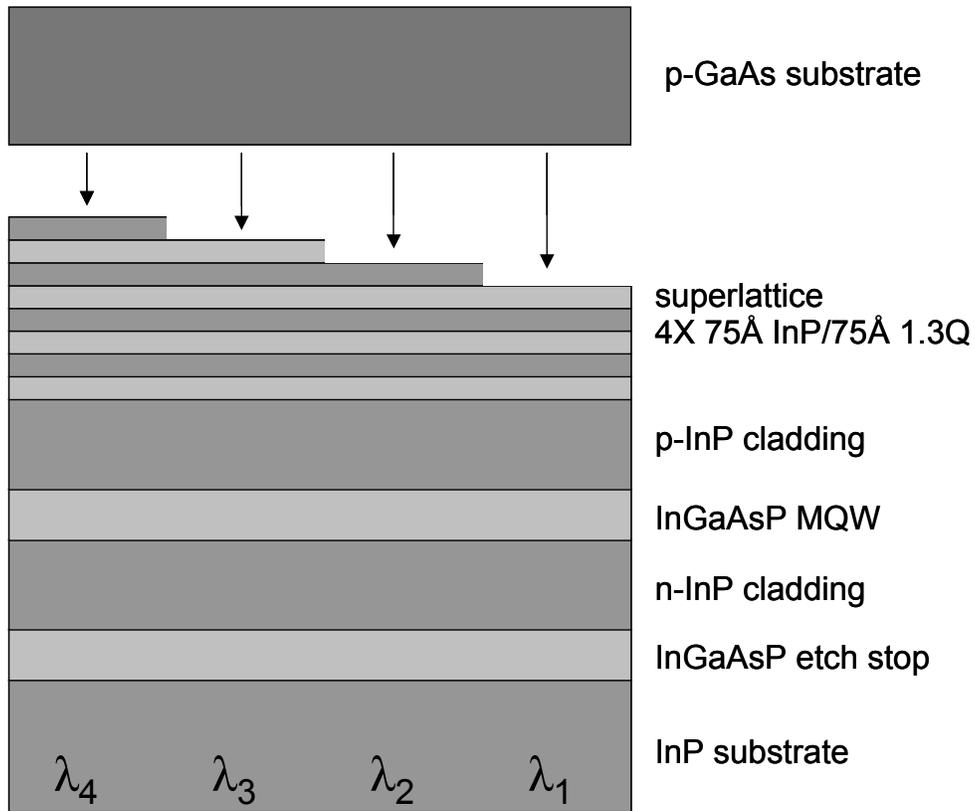


Figure 3.20 Bonding of p-i-n diode structure to determine electrical characteristics of multiple wavelength structures

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The electrical characteristics of the multiple wavelength structure were studied for step heights of one and two layers between adjacent elements, corresponding to  $\Delta\lambda \approx 5$  nm and  $\Delta\lambda \approx 10$  nm. After bonding, the InP substrate and InGaAsP etch stop were removed. Mesa structures were etched through the InP-based epitaxial material and into the GaAs substrate. The pillar diameters were 30-50  $\mu\text{m}$ , similar to the actual VCSEL structure. Contacts were deposited on top of the pillar (n-contact) and on the substrate backside (p-contact). The diode characteristics for four adjacent devices with a 150  $\text{\AA}$  step ( $\Delta\lambda \approx 10$  nm) are shown in Figure 3.21.

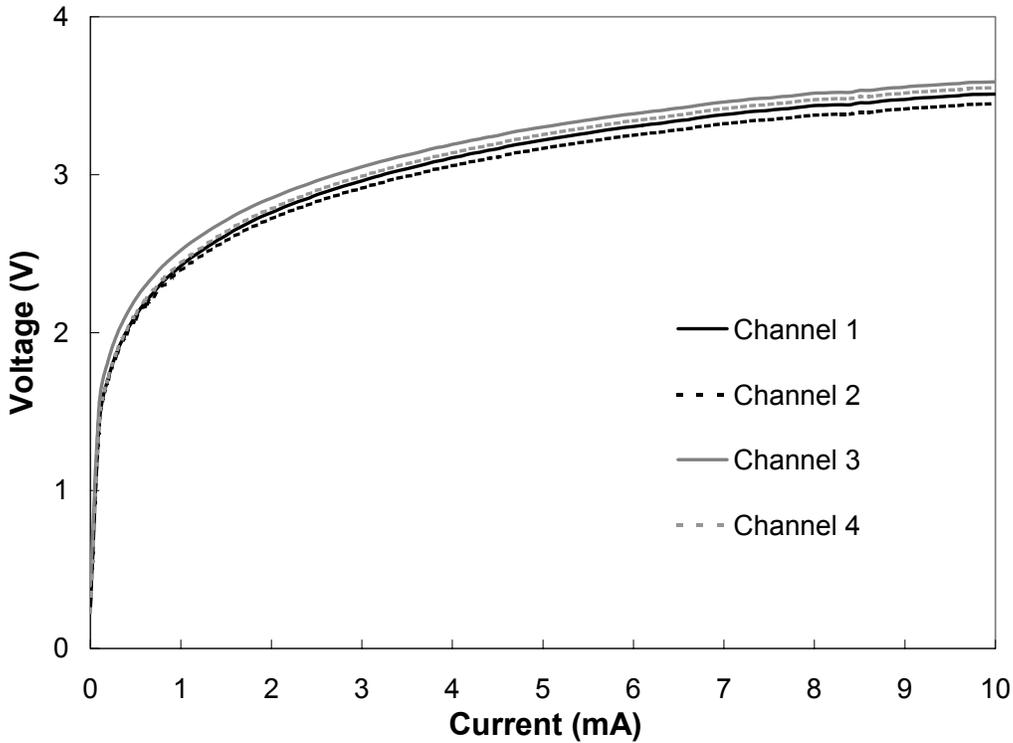


Figure 3.21 Electrical characteristics of bonded diodes with step height of 150  $\text{\AA}$

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The electrical characteristics are consistent with those expected from single wavelength p-i-n diodes with a p-GaAs:p-InP bonded junction. Channel 1 is the shortest device and channel 4 is the longest device. There is no systematic difference between diode turn-on voltage or resistance and channel number for any of the multiple arrays tested. The bonding quality, as indicated by the turn-on voltage, is similar across the array. The series resistance is also near constant. At 3 V, the current density is  $4 \text{ kA/cm}^2$ , more than sufficient for lasing. Although each device sees a different number of electrically resistive superlattice periods, this is only a small part of the total resistance in the structure. Significantly, these results indicate that uniform electrical transport is possible across a patterned junction with a step height of  $150 \text{ \AA}$ . Similar results were obtained for diodes with a  $75 \text{ \AA}$  step height.

### **3.9. Summary**

In this chapter, the process of wafer bonding was described. Structural, optical and electrical properties of the bonded junction were summarized. The use of a novel superlattice defect-blocking layer was found to preserve and even enhance the luminescence of InGaAsP quantum wells in bonded InP active regions. A patterned InP/InGaAsP superlattice was proposed as an intracavity

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tuning layer in a double bonded VCSEL. The electrical characteristics of these patterned and bonded active regions are suitable for continuous-wave lasing. Further analysis of single and multiple wavelength VCSEL cavities will be presented in Chapter 4.

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## 4. Device Design and Fabrication

### 4.1. Introduction

In this chapter, the design and fabrication processes for wafer bonded 1.55  $\mu\text{m}$  VCSELs are outlined. Mirror reflectivities and the number of quantum wells in the gain region are chosen to satisfy requirements for low threshold current and reasonable output power. Round trip gain and loss are considered, including standing wave effects. The impact of mode detuning is used to determine growth tolerances for individual lasers and the tuning range for multiple wavelength devices. Optical and electrical confinement schemes are discussed. A half-intracavity design is used in order to provide uniform carrier injection while reducing optical loss. The lithographic, etch and deposition procedures used to fabricate the device are described.

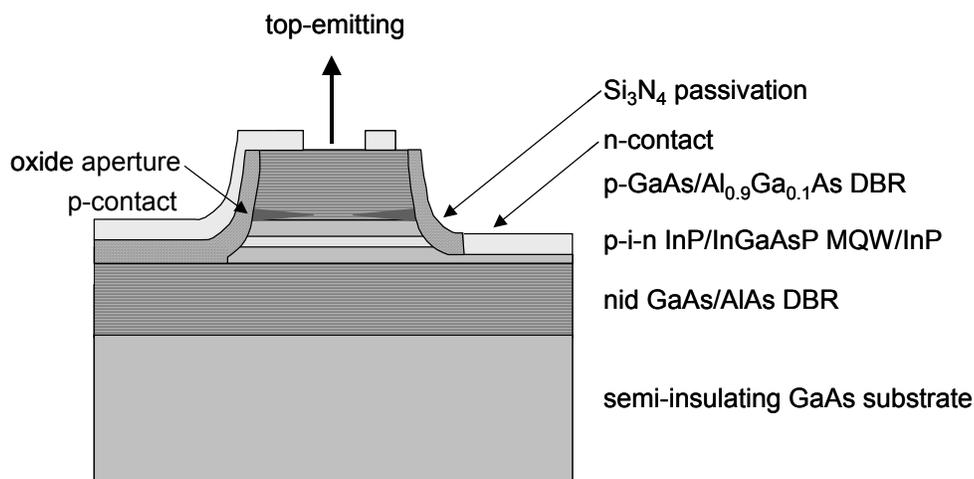


Figure 4.1 Wafer-bonded VCSEL structure

## **4.2. Gain Enhancement Factor**

One of the most striking differences between edge-emitting lasers and VCSELs is the disparity in cavity length. A typical edge-emitting laser is hundreds of microns long. A VCSEL cavity may be on the order of a micron in length, with the gain region occupying a fraction of that distance. Although the gain length is short in a VCSEL, three major effects combine to make the actual threshold material gain levels for edge-emitting lasers and VCSELs comparable. These are:

- Increased lateral confinement of the optical mode
- High reflectivity
- Standing wave gain enhancement

The increased lateral confinement is due to the unique VCSEL geometry. The optical mode overlaps the gain region over a large portion of the waveguide, rather than just a small fraction as in an edge-emitting laser. The typical mirror reflectivities for a VCSEL are greater than 99%. The non-transmissive DBR usually has a reflectivity in excess of 99.9%, while the reflectivity of the transmissive DBR is chosen to strike a balance between low threshold current and high output power. The active regions used in this work were  $3\lambda/2$  in length. This

cavity length was chosen to place the active region at a suitable distance from the bonded junction and at the central standing wave peak. Since the emitted light is coherent on this length scale, standing wave effects must be considered. In order to calculate the gain or loss from a thin section, the mean value of the electric field intensity must be calculated by integrating the field over the layer and dividing by the length of the section. The standing wave effects in the active region are accounted for by the *gain enhancement factor*,  $\xi_{enh}$ [1]

$$\xi_{enh} = \frac{2}{L} \int_{x_0 - L/2}^{x_0 + L/2} \cos^2\left(\frac{2\pi n_{eff} x}{\lambda}\right) dx \quad \text{Equation 4.1}$$

where L is the length of the section,  $x_0$  is the distance between the standing wave peak and the center of the active region,  $n_{eff}$  is the effective refractive index and  $\lambda$  is the free space wavelength. The analytic solution to this integral is given by

$$\xi_{enh} = 1 + \frac{\lambda}{4\pi n_{eff} L} \left( \sin\left(\frac{2\pi n_{eff}}{\lambda} (L + 2x_0)\right) + \sin\left(\frac{2\pi n_{eff}}{\lambda} (L - 2x_0)\right) \right) \quad \text{Equation 4.2}$$

Altering the cladding thickness on one side of the active region will shift the location of the standing wave peak in the VCSEL cavity. Equation 4.2 may be used to calculate the change in gain enhancement factor that results from shifting the standing wave peak from the center of the active region. The standing wave

peak could be kept in the center of the active region by patterning superlattices on both sides of the active region. However, proper design eliminates the need for this extra processing. The gain enhancement factor can be as high as 2 for very short gain regions and quickly converges to a value of 1 for lengths much longer than a wavelength. In Figure 4.2, the gain enhancement factor is plotted versus gain region thickness for a centered standing wave ( $x_0 = 0$ ),  $\lambda = 1550$  nm and  $n_{\text{eff}} = 3.3$ .

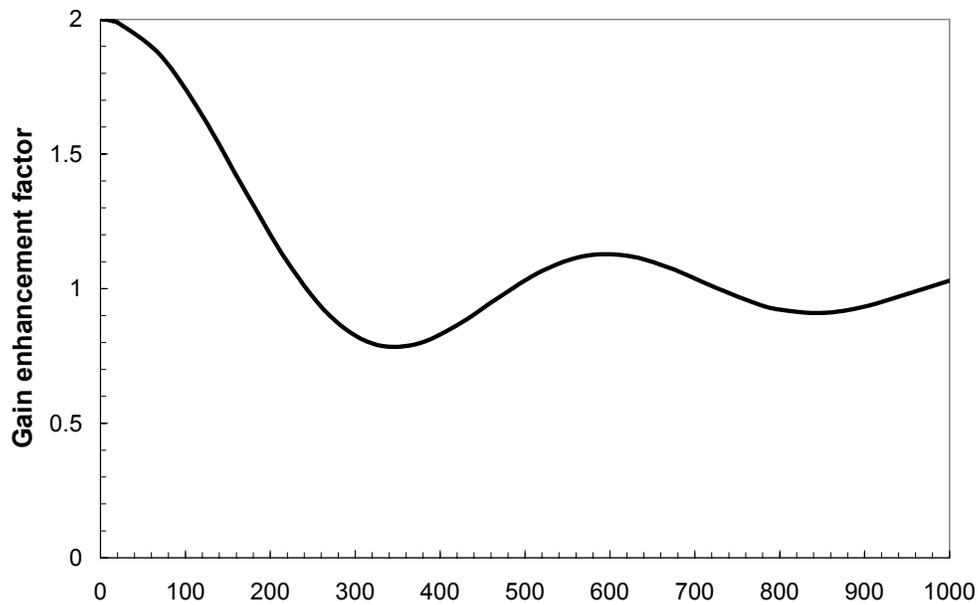


Figure 4.2 Plot of gain enhancement factor versus gain region layer thickness

The standing wave effect in a short cavity permits the gain region to be positioned in such a way as to increase the effective gain by a factor of 2. In

practice, this value is less than 2 due to the finite thickness of the gain region. The gain regions used in this work were 102 nm in length. This corresponds to  $\xi_{enh} = 1.7$  for the conditions described above. Removing superlattice tuning layers will change the value of  $x_0$  for devices with different wavelengths. It must be determined if this affects the gain enhancement factor. If this factor is altered appreciably between devices, there will be significant performance variation within the array.

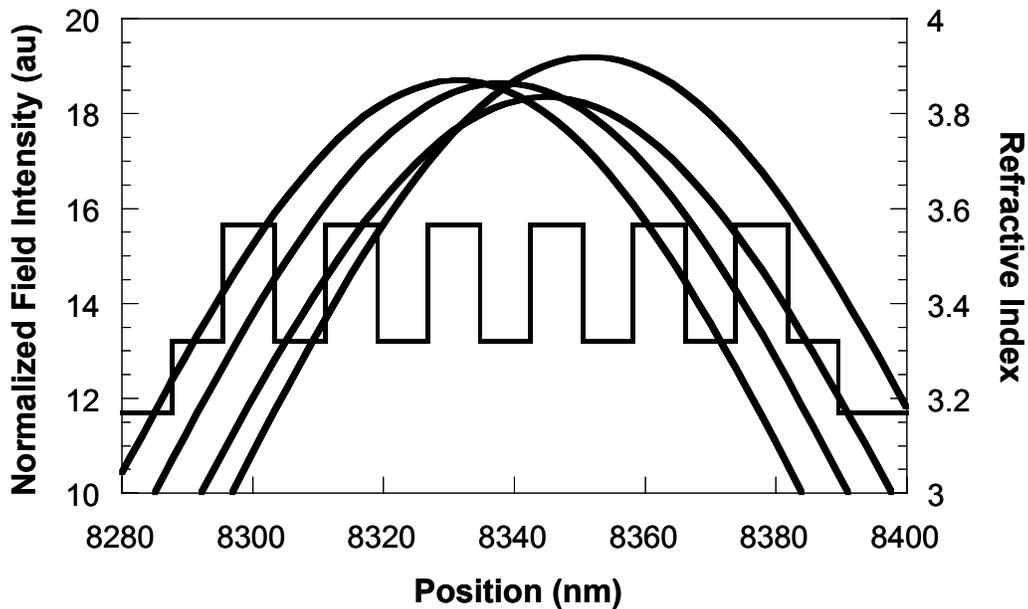
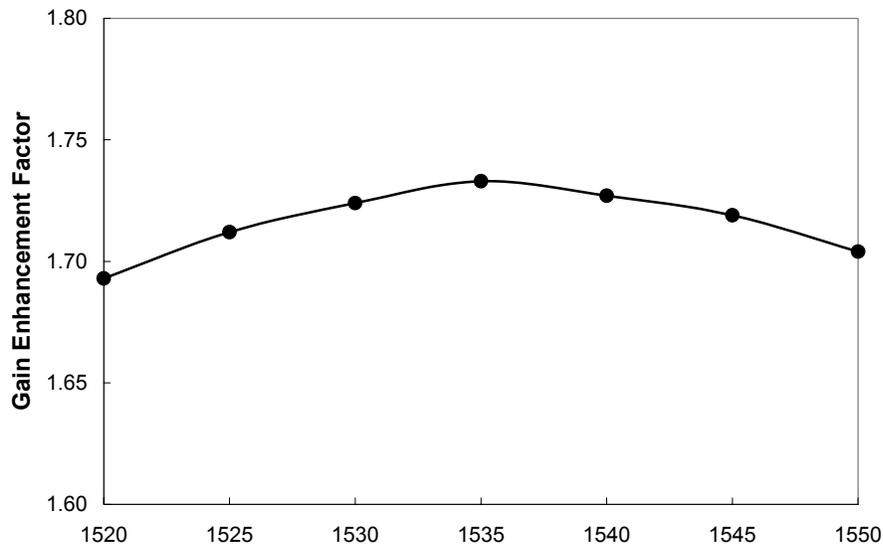


Figure 4.3 Central standing wave peaks for 1520, 1530, 1540 and 1550 nm cavity modes in  $3\lambda/2$  active region with 6 quantum wells. Active region index profile is plotted to indicate spatial overlap with quantum wells. Shortest wavelength peak (1520 nm) is furthest toward the left. Longest wavelength peak (1550 nm) is furthest toward the right.

In Figure 4.3, the central standing wave peaks for 1520, 1530, 1540 and 1550 nm cavity modes in a  $3\lambda/2$  active region are plotted along with the refractive index profile. The active region has 6 quantum wells, centered for a 1535 nm cavity mode. By choosing the cladding layer thickness properly, the standing wave peaks for all wavelengths may be well-aligned with the gain region. This is illustrated graphically in Figure 4.3, where the spatial overlap is similar for all four wavelengths under consideration. In Figure 4.4, the gain enhancement factor is plotted versus wavelength using the same parameters as above. This factor now depends on active region thickness and  $x_0$ , which is different for each wavelength.



**Figure 4.4** Gain enhancement factor versus wavelength in  $3\lambda/2$  active region designed for maximum overlap at 1535 nm

For a well-designed cavity, the gain enhancement factor varies by less than 3%. The uncertainty in material gain and internal quantum efficiency are both greater than 3%. This indicates that standing wave effects are not significant contributors to device non-uniformity. Variation in the gain enhancement factor could be reduced further by using a longer cavity or by tuning both cladding layers as mentioned previously.

### 4.3. Threshold Current

An appropriate set of design curves would show the current needed to reach threshold and the desired peak output power over a range of VCSEL parameters. A simple set of expressions may be used to generate these curves and determine the right number of quantum wells and the proper reflectivity for the output DBR. Although this model is only one-dimensional and neglects device self-heating, it still provides useful design information. The expressions used are adapted from well-known relationships between gain, loss, reflectivity, current density and output power[1]. The threshold material gain,  $g_{th}$ , is given by the expression

$$\Gamma \xi g_{th} (N_w d_w + N_b d_b) = \alpha_i L_{eff} + \ln\left(\frac{1}{R}\right) \quad \text{Equation 4.3}$$

where  $\Gamma$  is the optical confinement factor,  $\xi$  is the gain enhancement factor,  $N_w$  is the number of quantum wells,  $d_w$  is the well thickness,  $N_b$  is the number of barriers,  $d_b$  is the barrier thickness,  $\alpha_i$  is the internal cavity loss (assumed to be equally distributed),  $L_{\text{eff}}$  is the effective cavity length considering field penetration depth into the mirrors, and  $R$  is the mean power reflectivity of the two DBRs. This expression for modal gain includes gain enhancement, modal confinement, internal loss and mirror loss.  $L_{\text{eff}}$  and  $R$  are given by

$$L_{\text{eff}} = (N_w d_w + N_b d_b) + L_c + \frac{\lambda_0}{4\Delta n_t} + \frac{\lambda_0}{4\Delta n_b} \quad \text{Equation 4.4}$$

$$R = \sqrt{R_t R_b} \quad \text{Equation 4.5}$$

The first term in  $L_{\text{eff}}$  is the active region length. The cladding length,  $L_c$ , is chosen for each active region length so that the lasing wavelength is 1550 nm.  $\lambda_0$  is the free space wavelength,  $\Delta n_t$  is the index difference in the top mirror,  $\Delta n_b$  is the index difference in the bottom mirror,  $R_t$  is the reflectivity of the top mirror and  $R_b$  is the reflectivity of the bottom mirror. This approximation for DBR penetration depth is valid in the case of strongly reflective gratings. The material gain is related to radiative current density by the following expression:

$$g(J) = g_0 \ln\left(\frac{J}{N_w J_{tr}}\right) \quad \text{Equation 4.6}$$

where  $g$  is the material gain as a function of current density,  $g_0$  is a gain parameter,  $J$  is the current density and  $J_{tr}$  is the transparency current density for each well. Values for  $g_0$  and  $J_{tr}$  may be obtained through calculation or comparison with actual data. This expression may be used to obtain the threshold current density once the threshold material gain is known. The threshold current is simply given by the product of the threshold current density and the active area. Assuming that all light is exiting through one mirror, the differential efficiency,  $\eta_D$  is given by

$$\eta_D = \eta_i \frac{\ln\left(\frac{1}{R}\right)}{\alpha_i L_{eff} + \ln\left(\frac{1}{R}\right)} \quad \text{Equation 4.7}$$

where  $\eta_i$  is the internal quantum efficiency. The radiative current required to reach a particular output power,  $P$ , can be expressed as

$$I_p = I_{th} + \frac{q\lambda_0}{hc} \frac{P}{\eta_D} \quad \text{Equation 4.8}$$

where  $I_{th}$  is the threshold current density,  $q$  is the fundamental electronic charge,  $h$  is Planck's constant and  $c$  is the speed of light in vacuum. These expressions may be combined to indicate the current and mirror reflectivity required to reach a particular output power for a given number of quantum wells. Fixed design parameters are given in Table 4.1. These values were obtained through measurements on previously fabricated VCSELs, measurements on edge-emitting lasers, simulation and the occasional educated guess. The average internal loss was taken as  $42 \text{ cm}^{-1}$  ( $\approx 1\%$  round trip loss), based on prior analysis and simulation of likely designs. Although this is higher than anticipated loss level, it provides a margin for high temperature operation or lower than expected material quality. The device area was fixed at  $100 \text{ }\mu\text{m}^2$ .

Parameter	Description	Value
L	Round trip loss ( $\approx \alpha_i L_{eff}$ )	0.01
$g_0$	Material gain parameter	$836 \text{ cm}^{-1}$
$J_{tr}$	Transparency current density	$92 \text{ A/cm}^2$
$\eta_i$	Internal quantum efficiency	0.7
$R_b$	Bottom mirror reflectivity	99.99%
A	Area (active region)	$100 \text{ }\mu\text{m}^2$

**Table 4.1 Parameters used to plot design curves in Figure 4.5**

Two sets of design curves were created. Figure 4.5 shows the threshold current versus top (output) mirror reflectivity for 2-7 quantum wells. Figure 4.5 shows the current required for 1 mW output for 2-7 quantum wells.

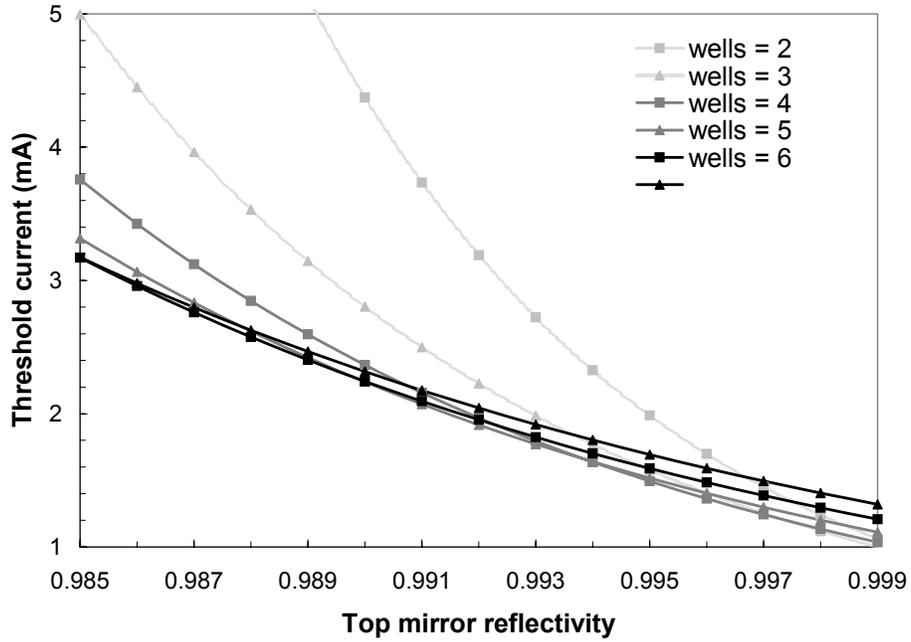


Figure 4.5 Threshold current versus top mirror reflectivity for  $N_w = 2-7$

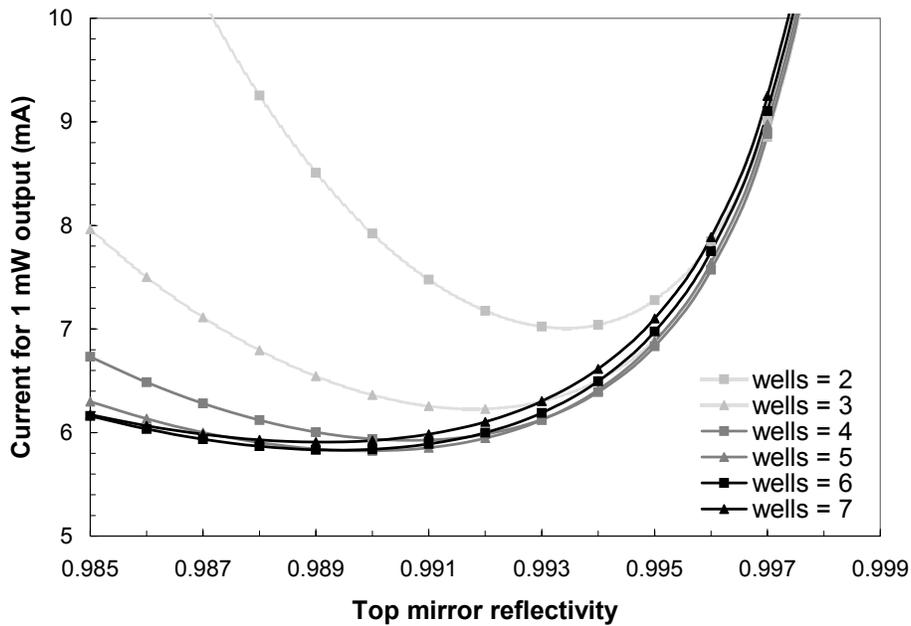


Figure 4.6 Current for 1 mW output versus top mirror reflectivity for  $N_w = 2-7$

As mentioned earlier, this simple model neglects device self-heating, which reduces the gain for a particular injection level. Increased gain is also desirable to support lasing at elevated ambient temperatures. Current spreading, which increases threshold current from the ideal one-dimensional value, has also been neglected. These effects can be mitigated somewhat by using higher mirror reflectivities at the expense of output power. Increasing the number of quantum wells can compensate for poor material quality or spatial misalignment of the gain region. The devices fabricated in this work contained either 5 or 6 quantum wells with top mirror reflectivities of 99.3-99.5%. A p-DBR design matching this reflectivity specification was presented in Section 2.5. It will also be seen that operating with higher reflectivities supports lasing over a wider wavelength span, which is a critical issue for multiple wavelength arrays.

#### **4.4. Mode Detuning**

The position of the cavity resonance is rarely in perfect alignment with the peak DBR reflectivity. Although the DBR reflectivity is quite high over a wide range, cavity modes at different points in the stop band will encounter different reflectivities and have different threshold currents. This has important implications for single wavelength, multiple wavelength and tunable devices.

Variations in epitaxial layer thickness will inevitably detune the cavity mode to some degree for an individual device. The reflectivity bandwidth for multiple wavelength and tunable devices must be sufficiently uniform to permit operation over the desired wavelength span without large increases in threshold current. An appropriate figure of merit might be the maximum wavelength span over which the threshold current varies by less than 20%.

The first step is to establish the change in reflectivity that results in a threshold variation of 20%. Using the equations above and the design curve for a six quantum well device with a mean power reflectivity of .9960, it is determined that a reduction of the mean power reflectivity to .9934 would cause a 20% increase in threshold current. In a double bonded VCSEL, it is likely that the cavity wavelength is detuned from the peak reflectivity wavelengths of both DBRs. However, the threshold current is more sensitive to a reflectivity reduction in the output mirror. It is assumed that the reflectivity variation is contained entirely within the transmissive DBR. This reduction in overall reflectivity corresponds to a reduction in output mirror reflectivity from 99.30% to 98.78%, assuming a 99.95% reflective bottom DBR. Using the equations presented in Chapter 2, it is found that this includes the wavelength span of 1507-1593 nm for a DBR centered at 1550 nm. This 86 nm bandwidth is more than enough to

support multiple wavelength operation over the EDFA gain bandwidth (1530-1560 nm). The fractional bandwidth of 5.54% suggests that DBR layer thickness may vary by  $\pm 5.54\%$  before the threshold current changes by 20%.

The relationship of the cavity mode to the reflectivity spectrum is only part of the story. The material gain also varies with wavelength. Although there are no simple analytic formulas for the gain spectrum of a quantum well active region, a polynomial curve fit may be used to approximate gain as a function of wavelength over the interval of interest. The peak material gain as a function of current density is written using the standard logarithmic form:

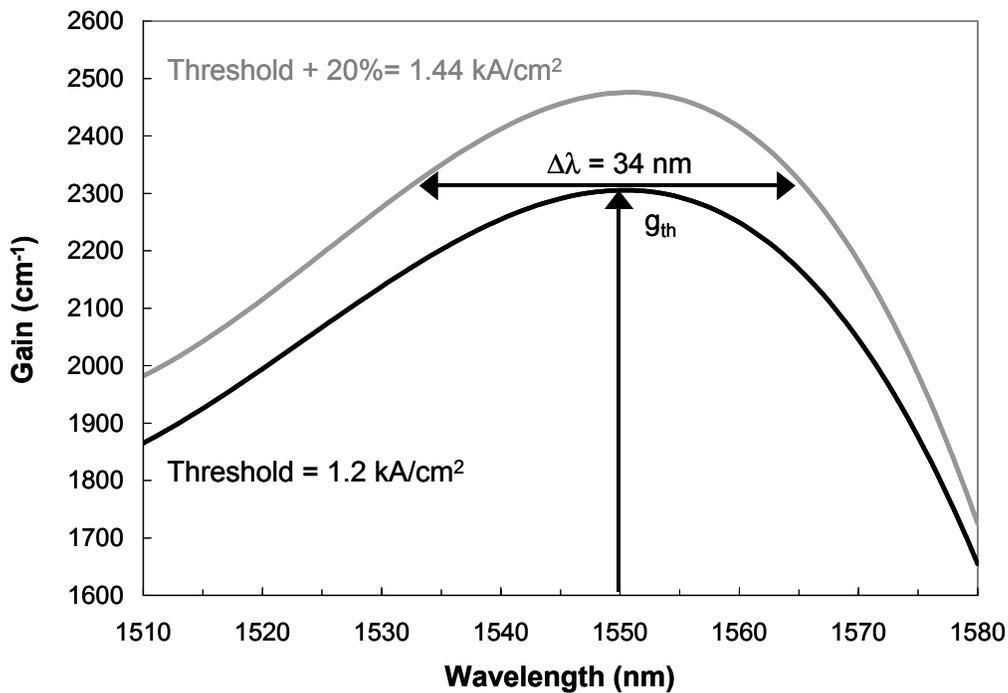
$$g(J) = g_0 \ln\left(\frac{J}{J_{tr}}\right) \quad \text{Equation 4.9}$$

where  $J$  is the current density and  $J_{tr}$  is the total transparency current density.

Consider an active region pumped with two different current densities, 1.2 kA/cm<sup>2</sup> and 1.44 kA/cm<sup>2</sup>, 20% higher. Using Equation 4.9 and previous numerical modeling of quantum well gain spectra[2, 3], the following curve fits are derived for the two injection levels:

$$\begin{aligned} 1.2 \text{ kA/cm}^2 : g(J, \lambda) &= g(J) + 2.993(\lambda - 1550) - 0.595(\lambda - 1550)^2 - .00673(\lambda - 1550)^3 \\ 1.44 \text{ kA/cm}^2 : g(J, \lambda) &= g(J) - 8.861(\lambda - 1550) - 0.792(\lambda - 1550)^2 - .00834(\lambda - 1550)^3 \end{aligned}$$

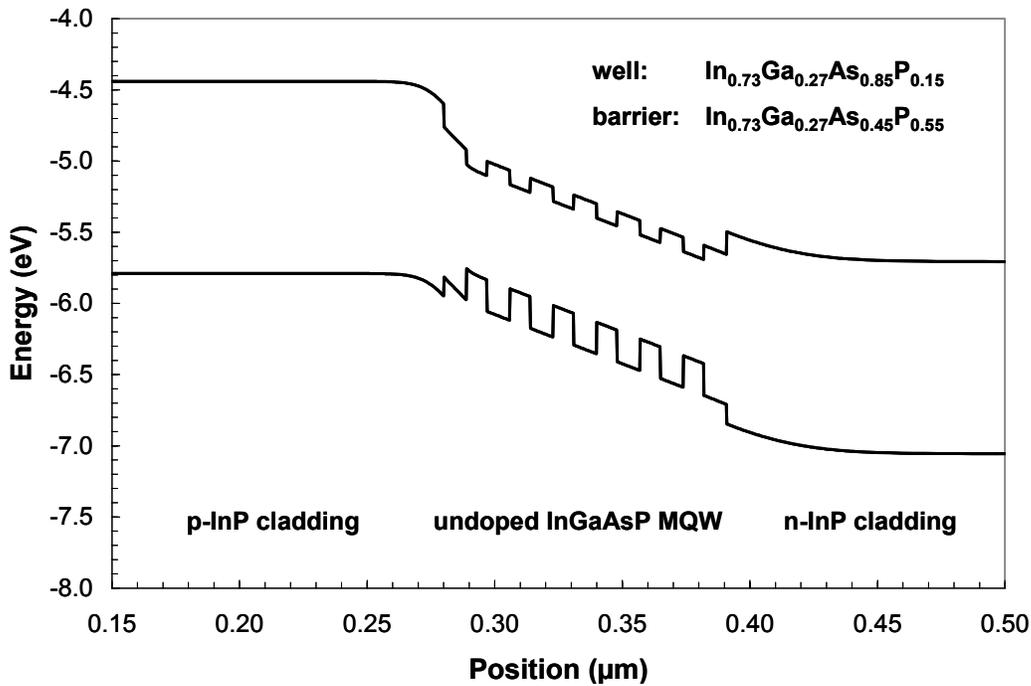
where  $g$  is in  $\text{cm}^{-1}$  and  $\lambda$  is in nm. The added polynomial is centered around 1550 nm, which is taken as the peak gain wavelength. Although not exact, these curves are representative of the gain variation with wavelength at the two injection levels. Using  $g_0 = 836 \text{ cm}^{-1}$  and  $J_{\text{tr}} = 92 \text{ A/cm}^2$  as in the previous section, the gain bandwidth that defines a 20% variation in threshold current may be extracted from the curves in Figure 4.7.



The two curves show gain as a function of wavelength for current densities of 1.2 kA/cm<sup>2</sup> (assumed to be threshold) and 1.44 kA/cm<sup>2</sup> (threshold + 20%). It is assumed that the cavity mode is aligned with the gain peak at 1550 nm, as indicated by the vertical arrow. The threshold gain value of 2300 cm<sup>-1</sup> at 1.2 kA/cm<sup>2</sup> for a 1550 nm cavity mode may be achieved over the range of 1532-1566 nm at 1.44 kA/cm<sup>2</sup>. This suggests that the wavelength may be varied over a 34 nm span with only a 20% increase in threshold due to the gain profile. Fortuitously, this span coincides nearly perfectly with EDFA gain bandwidth. The VCSEL tuning range is limited by the gain variation with wavelength rather than by DBR reflectivity. A more flat gain profile could be created by using a chirped quantum well active region with each well providing peak gain at a different wavelength. This technique is also of interest for reduced temperature sensitivity[4]. However, a wider gain distribution will result in higher threshold currents. An optimized solution considering the desired cavity mode(s), reflectivity spectrum and gain spectrum may be determined for single or multiple wavelength operation based on the desired output characteristics.

Quantum well active regions for 1.55 μm lasers in the InGaAsP/InP material system have been studied extensively[5, 6]. The adoption of strained quantum wells has reduced transparency current densities while increasing

differential gain. An equilibrium energy band diagram for the active region used in this work is shown below in Figure 4.8. The diagram shows the central portion of the active region, including only the quantum well region and 0.1  $\mu\text{m}$  cladding on either side. A uniform doping level is assumed in the p-cladding for clarity, but a doping grade was used in actual devices and will be discussed in Section 4.6.



A binary cladding is used for improved carrier confinement, increased thermal conductivity and reduced absorption relative to ternary or quaternary claddings. The well depth is approximately 136 meV in the conduction band. At

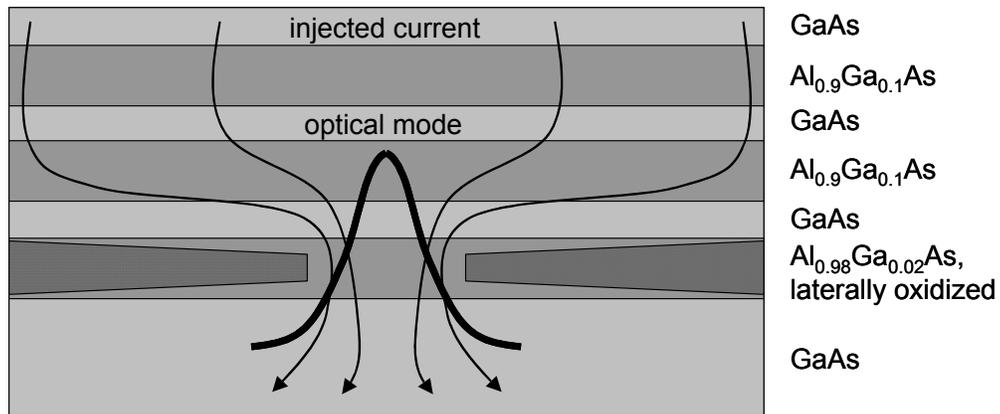
InGaAsP heterojunctions, only 40% of the band offset is accommodated in the conduction band[7]. Electron leakage could be reduced significantly by using an AlInGaAs active region. In this material system, 68% of the band offset takes place in the conduction band. This would dramatically improve carrier confinement, particularly at high temperature. Carrier leakage and thermal effects in fabricated devices will be examined more closely in Chapter 5.

#### **4.5. Confinement**

The discussion to this point has been focused on issues of gain, loss and reflectivity. The precise VCSEL geometry and current injection scheme selected also have a large impact on device performance. An advantage of using GaAs-based DBRs in long wavelength VCSELs is that the robust lateral confinement techniques of short wavelength VCSELs may be applied. The three types of lateral confinement to be considered are mode confinement, current confinement and carrier confinement. Confinement of the optical mode reduces optical losses by guiding photons along the desired axis through a lateral index perturbation. A small degree of current confinement is introduced by injection through a finite contact area. However, increased confinement is desirable for efficient lasing and improved spatial overlap between the mode and the gain. Carrier confinement may be achieved with a lateral bandgap step in the active region. This increase in

bandgap limits carrier diffusion out of the active region. Carrier confinement in VCSELs is generally difficult to achieve without complicated processing that might eliminate the cost advantages associated with the vertical cavity geometry. Advanced techniques for mode and current confinement have been developed for GaAs-based short wavelength VCSELs. The etched pillar and oxide aperture have enabled tremendous performance advances in threshold current and wallplug efficiency[8, 9]. These techniques have been adapted for wafer bonded VCSELs at UCSB by Babic[10] and Margalit[11]. The etched pillar alone confines the current to an area defined by the pillar. However, this design is entirely gain-guided. The optical mode encounters significant loss at the pillar sidewalls without any index guiding for photon confinement. Etching through the active region results in significant non-radiative recombination due to the existence of surface states. The fabrication of small, low-threshold devices is difficult due to this non-radiative recombination mechanism and the high optical loss associated with the optical mode filling the width of the pillar. These effects are reduced dramatically by the introduction of an oxide aperture. After etching through the top DBR and active region, a high aluminum content AlGaAs layer is laterally oxidized at temperatures of 400-500°C using steam. Pure AlAs is difficult to oxidize reproducibly. The oxidation rate is more easily controlled for layers containing small amounts of gallium, e.g.  $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$ . Only one oxide aperture

is desired. The other AlGaAs layers in the DBR have  $x=90\%$  so that the oxidation rate is negligible compared to that of the  $x=98\%$  layer. The insulating aluminum oxide layer forces current inward to the unoxidized AlGaAs region. The lateral index perturbation from the oxide confines the optical mode in the center of the pillar, reducing optical loss at pillar sidewalls and enabling spatial overlap between the mode and gain profile. The aperture is usually placed at or near a null in order to reduce diffraction loss[12]. Thin, tapered apertures may be used to reduce scattering loss[9]. A schematic of an oxidized DBR aperture is shown in Figure 4.9.



**Figure 4.9** Lateral current and mode confinement with oxidized AlGaAs aperture. The bold black line illustrates the confined optical mode. The arrows show current confinement in the center of the pillar.

It should be noted that current aperturing is far more effective for confining hole current than for electron current. The high mobility of electrons limits n-side aperturing, as the electron current will spread again quickly after passing through the aperture. However, hole current may be well-confined over a greater distance due to lower hole mobility. The effects of current spreading beneath the aperture have been studied by other authors[13] and will be examined more closely in Chapter 5.

#### **4.6. Optical Loss**

In the previous section, gain and bandwidth were calculated based on a round trip loss level of 1%, corresponding to an effective loss coefficient of  $42 \text{ cm}^{-1}$  for a  $3\lambda/2$  cavity. The origin of these losses is now presented in further detail. Although light emitted at  $1.55 \mu\text{m}$  is below the bandgap energy for both GaAs and InP, free carrier absorption and intervalence band absorption (IVBA) in doped GaAs and InP are significant loss contributors. The absorptive losses at three different wavelengths are summarized in Table 4.2. The losses are normalized to a  $10^{18} \text{ cm}^{-3}$  doping level. For instance, the absorptive loss in p-GaAs doped at  $2 \times 10^{18} \text{ cm}^{-3}$  is  $58 \text{ cm}^{-1}$ .

Material	0.98 $\mu\text{m}$	1.3 $\mu\text{m}$	1.55 $\mu\text{m}$
p-GaAs	7 $\text{cm}^{-1}$	15 $\text{cm}^{-1}$	29 $\text{cm}^{-1}$
p-InP	-	15 $\text{cm}^{-1}$	15 $\text{cm}^{-1}$
n-GaAs	5 $\text{cm}^{-1}$	6 $\text{cm}^{-1}$	6 $\text{cm}^{-1}$
n-InP	-	5 $\text{cm}^{-1}$	5 $\text{cm}^{-1}$

**Table 4.2** Absorptive loss per  $10^{18} \text{ cm}^{-3}$  doping level for GaAs and InP at 0.98, 1.3 and 1.55  $\mu\text{m}$

Two major trends are apparent. First, the absorption losses in p-type material are greater than in n-type material for the same doping level. Second, the loss exhibits an increase with wavelength due to IVBA. Since long wavelength VCSELs require low optical loss and low electrical resistance, these effects combine to severely limit the range of doping levels that can be used. Fortunately, the impact of these optical losses can be mitigated by placing highly doped layers at nulls in the standing wave pattern. The *effective absorption coefficient*,  $\alpha_{\text{eff}}$ , is defined by the following expression[14]:

$$\alpha_{\text{eff}} = (2 - \xi)\alpha_{\text{material}} \quad \text{Equation 4.10}$$

where  $\alpha_{\text{material}}$  is the material loss coefficient from Table 4.2 and  $\xi$  is the gain enhancement factor defined in Section 4.2. The factor  $(2 - \xi)$  may be thought of as

a *loss reduction factor*. Highly doped DBR sections and the bonded junctions are placed at standing wave nulls in the cavity, where the loss reduction factor is between 0.01 and 0.1. Although the bonded junction is not intrinsically lossy, it is a gettering site for dopants, particularly Zn, that contribute to optical absorption.

Table 4.3 summarizes the calculated optical loss in each section of the wafer bonded VCSEL. Interaction lengths are determined by standing wave effects and effective DBR penetration depths. The absorptive loss in the DBRs was calculated using the 1-D transfer matrix method. For the p-DBR, the doping layer given corresponds to that used in the seven DBR periods closest to the active region. The complete doping profile can be found in Section 2.7. The p-cladding was grown using three different dopant levels to reduce zinc damage and absorption near the quantum well region. An absorption level of  $2 \text{ cm}^{-1}$  is chosen for undoped material. The loss reduction factor is shown as multiplying the interaction length. The absorption loss in the MQW region is based on estimates of carrier density at threshold and will vary based on the injected current.

Region	Material	Doping (cm <sup>-3</sup> )	Interaction length (nm)	Loss (cm <sup>-1</sup> )	Round trip loss (%)
p-DBR	p-GaAs/Al <sub>0.9</sub> Ga <sub>0.1</sub> As	4E17/6E17	897	12	0.21%
p-cladding	p-InP/InGaAsP	2E18	30*0.06	30	0.001%
p-cladding	p-InP	1E18/5E17/nid	260	15/7.5/2	0.04%
MQW	nid-InGaAsP	nid	102*1.72	50	0.18%
n-cladding	n-InP	2E18	310	10	0.06%
nid DBR	nid-GaAs/AlAs	nid	805	2	0.03%
<b>Total</b>					<b>0.52%</b>

**Table 4.3** Calculated losses in VCSEL structure

Standing wave factors are used to calculate the loss contribution from the superlattice cap (close to null) and the MQW active region (at peak). The loss contribution of the superlattice cap is negligible and may be taken as constant for devices with different wavelengths. The p-DBR is the single largest contributor to round trip loss. Reducing the doping levels in the DBR further would reduce absorption, but also increase the electrical resistance of the device. Tunnel junction injection would allow the use of two n-type DBRs. Due to diffusion during growth, this transport scheme is not possible using Zn-doped active regions.

## 4.7. Structure

The desired cavity length, number of quantum wells, mirror reflectivity and confinement scheme have been determined using a combination of simulation, wafer bonding constraints and past work with short wavelength

devices. Current injection through the p-DBR is desirable in order to present a uniform carrier profile and use lateral confinement for fabrication of low threshold devices. Additional structural issues remain, including the choice of whether the VCSEL should be top or bottom-emitting and the n-contact location. The emission direction chosen depends on the type of packaging that will be used. Top-emitting devices may be epoxied to TO headers or a simple chip tray. A bottom-emitting device will need to be flip-chip bonded or mounted upside down on drive circuitry, a more complicated process. Coplanar ground-signal-ground bond bands are desirable for high-speed modulation. A p-bondpad may be deposited on insulating material and connected to a p-contact on top of the DBR using bridge metal. In this geometry, an intracavity n-contact permits coplanar bondpads and allows the use of an undoped bottom DBR, which reduces optical loss. Processing is complicated only slightly by the need to stop the pillar etch on the n-InP cladding. In summary, the major features of the VCSEL under consideration are:

- $3\lambda/2$  cavity
- 6 quantum well active region at standing wave peak
- p-type top GaAs/Al<sub>0.9</sub>Ga<sub>0.1</sub>As DBR with 99.3% reflectivity
- undoped bottom GaAs/AlAs DBR with 99.9% reflectivity
- etched pillar to n-InP cladding
- oxide aperture for mode and current confinement at standing wave null
- superlattice tuning layer near standing wave null
- p-contact on p-DBR

- n-contact on n-InP cladding
- coplanar ground-signal-ground bond pads for high speed modulation

These properties may be combined in a single design. The refractive index profile and standing wave pattern are shown below in the vicinity of an active region with two superlattice periods. This cavity wavelength is in the middle of the tuning range.

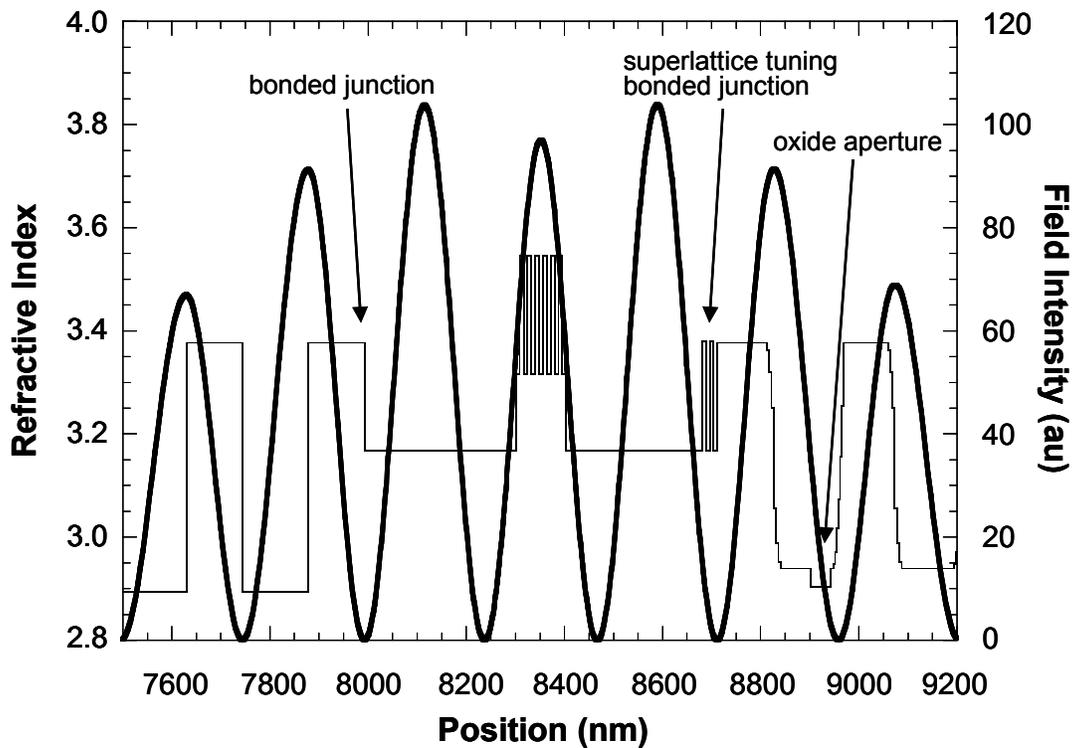


Figure 4.10 Standing wave pattern near VCSEL active region

The quantum wells are located at the central standing wave peak in the  $3\lambda/2$  active region. Bonded junctions are located at the second null. The superlattice tuning layers are located on the InP side of the p-InP:p-GaAs bonded junction and are only slightly displaced from the null. Since the superlattice heterojunctions can be highly resistive, it is desirable to heavily dope these layers. Placing them at or near a standing wave null reduces the associated optical loss. The tapered oxide aperture is located near the third null. This allows an index perturbation while reducing scattering and diffraction loss. The p-DBR heterojunctions are graded as described in Chapter 2.

## **4.8. Fabrication**

In this section, the fabrication process is outlined with a general description of each step.

### *4.8.1. Wafer Bonding*

The bonding process is completed as described in Chapter 3. The sample size is typically 1 cm x 1 cm. Prior to bonding, a grid-like pattern of channels is etched into the surface of the p-cladding. These channels allow the escape of trapped gas and liquid during the bonding process. The channel pitch is 250  $\mu\text{m}$  and the etch depth is 150-200 nm. Although the exact thickness is not critical, the

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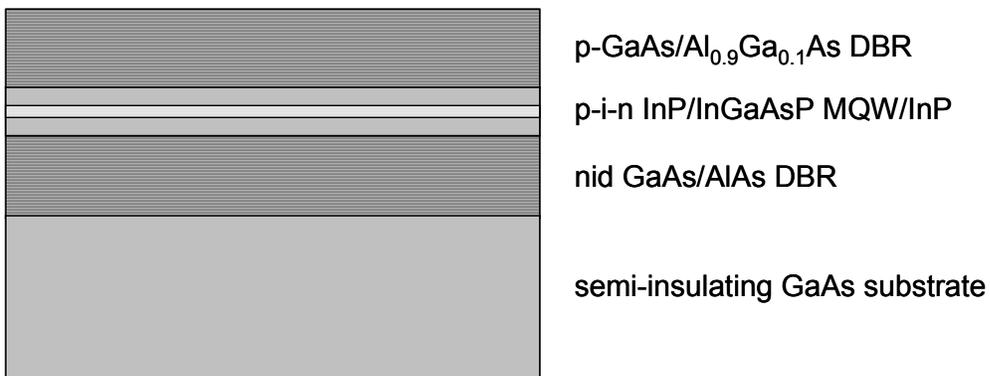
channels should not impinge upon the quantum well region. It is important to make sure that the channels run all the way to the edge of the sample.



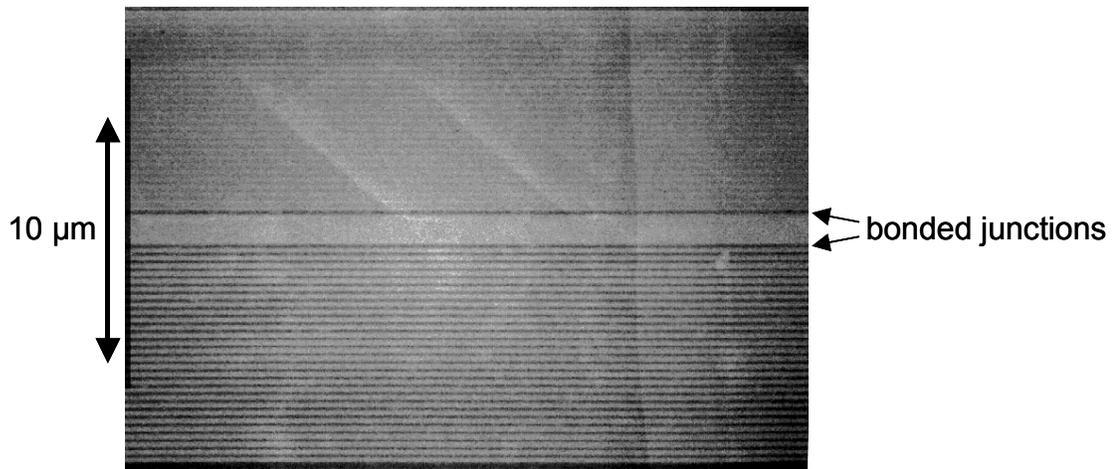
**Fi**  
**depth is 150 nm.**

**1 pitch is 250  $\mu\text{m}$ . Channel**

For WDM arrays, the surface etches described in Chapter 3 are performed prior to bonding to create multiple wavelength cavities. A schematic of the bonded structure is shown in Figure 4.12 and an SEM image in Figure 4.13.



**Figure 4.12 Schematic of double-bonded VCSEL structure on GaAs substrate**



**Figure** **structure**

After the GaAs substrate is etched away, it is critical that the AlGaAs etch stop layer be promptly and completely removed. This layer will oxidize quickly upon exposure. After etch stop removal, the p-GaAs contact layer is exposed. Any residual oxide or AlGaAs will degrade the quality of the p-contact formed in the next step. Remaining surface debris should be carefully removed. Although bonding is rarely achieved at the very edges of the sample, the bonded area typically covers more than 90% of the surface. The surface morphology of the bonded sample is critical. Poor morphology will lead to complications and poor yield in all remaining process steps. Nomarski micrographs at 50x magnification of three surface morphologies are shown in Figures 4.13a-c. The images are of the

exposed p-DBR surface after double bonding and substrate removal. Figure 4.13a shows a good surface with only a small number of point defects. The channel pattern is visible, indicating a slight bowing of the transferred epitaxial material. The surface in Figure 4.13b has a high density of microscopic voids, on the order of 1  $\mu\text{m}$  in diameter. These voids are thought to be caused by trapped gas at the bonded interface and can be prevented by using deeper channels or otherwise forcing out all trapped liquid prior to bonding. The large-scale bubbling and cracking seen in Figure 4.13c are caused by unevenly applied pressure or particulate contamination during bonding. The surfaces in these images were patterned for multiple wavelength definition prior to the first bond.



**Figure 4.13a-c** Nomarski micrographs of exposed surfaces after double bonding process. From left to right: good surface, high microscopic void density, large-scale cracking

After bonding, identical processing steps are used to fabricate single or multiple wavelength devices.

4.8.2. *p*-metallization

The *p*-contact resistance is much greater than the *n*-contact resistance and far more sensitive to surface quality and process fluctuations. For this reason, it is desirable to put the *p*-contact down as soon as possible. After solvent cleaning, image reversal lithography using AZ5214 for liftoff is performed. Since the device will be top-emitting, a ring contact is used. An oxygen plasma descum and acid dips are performed to leave a clean, oxide-free *p*-GaAs surface. The surface morphology must be smooth in order to develop the proper liftoff profile. The *p*-contact metals are evaporated using an electron beam evaporator. Ti/Pt/Au (50/400/2000 Å) was used as the *p*-contact metallization. Titanium improves the sticking quality and platinum acts as a barrier to gold diffusion during the high temperature oxidation process. An illustration of the metallized surface is shown in Figure 4.14.

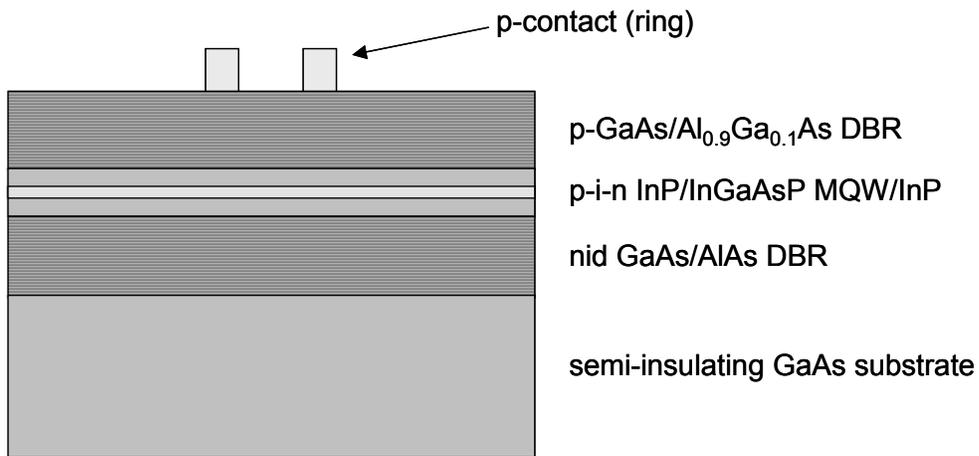


Figure 4.14 Bonded VCSEL structure with *p*-metal (Ti/Pt/Au) ring contact

### 4.8.3. Pillar etch

After liftoff is complete, a 1000 Å  $\text{Si}_3\text{N}_4$  (silicon nitride) layer is deposited using plasma enhanced chemical vapor deposition (PECVD). This layer will serve as part of an etch mask for the device pillar. A 3 μm layer of photoresist (AZ4330) is spun on over the  $\text{Si}_3\text{N}_4$ . A mask layer of this thickness is required due to the depth of the pillar etch, which is more than 6 μm. Circular mesas are aligned with the p-metal rings and patterned. Edge bead removal prior to pattern exposure ensures good alignment and even intensity distribution. Large pillar diameters (30-50 μm) are used to lower thermal and electrical resistance. Portions of the  $\text{Si}_3\text{N}_4$  layer not covered by photoresist are etched using a  $\text{CF}_4$  plasma, leaving a photoresist/ $\text{Si}_3\text{N}_4$  mask over the p-metal rings. The patterned etch mask is shown in Figure 4.15.

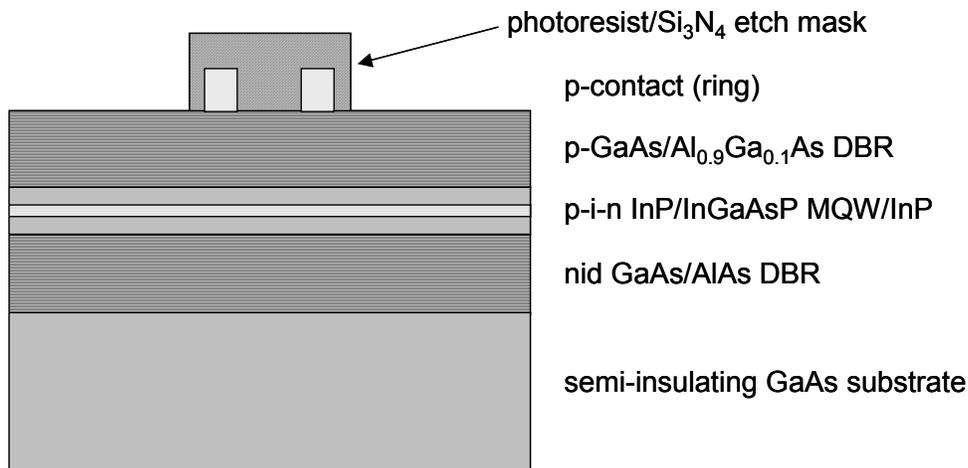


Figure 4.15 Bonded VCSEL structure with pillar etch mask

Baking the sample at 110°C for 2 minutes hardens the photoresist and makes the combined mask more resistant to the etch process. The pillars are defined using a reactive ion etcher (RIE) and a gas mixture of  $\text{BCl}_3/\text{Cl}_2/\text{SiCl}_4$ . A slight sidewall slope is actually desirable so that bridge metal from a bond pad can later be run up the pillar to connect to the p-metal ring. The etch proceeds through the p-DBR, bonded junction, p-cladding, and quantum wells before stopping on the n-cladding. The etch rate and depth are monitored using *in situ* laser reflectometry. Alignment and use of the laser monitor is made more difficult by the rough surfaces that may exist on bonded wafers. After the etch is complete, the sample is rinsed under running DI water to remove chlorine etch residue. Photoresist is removed using solvents. The  $\text{Si}_3\text{N}_4$  layer is left intact to protect the p-metal during the oxidation process.

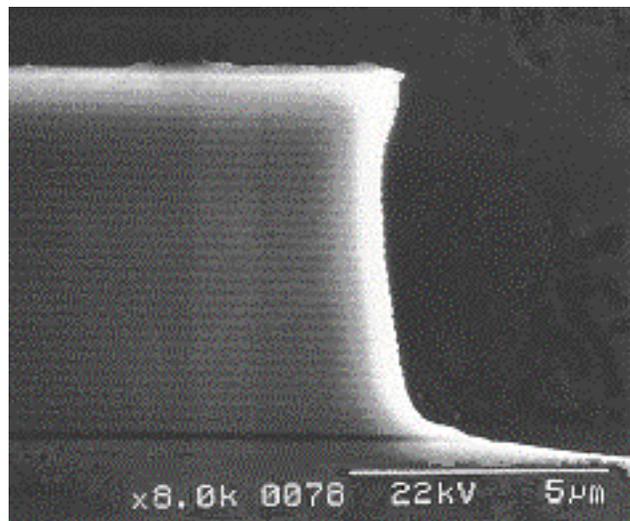


Figure 4.16 SEM image of etched VCSEL pillar

An oxide aperture is introduced for mode and current confinement, as described in Section 4.4. Steam oxidation at 440°C is used to laterally oxidize an  $\text{Al}_{0.98}\text{Ga}_{0.02}\text{As}$  layer at a rate of approximately 1  $\mu\text{m}/\text{minute}$ . An  $\text{NH}_4\text{OH}$  dip may be used prior to lateral oxidation to remove surface oxide.  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$  layers on either side of the oxidation layer create a taper that significantly reduces scattering loss in small aperture devices. The laterally oxidized structure is illustrated in Figure 4.13. An SEM image of an etched DBR pillar that has been laterally oxidized is shown in Figure 4.14.

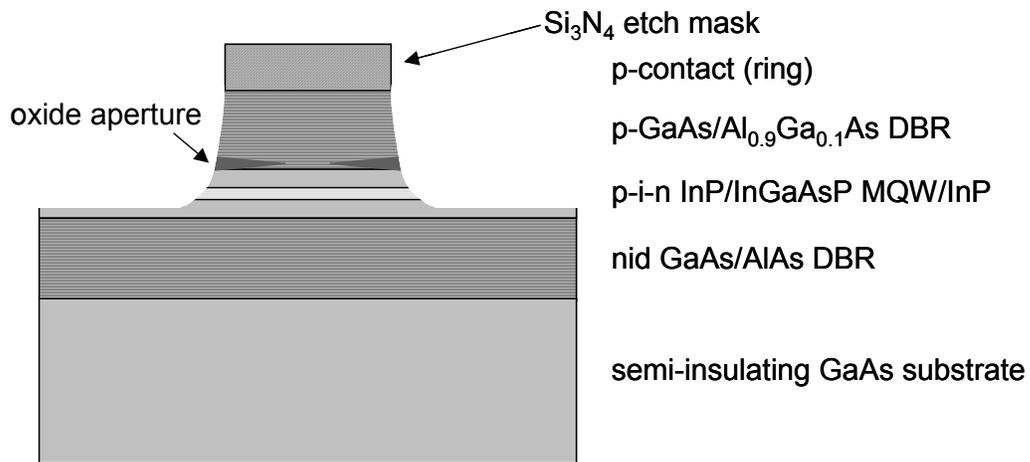
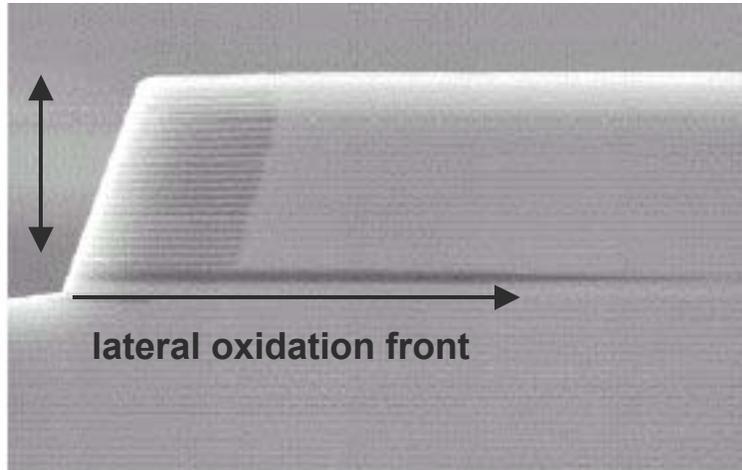


Figure 4.13 Bonded VCSEL structure with etched pillar



#### 4.8.4. *n*-metallization

After the oxidation process is complete, the  $\text{Si}_3\text{N}_4$  layer is removed using a  $\text{CF}_4$  plasma. A small region of exposed n-InP is etched away. The p-bondpad will eventually reside on  $\text{Si}_3\text{N}_4$  over this part of the device. This reduces bondpad capacitance, improving high-speed response. A ground-signal-ground configuration can then be used to enable high-speed testing. A new 4000 Å  $\text{Si}_3\text{N}_4$  layer is deposited over the entire sample. This thickness is required to provide isolation between the p-contact and n-contact. After depositing the first 2000 Å, the sample is dipped in methanol and dried. This helps to prevent pinholing in the  $\text{Si}_3\text{N}_4$  layer. The sample is then returned to the PECVD chamber for deposition of the final 2000 Å.

The  $\text{Si}_3\text{N}_4$  is patterned to open an emission window over the pillar and expose the n-InP cladding. The final metallization creates a p-bondpad, bridge metal from this bondpad to the p-contact and an n-contact on the n-InP cladding. It is critical that the  $\text{Si}_3\text{N}_4$  be completely removed before the final lithography takes place. Residual nitride will disrupt the bridge metallization and prevent completion of the p-contact. A double layer resist process using AZ5214 and OCG825 is used to obtain the required liftoff profile. This is a difficult lithography under the best of circumstances and can be further complicated by poor morphology or wide variations in feature size. The evaporated layer is composed of Ti/Au (100/3000 Å). The metals are deposited using rotating e-beam evaporation at a  $30^\circ$  angle to ensure sidewall coverage. A schematic of the device is presented in Figure 4.15. An SEM image of the p-metallization is shown in Figure 4.16a and a top-down photograph of the device in Figure 4.16b.

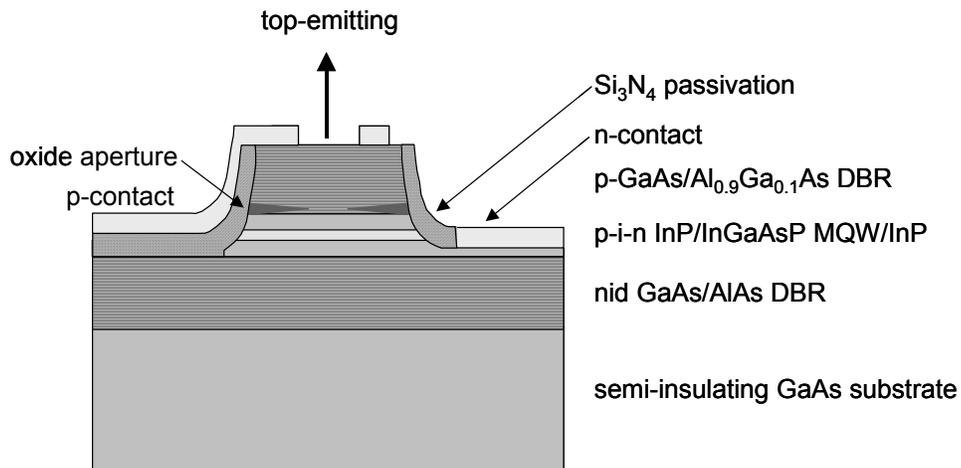


Figure 4.15 Wafer bonded VCSEL structure

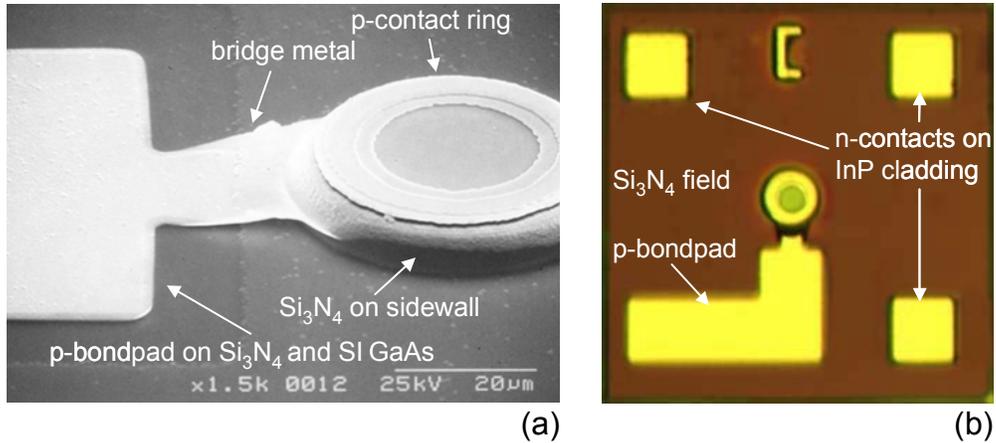


Figure 4.16a-b SEM and optical microscope images of finished device

#### 4.9. Summary

VCSEL design issues were presented. Design curves for the VCSEL structure under consideration were generated in order to determine parameters that would allow 1 mW of output power for a given loss level. The changes in reflectivity and material gain as a function of wavelength were used to estimate the wavelength span over which the threshold current would not vary significantly. This is important in determining the performance limits of multiple wavelength arrays and tunable lasers. Motivations for a half-intracavity and top-emitting design were presented. The fabrication process was summarized.

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## **5. Device Results and Analysis**

### **5.1. Introduction**

This chapter summarizes the performance of the devices discussed in Chapter 4, including both single VCSELs and multiple wavelength arrays. Three generations of devices are analyzed. The characteristics of interest include threshold current, voltage, output power, differential efficiency, spectra and high temperature operation. Thermal resistance is analyzed in detail. Major accomplishments in these areas include

- Electrically pumped operation of 1.55  $\mu\text{m}$  WDM VCSEL array with four wavelengths. This is the first report of electrically pumped WDM VCSEL arrays in the 1.3-1.55  $\mu\text{m}$  band.
- Continuous-wave operation up to 105°C. This is the highest reported CW operating temperature for a 1.55  $\mu\text{m}$  VCSEL
- Threshold current of 0.8 mA for a 5  $\mu\text{m}$  device

Limitations to performance are identified and device improvements are proposed.

## 5.2. Generation A: 85°C continuous wave operation

The devices discussed in this section were fabricated with a single wavelength active region containing 6 quantum wells and capped with a four period superlattice. The top mirror was a 25.5 period p-GaAs/Al<sub>0.9</sub>Ga<sub>0.1</sub>As DBR with an oxide aperture and a center wavelength of 1535 nm. The bottom mirror was a 31 period non-intentionally doped GaAs/AlAs DBR with a center wavelength of 1540 nm. The n-InP bondpad etch for reduced capacitance described in Section 4.8.4 was omitted in this generation of devices. Device size was determined by the depth of the oxide aperture. The VCSEL structure is shown in Figure 5.1. The cavity standing wave pattern and refractive index profile are shown in Figure 5.2.

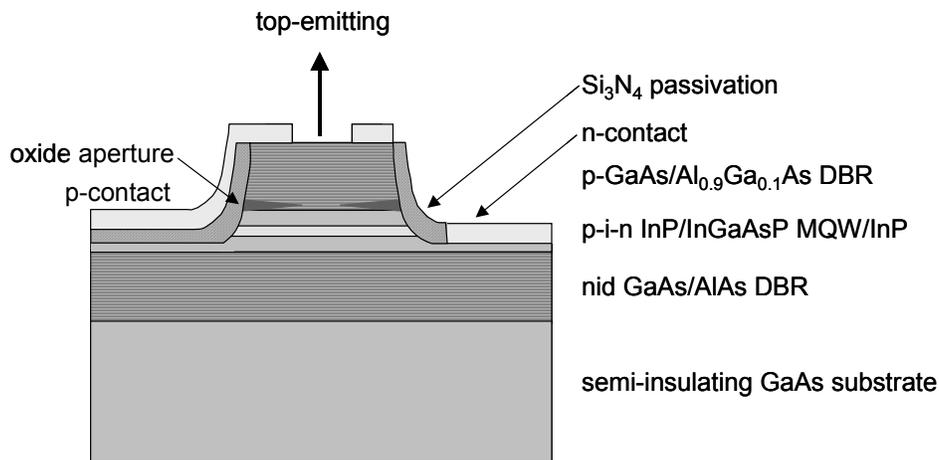


Figure 5.1 Generation A VCSEL device structure

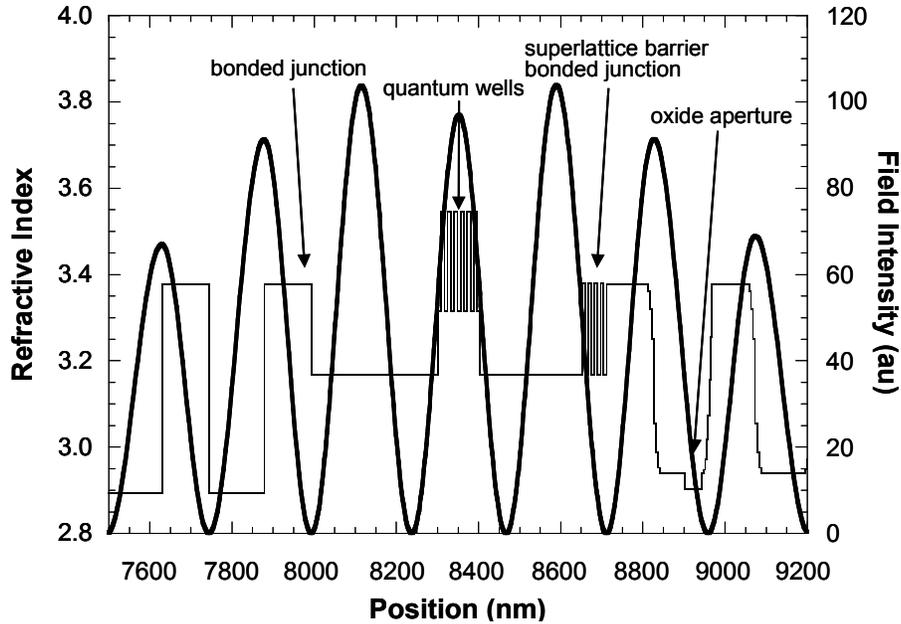


Figure 5.2 Refractive index profile and standing wave pattern in Generation A VCSEL

### 5.2.1. Room Temperature Performance

A typical light-voltage-current (L-V-I) characteristic is shown below for a device with a 6  $\mu\text{m}$  oxide aperture. Although the threshold current of 1.1 mA seems reasonable, the threshold voltage is surprisingly high compared to wafer bonded devices previously fabricated at UCSB. Clearly, the diode is not functioning as expected. Further investigation using transmission line measurements (TLM) on a test pattern indicated that the p-contacts were not ohmic and had a turn-on voltage of 3-4 V. It is believed that this is due to a fault in the p-contact metal or a poorly prepared p-contact layer. This excess voltage is

not related to the bonded junction. The high forward voltage does not impact lasing on the optical time scale, but will contribute significantly to device self-heating.

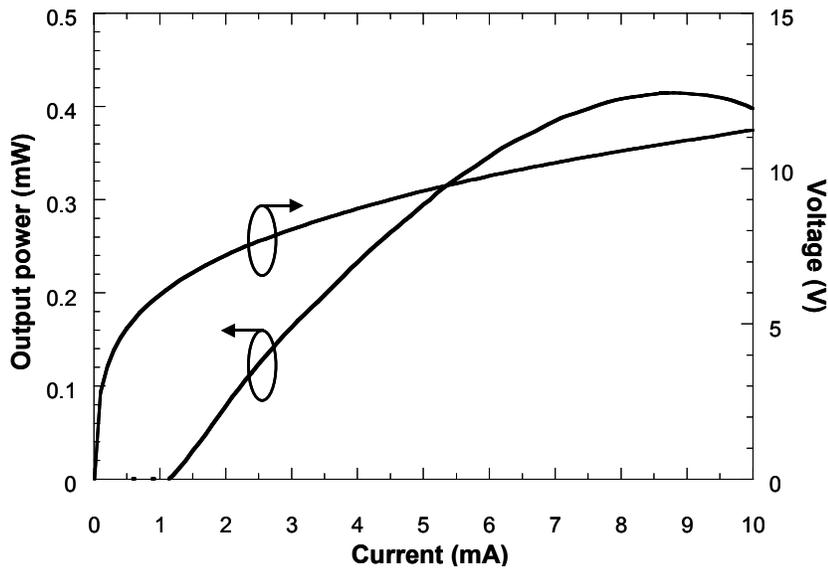


Figure 5.3 Room temperature (20°C) light-voltage-current characteristic of Generation A VCSEL with 6  $\mu\text{m}$  aperture

The lasing spectrum for a 5  $\mu\text{m}$  device at a bias current of 6 mA is shown in Figure 5.4. The lasing wavelength at this bias level is 1529.6 nm. The side mode suppression ratio (SMSR) is 45 dB. Single mode operation was observed over a wide range of currents for device sizes up to 5  $\mu\text{m}$ . Larger devices operated with multiple modes.

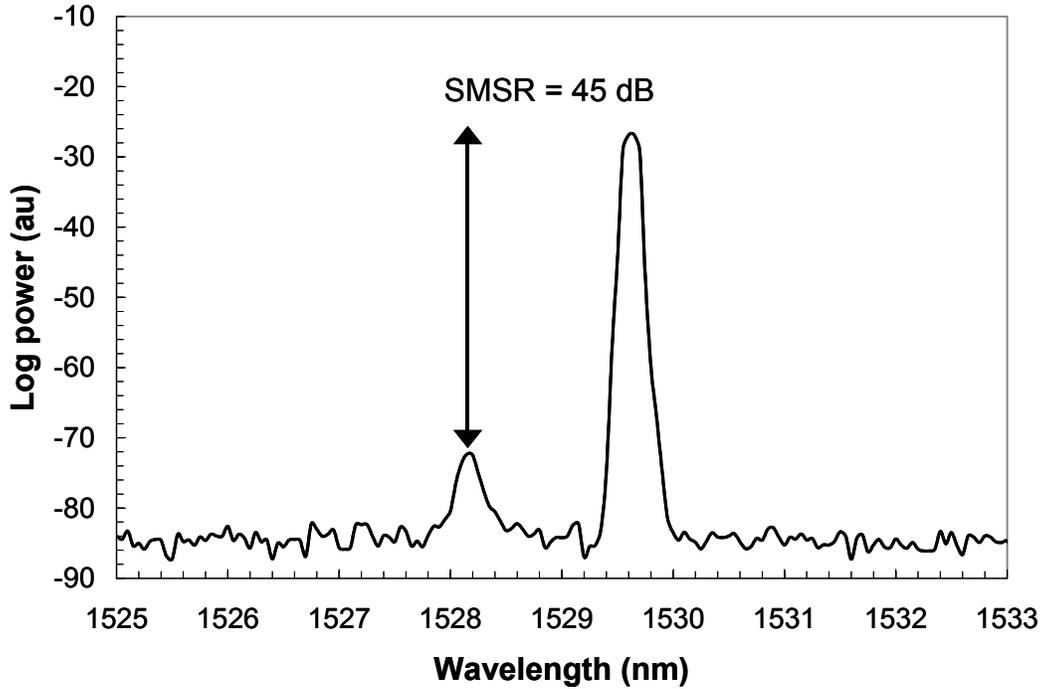


Figure 5.4 Single mode lasing spectrum from 5  $\mu\text{m}$  device with SMSR = 45 dB

### 5.2.2. High Temperature Performance

Based on photoluminescence measurements, the room temperature gain peak of the quantum well active region is estimated to be at 1544 nm. Both the lasing wavelength and peak gain wavelength increase with temperature. The lasing wavelength increases at a rate of 0.1 nm/ $^{\circ}\text{C}$ , and the peak gain wavelength increases at a rate of 0.5 nm/ $^{\circ}\text{C}$ [1]. The shift in lasing wavelength was confirmed during device testing, as illustrated in Figure 5.5.

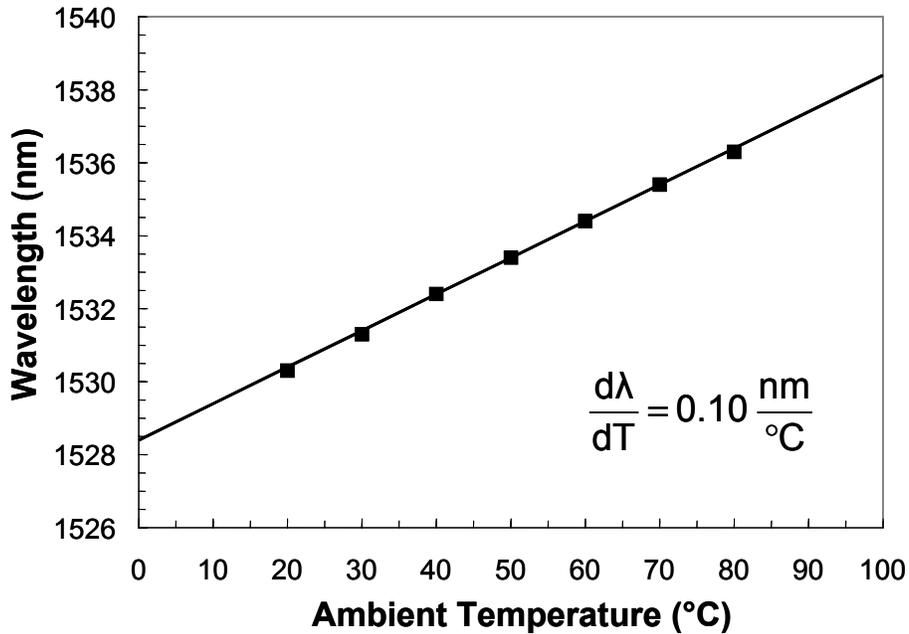


Figure 5.5 Shift in lasing wavelength with ambient temperature

If the lasing mode is on the short wavelength side of the gain peak at room temperature, the mode and gain will drift further apart at elevated temperatures. The combination of misaligned and reduced gain at higher temperatures will eventually limit device operation. The internal device temperature is also affected by device self-heating. Despite the high voltage and unfavorable mode-gain offset for these devices, continuous wave operation was achieved at temperatures as high as 85°C. A family of L-I curves for CW operation from 10-85°C is shown in Figure 5.6.

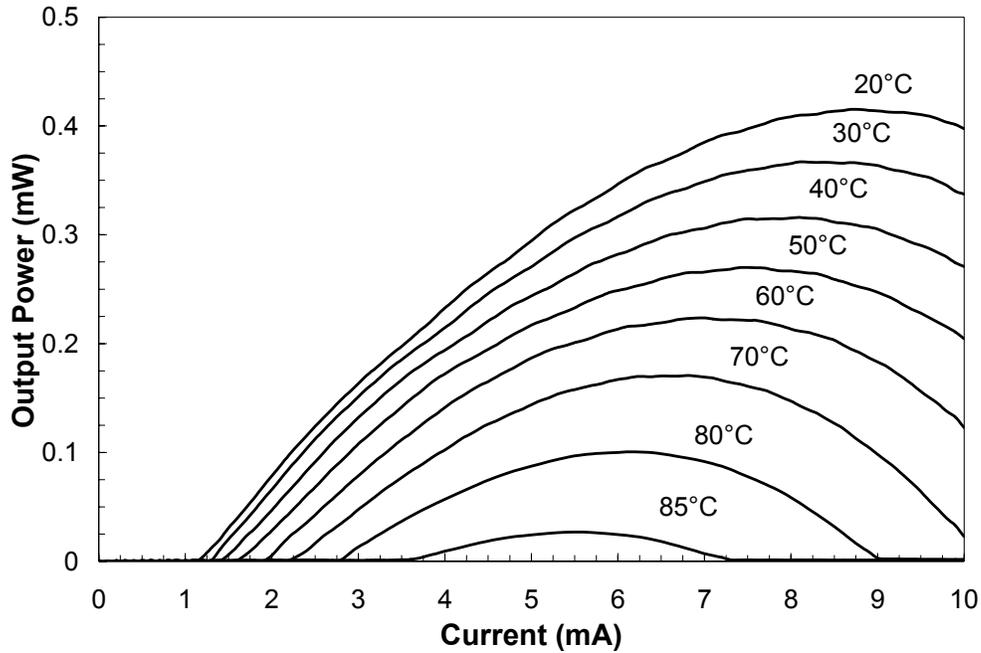


Figure 5.6 Continuous-wave L-I curves for ambient temperatures of 20-85°C

### 5.2.3. Thermal Resistance

The high temperature operation of these devices may be described using a simple thermal model that includes both ambient temperature and device self-heating. It is assumed that the device stops lasing once the active region reaches a certain maximum temperature,  $T_{\max}$ . This bias point is referred to as rollover and is illustrated below.

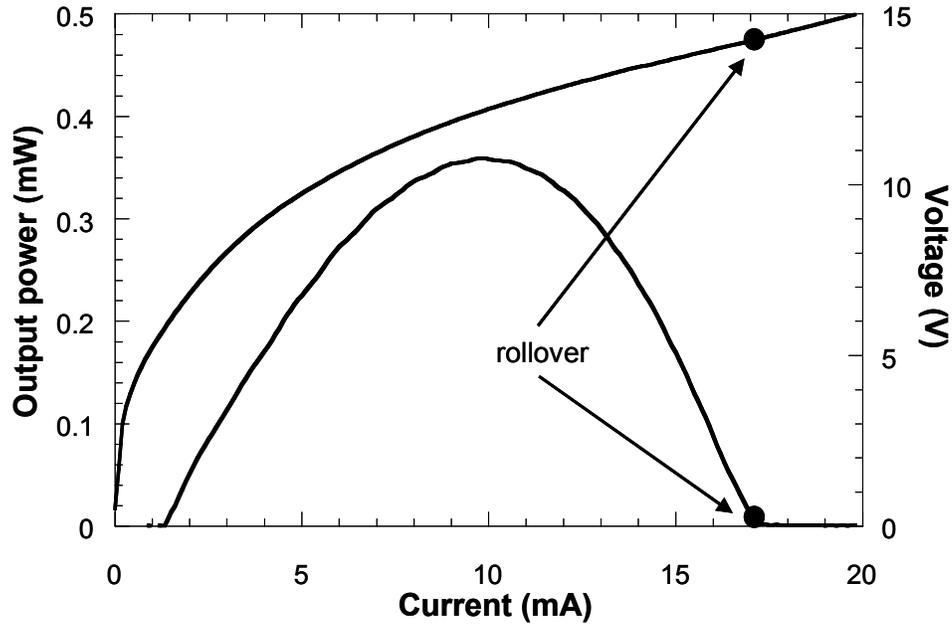


Figure 5.7 L-V-I characteristic with rollover point highlighted

The maximum active region temperature that will support lasing is assumed to be constant for all ambient temperatures.  $T_{\max}$  is equal to the ambient temperature,  $T_{\text{amb}}$ , plus the thermal resistance,  $R_{\text{th}}$ , multiplied by the dissipated electrical power,  $P_{\text{roll}}$ , at rollover. This can be expressed as the equation of a straight line, given by  $T_{\max} = T_{\text{amb}} + P_{\text{roll}}R_{\text{th}}$ . Data points and a linear fit for the device characterized in Figure 5.7 are shown below.

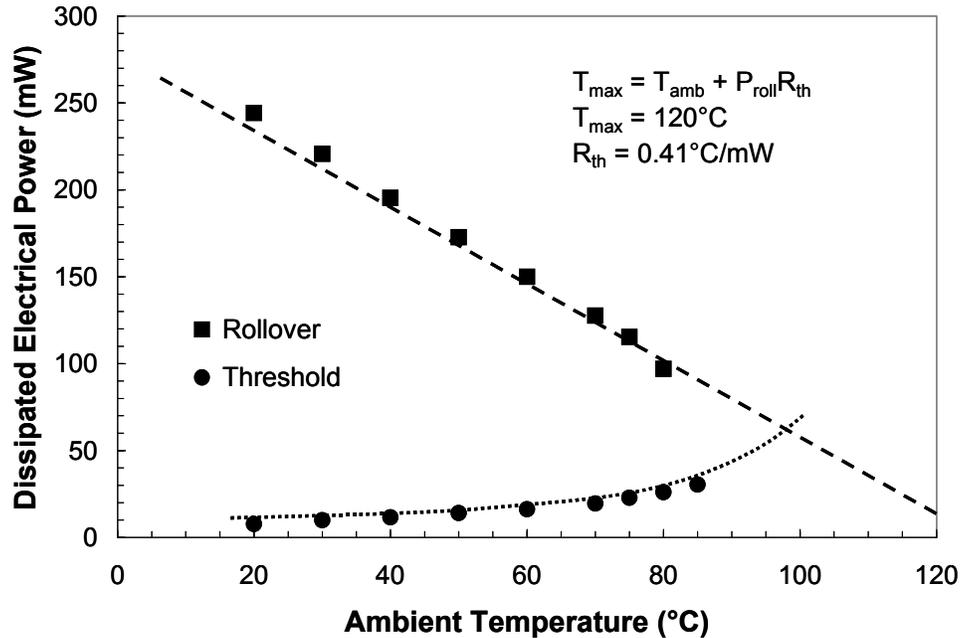


Figure 5.8 Dissipated electrical power and thermal resistance of 6  $\mu\text{m}$  device in 46  $\mu\text{m}$  pillar

The data points indicated by squares show the electrical power dissipated at the bias point where the L-I characteristic has rolled over and the device is no longer lasing. The data points indicated by circles show the electrical power dissipated at threshold. The continuous-wave operating regime is bounded by the threshold and rollover dissipated power curves. A thermal resistance of 0.41°C/mW is extracted from the linear fit for a device defined by a 46  $\mu\text{m}$  diameter pillar and 6  $\mu\text{m}$  diameter oxide aperture. The maximum active region

temperature that will support pulsed lasing is determined to be 120°C. The simple fit used to extract these parameters treats the active region temperature as a one-dimensional distribution. A higher degree of accuracy could be obtained by using a two or three-dimensional model to determine local heating within the active region.

The slope of the rollover dissipated power line is determined by the thermal resistance of the device. The device design is already well-optimized for high thermal conductivity. The measurements described in this chapter were made after mounting the VCSEL chip on a temperature-controlled copper stage using a thermally conductive paste. Devices were tested in a p-side up configuration without additional special heat sinking. The thermal resistance could be reduced slightly with an improved packaging scheme such as flip-chip bonding. However, in order to maintain a cost advantage over edge-emitting lasers, it is desirable to keep VCSEL device mounting as simple as possible. The x-intercept of the dissipated power line corresponds to the maximum lasing temperature under pulsed operation (no device self-heating). This maximum temperature can be increased by providing higher material gain at elevated temperatures. Increased gain above room temperature may be provided through improved quantum well design or by switching to an active region material with superior high temperature

gain characteristics, such as AlInGaAs. The gain available to the lasing mode is determined by the peak material gain and the mode-gain offset. Proper alignment of the mode position and gain peak would lead to increased modal gain and a higher maximum lasing temperature. The bottom boundary of the continuous-wave operating regime may be lowered by reducing the threshold current or voltage. The effects of reducing threshold voltage will be seen in Generation B devices.

The thermal resistance of the device can be used to determine the thermal conductivity of the bottom DBR. The bottom DBR separates the heat source (active region) from the heat sink (substrate and copper stage). For a disk source on a large substrate, three-dimensional heat flow may be assumed. The thermal resistance may be expressed as[2]:

$$R_{th} = \frac{1}{2\kappa_{DBR}d}$$

**Equation 5.1**

where  $\kappa_{DBR}$  is the thermal conductivity of the bottom DBR and  $d$  is the pillar diameter. Using the thermal resistance value calculated above, the thermal conductivity of the bottom DBR is determined to be 0.263 W/cm K. This value is only slightly lower than the expected value for GaAs and AlAs in parallel.

<b>Material</b>	<b>Thermal conductivity (W/cm K)</b>
GaAs	0.44
AlAs	0.91
GaAs/AlAs DBR (calculated parallel)	0.297
GaAs/AlAs DBR (actual)	0.263

**Table 5.1 Thermal conductivities of GaAs, AlAs and GaAs/AlAs DBR**

This slight deviation is due to phonon scattering. A portion of the phonon energy is scattered at each heterointerface, limiting heat transport in the transverse direction. This effect limits thermal conductivity in all DBR structures containing a large number of interfaces. Despite this reduction, the thermal conductivity of GaAs/AlAs DBRs is still higher than that of other long wavelength DBRs

Knowing the thermal resistance of the device, the L-I characteristic may be used to determine the internal device temperature as a function of bias current. The temperature rise relative to the ambient temperature is given by the product of bias current, bias voltage and thermal resistance. Output power and internal device temperature are plotted in Figure 5.9 for the device with the L-I characteristic shown in Figure 5.7.

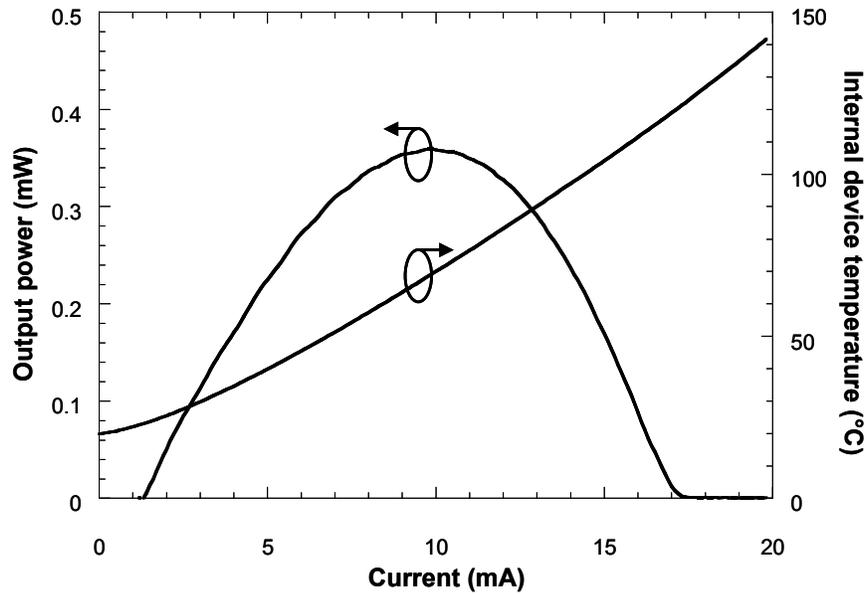


Figure 5.9 Output power and internal device temperature versus bias current at 20°C

It should be noted that superior thermal performance was achieved on a large number of devices. Thirty-seven VCSELs of various sizes that passed current were characterized over a range of temperatures. All of these devices had maximum continuous-wave operating temperatures of 65°C or greater. This may be taken as an indication of VCSEL consistency and quality across the entire sample. A histogram of the maximum CW operating temperature is plotted in Figure 5.10.

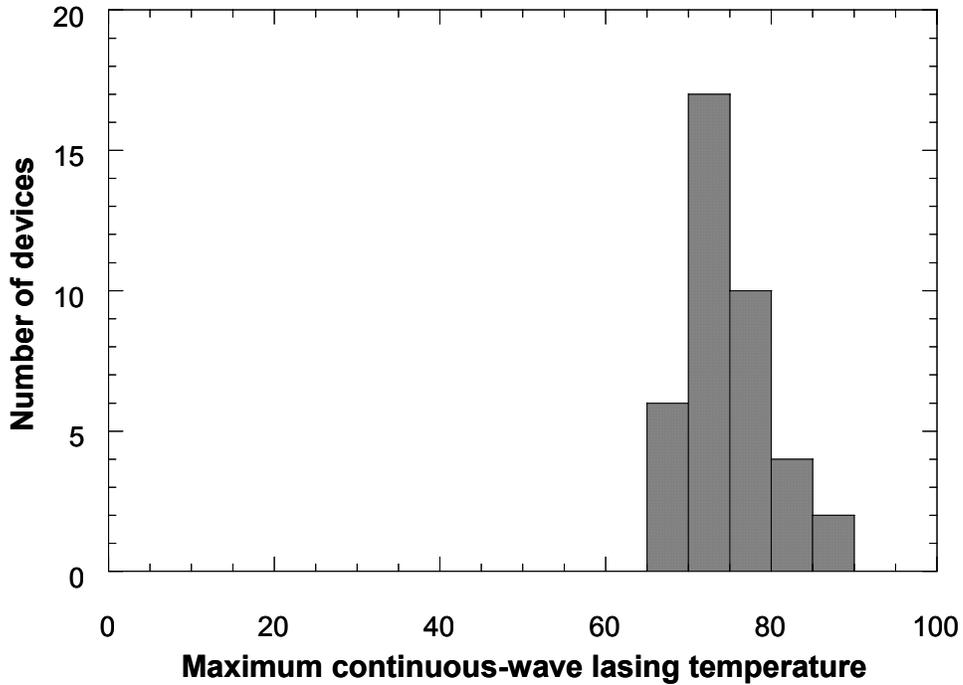


Figure 5.10 Histogram of maximum CW lasing temperatures for Generation A devices

#### 5.2.4. Threshold current and differential efficiency

The high temperature performance of semiconductor lasers with InGaAsP active regions has been studied extensively[3]. Previous calculations performed on bonded VCSEL structures have indicated that Auger recombination is the dominant non-radiative current path at elevated temperatures, followed by vertical carrier leakage[4]. Internal losses are increased at higher temperatures due to a rise in intervalence band absorption. These mechanisms lead to a thermal runaway process. Greater amounts of current are required to provide the gain needed to

compensate for an internal temperature increase. This additional injected current further increases the temperature of the device, creating the need for even more current. This process limits the differential efficiency and maximum output power of the laser. The internal efficiency is reduced at higher temperatures by vertical electron leakage. Due to a low effective mass and shallow conduction band potential wells, injected electrons can easily overshoot the quantum well region or escape before recombining radiatively. The threshold current is affected by the same mechanisms. In Figure 5.11, the continuous-wave threshold current density and differential efficiency are plotted as a function of ambient temperature for a 6  $\mu\text{m}$  device. It should be noted that the threshold current density is calculated based on the diameter of the oxide aperture, although there may be significant current spreading beyond that point.

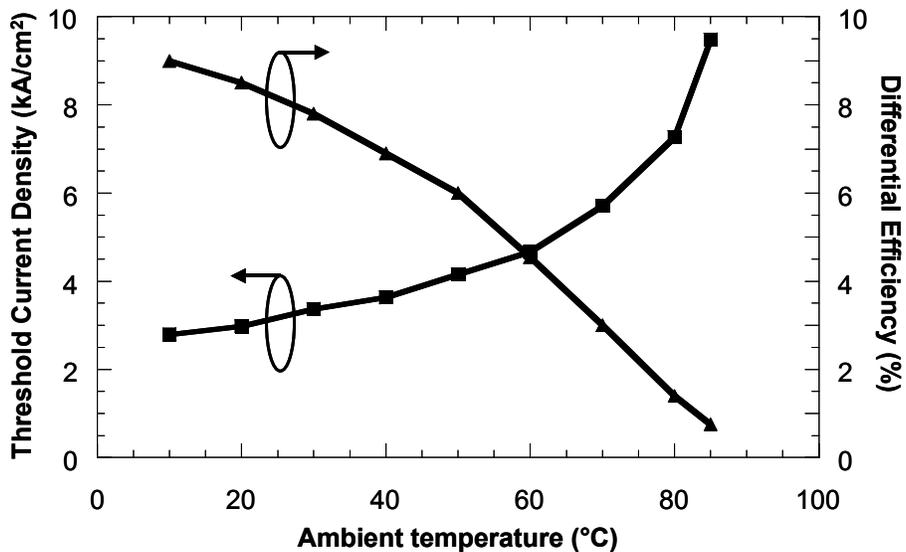


Figure 5.11 Continuous-wave threshold current density and differential efficiency versus ambient temperature for a device with a 6  $\mu\text{m}$  oxide aperture

The scaling of threshold current density with device size is also of interest. Non-ideal scaling is an indication of size dependent injection or loss mechanisms, such as current spreading or scattering by the oxide aperture. The continuous wave threshold current,  $I_{th}$ , and threshold current density,  $J_{th}$  are plotted below versus the oxide aperture diameter. Due to the low thermal resistance, the observed threshold currents are nearly identical under pulsed and continuous-wave operation. Differential efficiencies also track closely for modest bias currents. Threshold current and differential efficiency values may be extracted from pulsed or CW curves with no loss of accuracy.

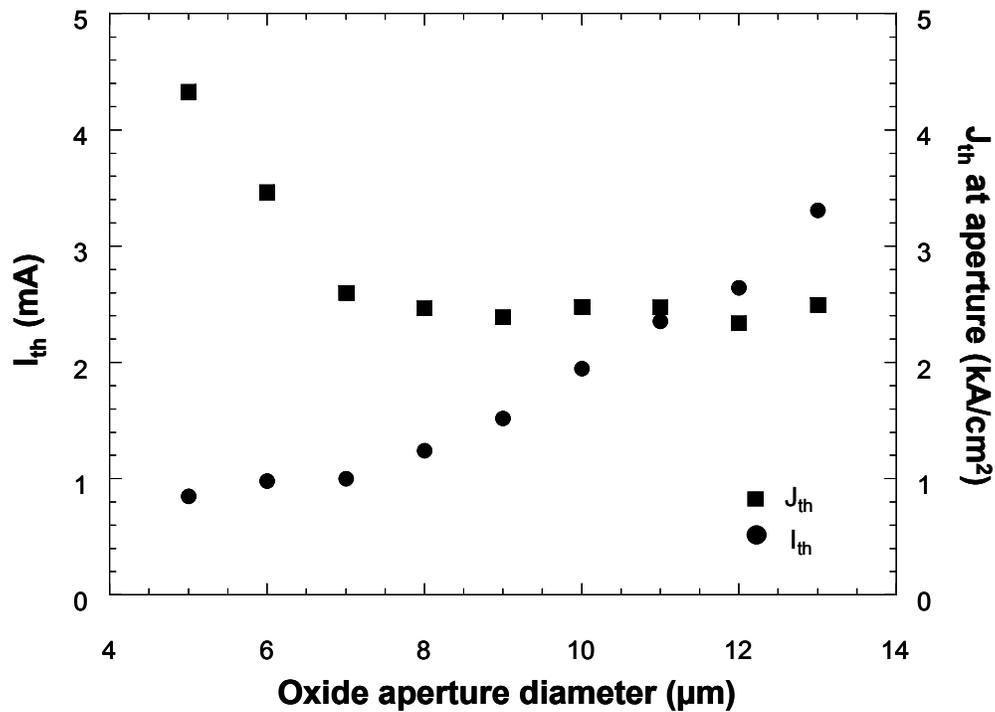


Figure 5.12 Threshold current and aperture threshold current density versus aperture diameter

The data suggests a broad-area aperture threshold current density of 2.4 kA/cm<sup>2</sup> for this generation of devices. The threshold current decreases monotonically with device size until the aperture diameter reaches 7 μm. The saturation of threshold current and sharp rise in threshold current density at that point indicate the presence of a size-dependent loss mechanism. The diameter of 7 μm is too large for scattering losses to reach appreciable values. The increased current spreading in bonded long wavelength VCSELs compared to short wavelength VCSELs is due to a number of factors. The current confining aperture in these wafer bonded VCSELs is more than 400 nm from the quantum well region, compared to 50 nm or less in short wavelength VCSELs. The lack of a robust aperturing technique on InP forces aperture placement in the GaAs/AlGaAs DBR. The injected current must travel across the bonded junction and p-InP cladding before reaching the active region, spreading in response to electrical resistance. The bonded junction is highly resistive, as discussed in Chapter 2. This forces current to spread laterally. The use of zinc as a p-type dopant also influence electrical characteristics. Due to high p-type absorption losses, a low doping level is chosen in the p-InP cladding. The high diffusivity of zinc during the growth and bonding processes makes it essential to leave the 1000 Å of InP cladding nearest the quantum wells undoped to prevent damage to the active region.

These effects combine to make current spreading a major contributor to high threshold current for devices with an aperture diameter of 8  $\mu\text{m}$  or less. A model for current spreading, developed by Hegblom, describes the threshold current in terms of a broad-area threshold current density,  $J_{ba}$  and a parameter  $I_0$  that is a function of sheet resistance and diode ideality factor beneath the aperture[5]. Since these two factors are rarely known with great precision,  $I_0$  is generally used as a fitting parameter. The expression for threshold current is given below.

$$I_{th} = J_{ba}\pi r^2 + \frac{I_0}{2} + \sqrt{J_{ba}\pi r^2 I_0} \quad \text{Equation 5.2}$$

where  $r$  is the aperture radius. Spreading contributions are included in the final two terms. The first of these terms,  $I_0/2$  is independent of device size. The next term scales linearly with aperture diameter. Measured threshold current data is plotted in Figure 5.13, along with calculated curves that illustrate ideal scaling of the broad-area threshold current and the spreading model described above.

The black circles indicate measured threshold currents for Generation A devices. The dashed line shows ideal scaling of threshold current for a threshold current density of 1.91  $\text{kA}/\text{cm}^2$ . The solid line shows how the threshold current

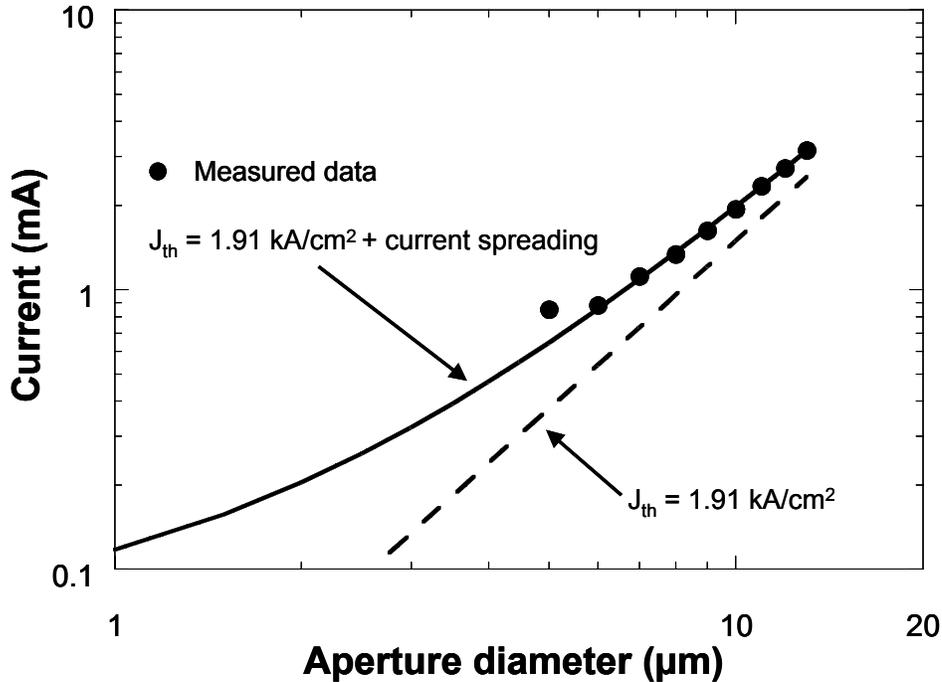


Figure 5.13 Threshold current versus oxide aperture diameter

scales using the same broad area threshold current density and using the expression above to include the effects of spreading beneath the aperture. This analysis suggests that 20-40% of the measured threshold current was due to current spreading, depending on aperture size. Although the solid line shows an improved fit, the spreading model used does not appear to give a complete description of threshold current for small devices. Previous analysis by Margalit, including near-field imaging, attributed this effect to reduced mode-gain overlap[6]. The small index perturbation of the oxide aperture does not effectively

confine the mode at small diameters, reducing the transverse confinement factor and increasing threshold. Additionally, current spreading at the bonded junction may not be adequately described by the model above. Further discussion of current spreading, including calculated profiles for the hole current density will be presented in Section 5.3.

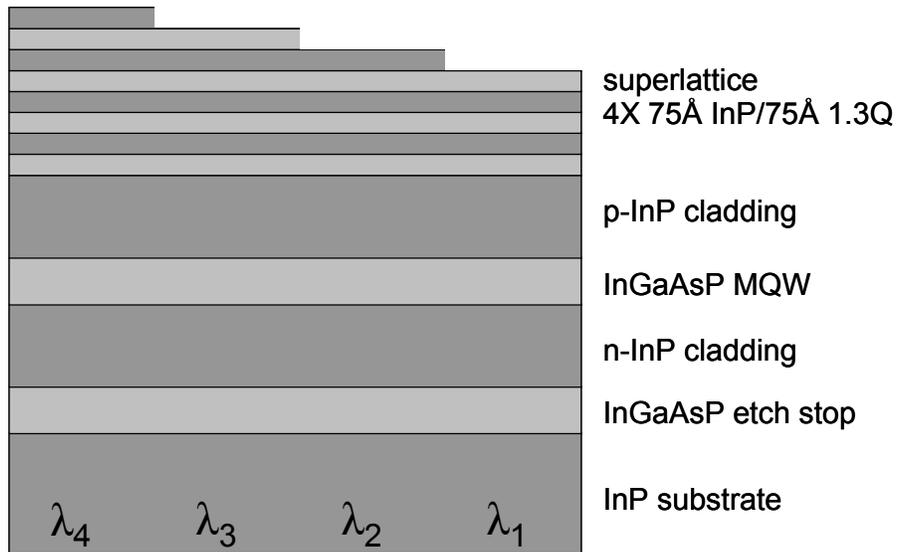
#### *5.2.5. Summary*

Electrically pumped, double bonded VCSELs with a lasing wavelength of 1528 nm were fabricated. The maximum CW operating temperature achieved was 85°C. At the time, this was the highest CW operating temperature reported for an electrically pumped long wavelength VCSEL. All devices lased under CW operation at temperatures up to 65°C. The maximum output power at 20°C was 0.55 mW. Previously fabricated devices without a superlattice barrier had a maximum CW operating temperature of 74°C and a maximum output power of 0.5 mW at 20°C[7]. Performance improvements relative to previous bonded VCSELs fabricated at UCSB are attributed to reduced loss in the p-mirror and fewer non-radiative recombination centers in the bonded active region. The maximum output power at 70°C was 62  $\mu$ W. Threshold currents of 0.9 mA were obtained for a 6  $\mu$ m aperture. The lowest aperture threshold current density measured was 1.9 kA/cm<sup>2</sup> for an 13  $\mu$ m aperture. Performance improvements are

expected for devices with a more favorable mode-gain offset, lower turn-on voltage and reduced series resistance.

### **5.3. Generation B: Multiple wavelength arrays, 105°C continuous wave operation**

The high temperature performance of Generation A VCSELs was limited by device self-heating. Analysis of the thermal resistance suggested that continuous-wave operation at temperatures over 100°C would be possible if the threshold voltage could be reduced to 3 V. As the high diode voltage and resistance were attributed to poor metallization, this goal is certainly within reach. An additional goal in this generation of devices is the fabrication of multiple wavelength arrays using the intracavity superlattice tuning layer described in Chapters 3 and 4. Prior to bonding, single layers of InP or InGaAsP were selectively etched on a 250  $\mu\text{m}$  pitch to define  $\Delta\lambda \approx 5$  nm between adjacent devices, as shown in Figure 5.14. This pattern was repeated over the entire sample. Reasonably uniform performance is expected over the tuning range of 15 nm as discussed in Chapter 4.



**Figure 5.14** Patterned intracavity superlattice for multiple wavelength cavity definition

The same epitaxial material was used in the fabrication of Generation B devices as was used in Generation A devices. The actual device structure was nearly identical. A slightly different mask set was used, with pillar dimensions and bondpad layout varying from the Generation A design. Other than variation with size, these changes are not expected to affect DC device performance. It is expected that the superlattice layer will not only provide 5 nm wavelength tuning between devices, but that the unetched superlattice periods will preserve active region quality as described in Chapter 3.

5.3.1. Room Temperature Performance

A light-voltage-current (L-V-I) characteristic is shown below for a device with a 44  $\mu\text{m}$  pillar and 7  $\mu\text{m}$  oxide aperture. The threshold current of 1.0 mA is similar to the values observed for Generation A devices. However, the threshold voltage has been sharply reduced. A 7  $\mu\text{m}$  device from Generation A had a threshold voltage of 6.6 V and a series resistance of 430  $\Omega$ . A Generation B device with the same aperture dimension has a threshold voltage of 2.5 V and a series resistance of 325  $\Omega$ . This voltage reduction is due to an improved p-contact. The reduced device self-heating manifests itself in higher peak output power and is expected to improve high temperature performance as well.

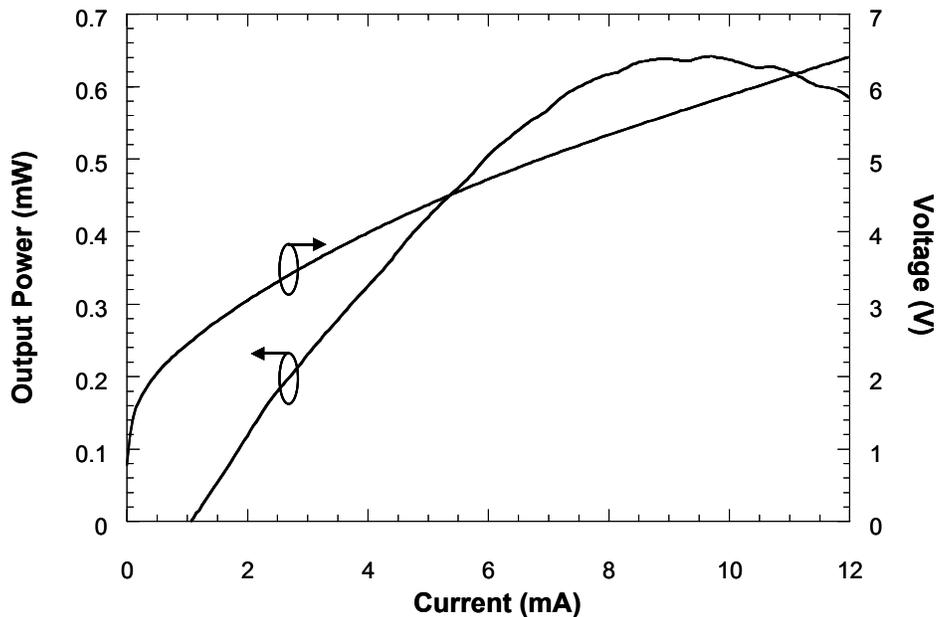


Figure 5.15 Room temperature (20°C) L-V-I characteristic of Generation B VCSEL with aperture diameter of 7  $\mu\text{m}$

Light-current characteristics are shown in Figure 5.16 for four adjacent 5  $\mu\text{m}$  devices. Threshold currents are nearly uniform across the array, varying between 1.04 and 1.10 mA. This is well within the limits expected based on earlier calculations. The slight variations in threshold and differential efficiency can be attributed to the different mode-gain-reflectivity offsets of the channels, as discussed in Chapter 4. Channel 1 refers to the device with the shortest wavelength and Channel 4 refers to the device with the longest wavelength.

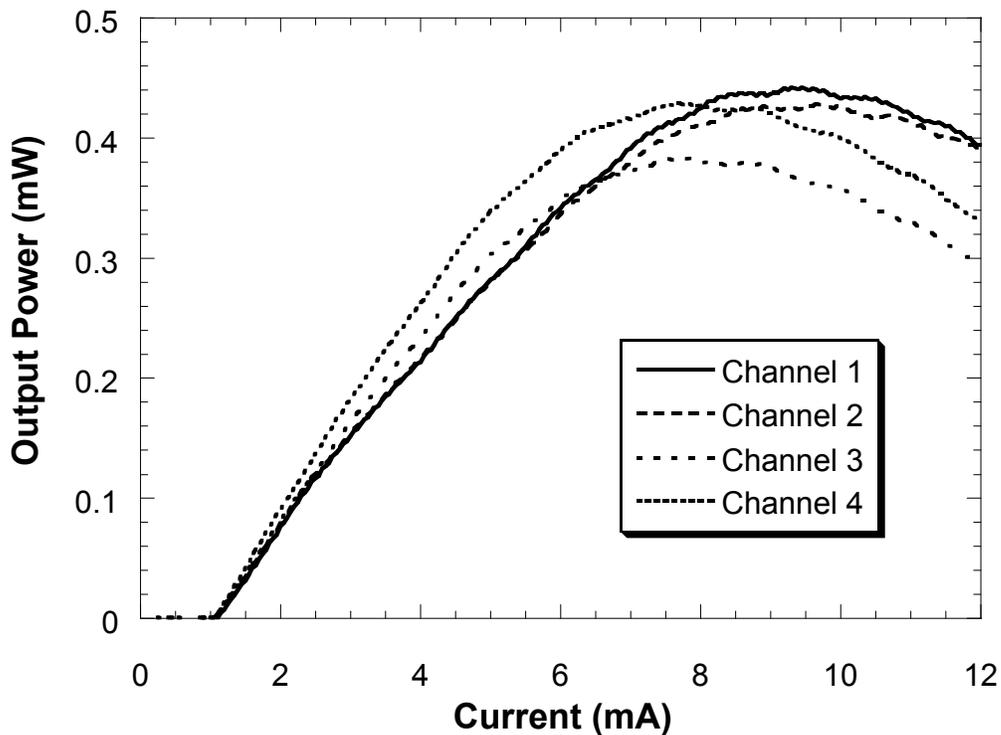


Figure 5.16 L-I characteristics for four adjacent 5  $\mu\text{m}$  devices in WDM VCSEL array

Uniformity in threshold voltage and series resistance is also desirable, so that the same power supply may be used to drive each element in the array. Similar electrical characteristics would also ensure similar thermal performance, encompassing both peak output powers and operation at high ambient temperatures. Voltage-current characteristics for the VCSEL array above are shown in Figure 5.17.

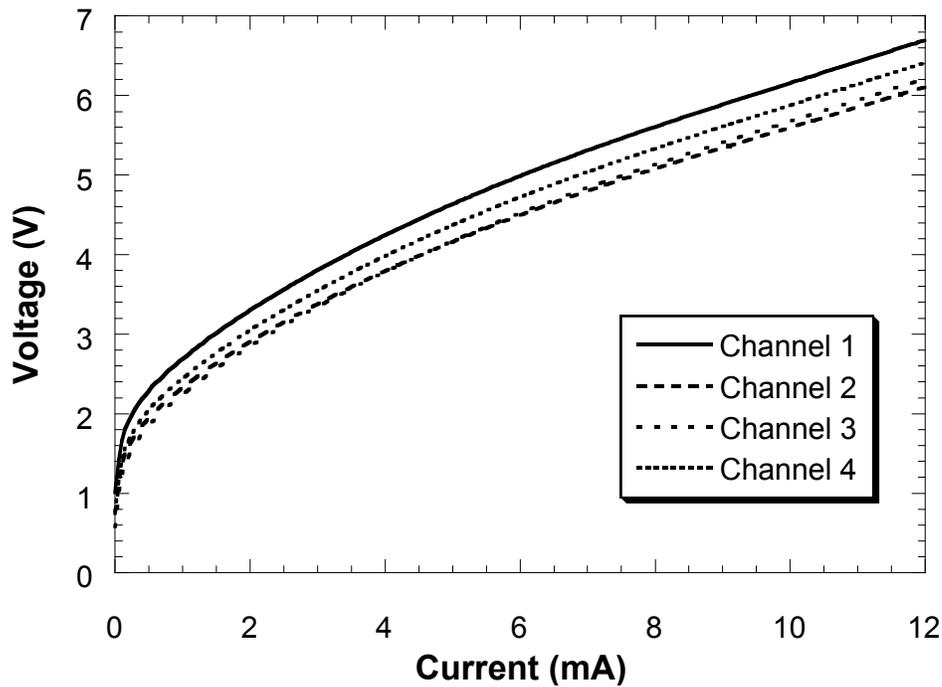


Figure 5.17 V-I characteristics for four adjacent 5  $\mu\text{m}$  devices in WDM VCSEL array

The theoretical effects of patterned bonding on diode characteristics are difficult to estimate. In practice, similar voltage-current characteristics were

measured across a number of VCSEL arrays. No systematic voltage dependence on channel number was observed. For the array with the characteristics shown above, the diode turn-on voltage varied between 1.7 and 2.0 V, as determined by the intercept of the linear portion of the diode characteristic with the y-axis. The threshold voltage was between 2.2 and 2.6 V. The series resistance varied between 283 and 333  $\Omega$ .

Lasing spectra at a bias of 6 mA are shown in Figure 5.18 for the WDM VCSEL array. The lasing wavelengths are 1509.1 nm, 1513.8 nm, 1518.6 nm, and 1524.4 nm. The active region photoluminescence peak is at 1542 nm and the output DBR reflectivity peak is at 1535 nm. All four channels are on the short wavelength side of the gain and reflectivity peaks. The higher numbered channels are located at longer wavelengths and are expected to have lower threshold currents and lower differential efficiencies, balancing device performance. The exact wavelengths depend on the thickness of the tuning layers. Increased control over the channel spacing is expected with improved superlattice growth and etch conditions.

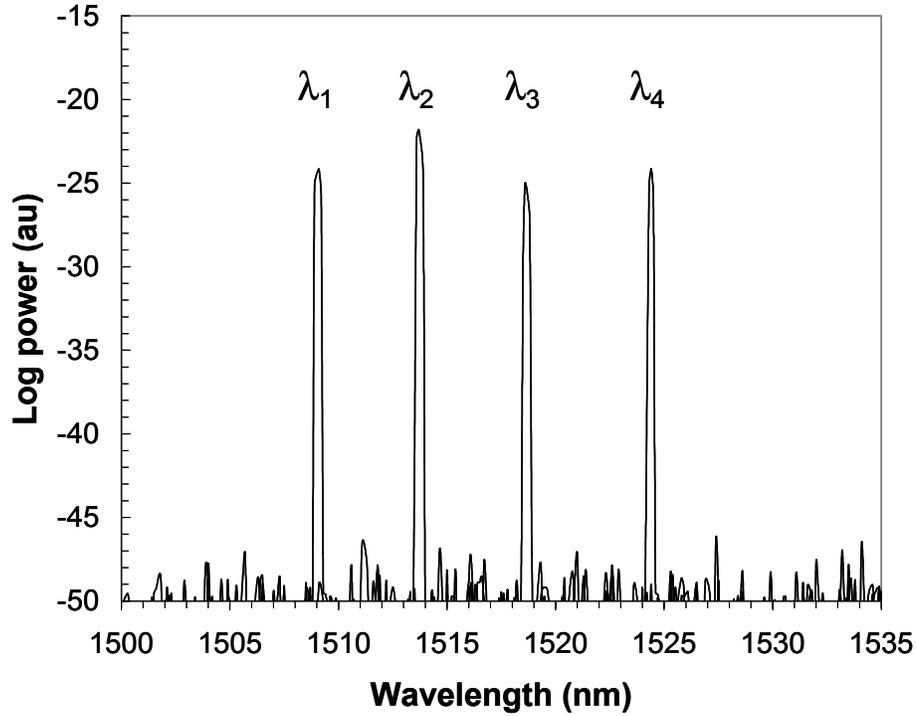


Figure 5.18 Lasing spectra for four adjacent 5  $\mu\text{m}$  devices in WDM VCSEL array

Characteristics for the WDM VCSEL array with an aperture diameter of 5  $\mu\text{m}$  are summarized in the table below.

Channel #	$\lambda$ (nm)	$I_{\text{th}}$ (mA)	$V_{\text{th}}$ (V)	$R_s$ ( $\Omega$ )	Peak output (mW)
1	1509.1	1.10	2.77	333	0.443
2	1513.8	1.08	2.40	283	0.429
3	1518.6	1.08	2.31	299	0.390
4	1524.4	1.07	2.52	310	0.431

Table 5.2 Summary of WDM VCSEL array results for 5  $\mu\text{m}$  aperture diameter

The lowered threshold voltage and series resistance indicate that high temperature operation beyond 85°C should be possible with this generation of devices. Since the same epitaxial material was used, the VCSEL thermal conductivity of the structure should be identical to that of previously fabricated devices. It follows that the thermal resistance should also remain unchanged for devices with the same pillar size. A family of L-I curves for continuous-wave operation from 20-105°C is shown in Figure 5.19. The room-temperature L-V-I characteristic of this VCSEL is shown in Figure 5.20. This device was channel 4 in a WDM array and had a lasing wavelength of 1526 nm.

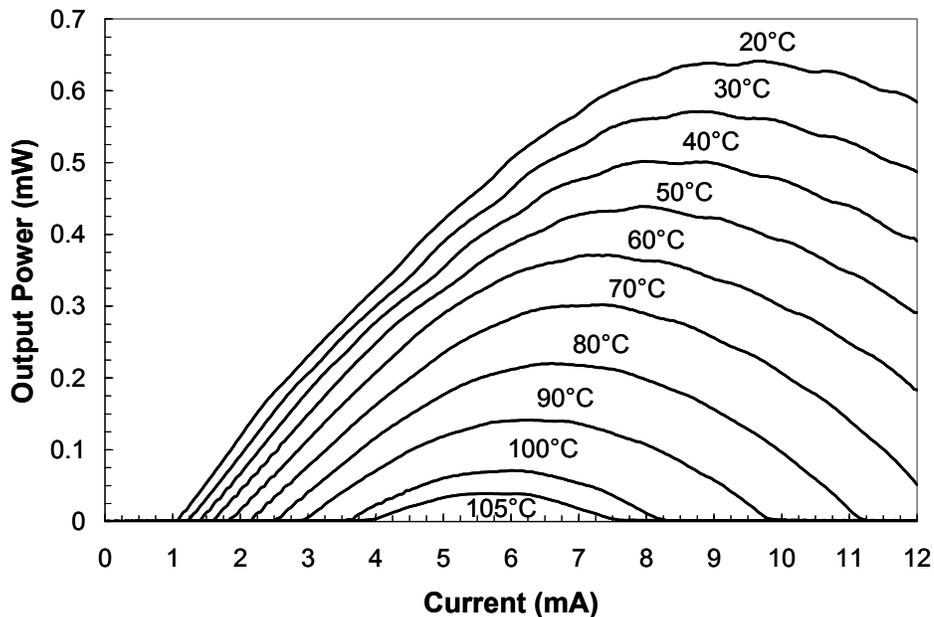


Figure 5.19 Continuous-wave L-I curves for ambient temperatures of 20-105°C

It should be noted that the mode-gain offset is in fact slightly larger for this generation of devices, even for the longest array wavelength. The improved high temperature performance relative to previously fabricated devices is due to reduced diode turn-on voltage and lowered differential resistance.

### 5.3.2. Thermal Resistance

The thermal resistance of these devices can be analyzed using the technique described in Section 5.2.3. Devices with 6  $\mu\text{m}$  apertures in 46  $\mu\text{m}$  pillars from each of the generations are compared. The results are plotted in Figure 5.20.

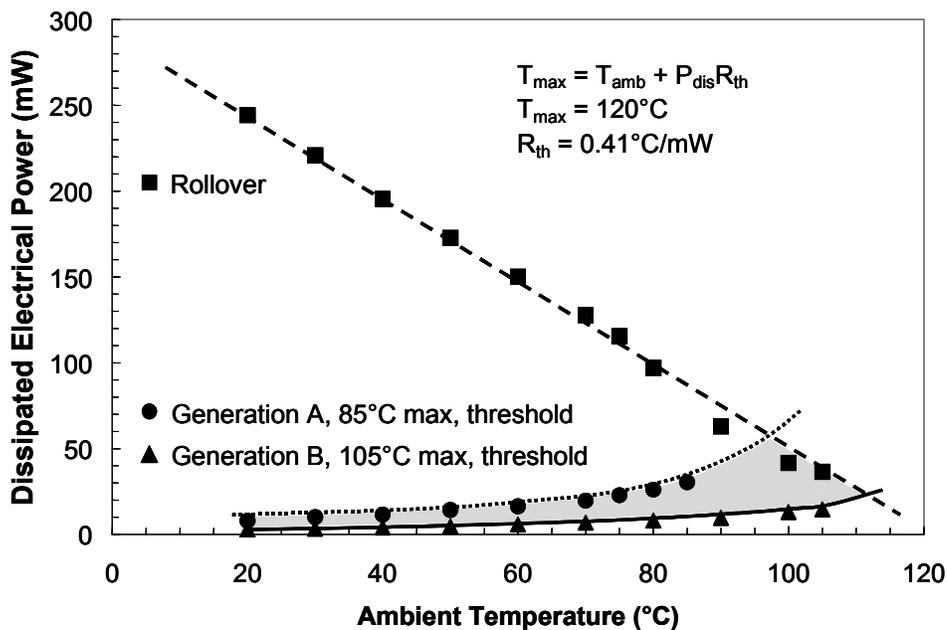


Figure 5.20 Thermal resistance and maximum operating temperature for Generation A and Generation B VCSELs with identical dimensions.

As expected, the dissipated electrical power at rollover for the Generation B device at temperature above 85°C falls along the same line established by the Generation A device. Since the devices have the same active region and thermal conductivity, the same amount of dissipated power will cause identical heating in the active region. The difference between the two generations lies in the amount of power required to reach threshold. The reduced threshold voltage of Generation B devices opens a larger window between the threshold and rollover power curves, enabling continuous-wave operation at temperatures up to 105°C. The shaded area shows the increased range of ambient temperatures and dissipated electrical powers over which Generation B devices are capable of operating. For identical device dimensions, the two generations of devices have the same thermal resistance of 0.41°C/mW, indicating a bottom DBR thermal conductivity of 0.263 W/cm K.

The thermal resistance increases with decreasing pillar diameter, as heat must flow through a smaller area to the copper stage. The thermal conductivity of the bottom DBR may be extracted or confirmed by observing the variation of thermal resistance with pillar diameter, according to the expression

$$R_{th} = \frac{1}{2\kappa_{DBR}d}$$

**Equation 5.3**

where  $R_{th}$  is the device thermal resistance,  $\kappa_{DBR}$  is the thermal conductivity of the bottom DBR and  $d$  is the pillar diameter. The linear fit technique described in Section 5.2.3 was used to determine thermal resistance for pillar diameters of 44-52  $\mu\text{m}$ . These results are plotted below, including a curve fit using  $\kappa_{DBR} = 0.263$  W/cm K.

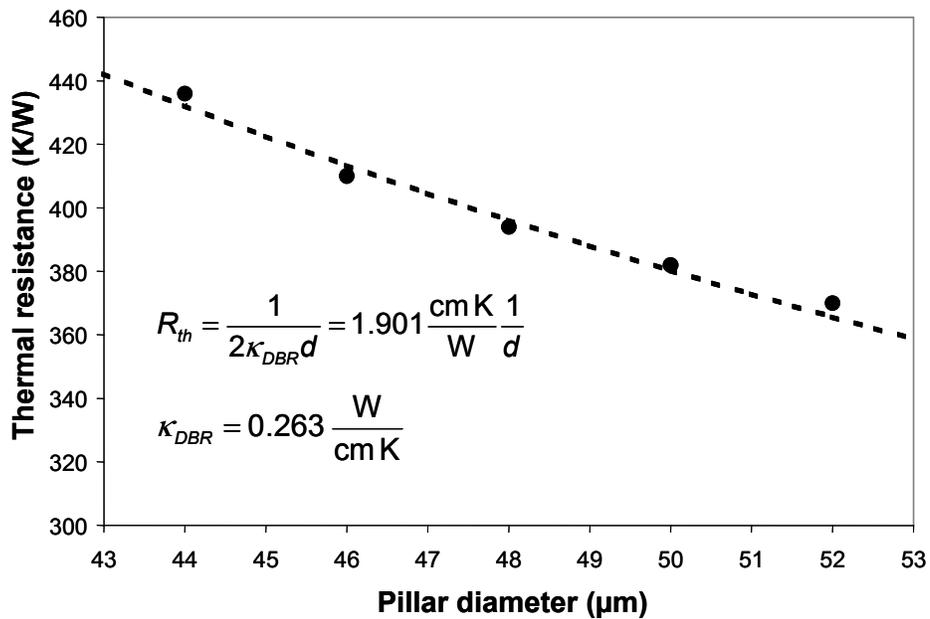


Figure 5.21 Thermal resistance versus pillar diameter

The thermal resistance scales with a  $1/d$  dependence that is suitably described with  $\kappa_{DBR} = 0.263$  W/cm K. This provides additional confirmation of the values extracted using single device sizes from each of the two VCSEL generations.

5.3.3. Threshold Current and Differential Efficiency

The threshold current density and differential efficiency for a 6  $\mu\text{m}$  device are plotted below over a range of temperatures.

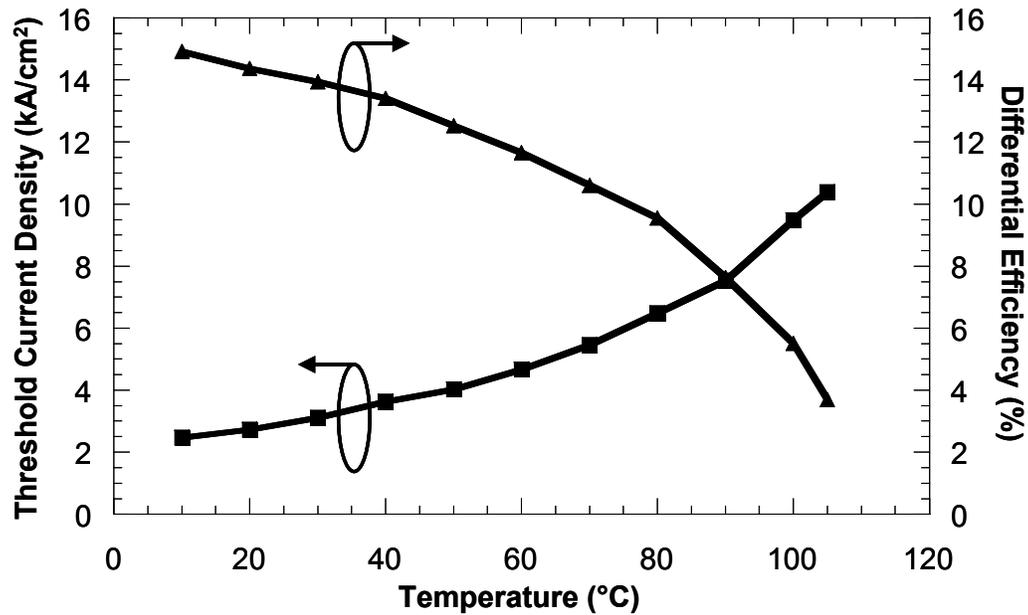


Figure 5.22 CW threshold current density and differential efficiency versus ambient temperature

Threshold current levels were slightly lower (2.5 kA/cm<sup>2</sup> versus 2.8 kA/cm<sup>2</sup> at 20°C) and differential efficiencies slightly higher (15% versus 9% at 20°C) in this generation of devices. This indicates an increase in internal quantum efficiency,  $\eta_i$ , or a reduction of internal loss,  $\alpha_i$ . Long wavelength VCSELs are highly sensitive to absorption in p-type material. The zinc concentration profile in the p-InP cladding is difficult to manage precisely during the growth and bonding

processes. It is possible that the zinc concentration near the quantum well region is lower in this generation of devices, resulting in less optical loss. However, the improved operation is more likely due to an increase in internal quantum efficiency. This may be attributed to reduced device self-heating and a lower internal temperature for a given injection level. Using the values for thermal resistance extracted earlier, the active region temperature for both device generations is plotted below as a function of bias current. This calculation assumes an ambient temperature of 20°C. The rise in temperature is given by the product of the dissipated electrical power and the thermal resistance.

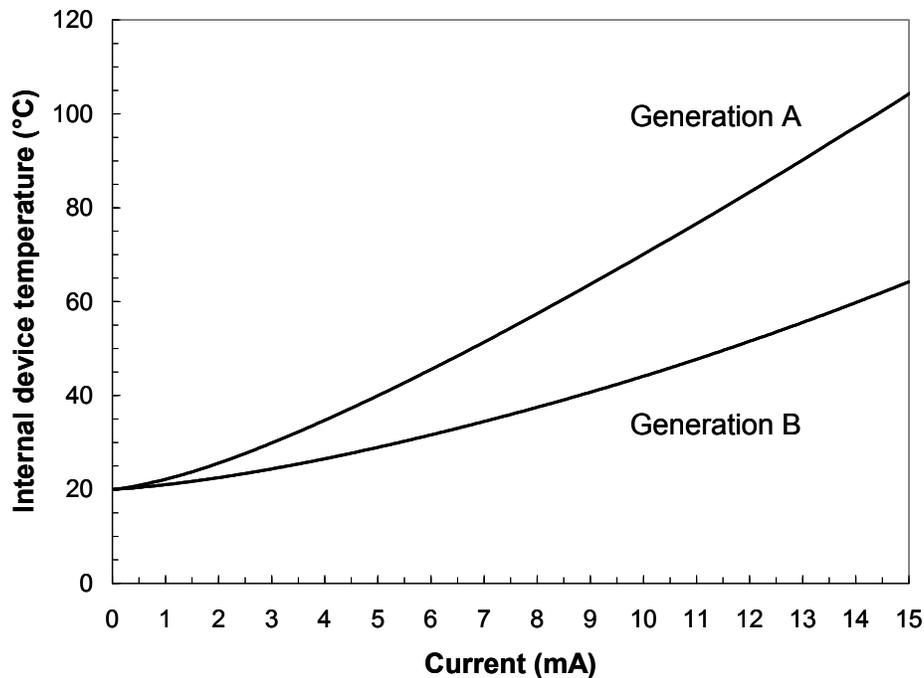
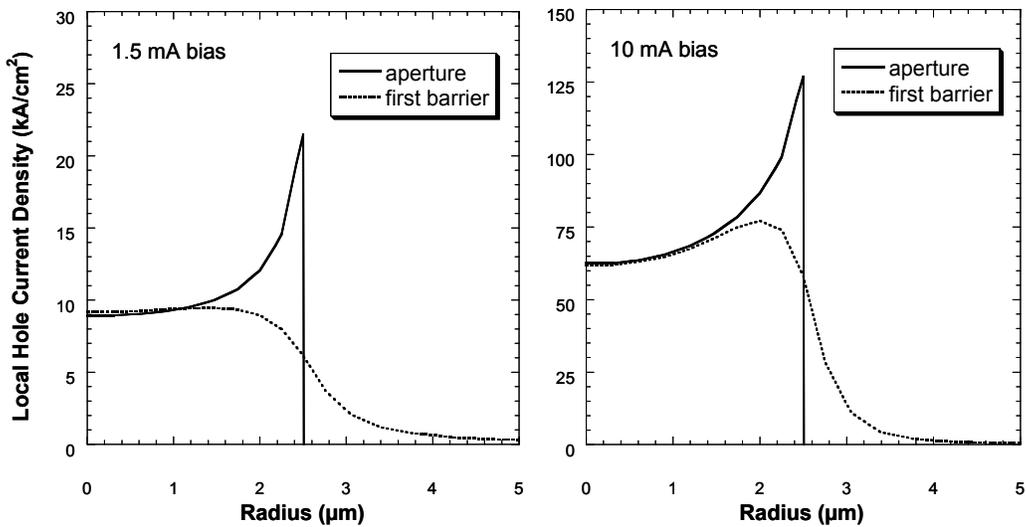


Figure 5.23 Internal device temperature versus bias current for two device generations

This plot reveals the striking difference in device self-heating between the two generations. At a bias current of 1 mA, near threshold, the device temperatures differ by 2°C. This increase has only a minor effect on the material gain and only a small difference in threshold current density is observed. Temperature dependent loss mechanisms remain unaffected at these relatively low temperatures. However, at higher bias currents, Generation B devices operate with a much lower internal temperature. At 10 and 15 mA drive currents, the temperature differences are 26°C and 40°C, respectively. InGaAsP lasers are particularly sensitive to temperature dependent loss and leakage mechanisms, including electron overshoot, Auger recombination and intervalence band absorption. The reduced internal temperature dramatically improves laser performance of Generation B devices relative to those of Generation A. Above threshold, the reduced temperature is responsible for increased internal quantum efficiency, lower internal loss, increased differential efficiency and higher peak powers. The dissipated power could be reduced further by lowering the device resistance. This could be accomplished by using larger pillars, or tunnel junction injection with n-type DBRs.

The effects of current spreading beneath the oxide aperture were analyzed in Section 5.2.4 using an analytically derived formula. These results indicated that

20-40% of the observed threshold current was due to current spreading beneath the aperture, depending on device size. No additional effort was made to reduce current spreading in Generation B devices and similar scaling was observed. Current injection into the VCSEL active region was simulated using a three-dimensional software package to calculate local hole current densities. The current profiles versus radius are plotted in Figures 5.24 and 5.25 for bias currents of 1.5 mA and 10 mA. The oxide aperture radius is taken as 2.5  $\mu\text{m}$ . The hole current profile is calculated at the oxide aperture and at the first barrier in the quantum well active region. The distance from the aperture to the barrier includes 128 nm of p-GaAs, the bonded junction and 310 nm of p-InP. The threshold current is 1.0 mA.



Figures 5.24, 5.25 Local hole current density versus radius at oxide aperture and first barrier for bias currents of 1.5 and 10 mA

The results of this simulation show current crowding at the edges of the oxide aperture for both bias levels. This effect is expected at any current constricting layer. Although the hole current density is leveled between the contact and oxide aperture, the current profile must be compressed in order to pass through the aperture. This leads to higher current densities at the aperture boundary. Integration of the local current density over the radius indicates that 15-20% of the active region current flows outside the aperture dimension. Considering the uncertainty in band offsets and mobility at the bonded junction, this value is in reasonable agreement with the 30-40% current spreading value estimated in Section 5.2.4 for a 5  $\mu\text{m}$  aperture. This effect raises the threshold current from expected values. However, it does not have a significant impact on differential efficiency. The current profile has already spread in reaching threshold and does not change significantly at higher bias levels. This may be inferred from the constant series resistance in the linear portion of the I-V characteristic for a laser diode. For small device sizes, the combination of current spreading and weak index confinement leads to gain guiding rather than index guiding. This effect is apparent in Figure 5.13, where the threshold current does not scale to small sizes in agreement with either ideal or current spreading models. It is believed that the bonded junction is a major contributor to hole current spreading, due to the high turn-on voltage and resistance. The resistive

superlattice barrier in these devices also promotes current spreading. Device efficiency would benefit greatly from an aperture placed in closer proximity to the active region. Although apertures on InP are neither as simple nor as robust as those on GaAs, it may be possible for high-quality apertures to be defined using selective wet etches[8] or the lateral oxidation of aluminum containing compounds[9].

#### *5.3.4. Summary*

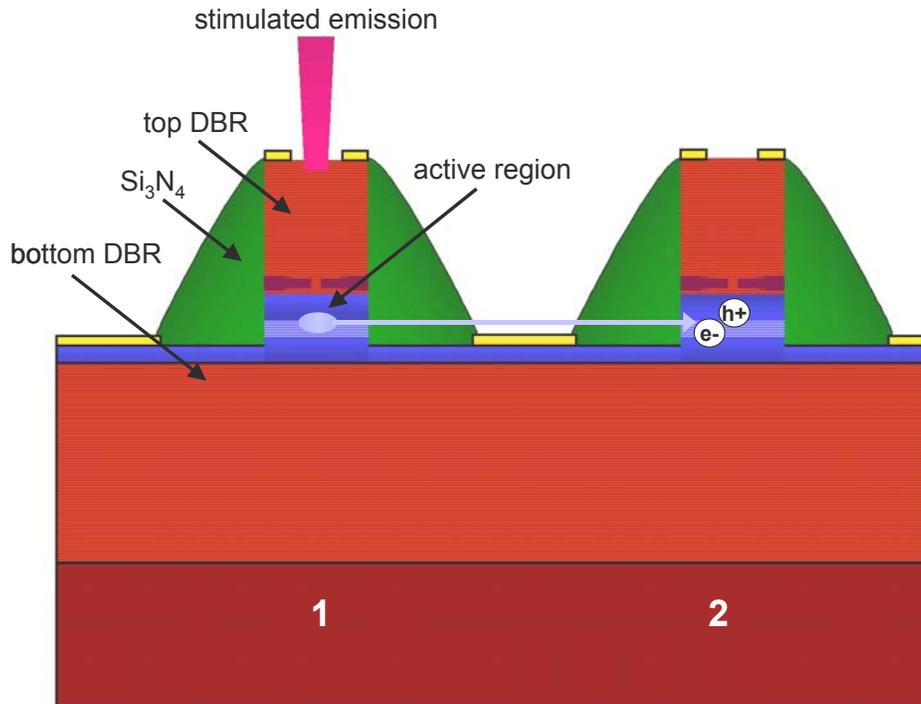
Four-channel WDM VCSEL arrays were fabricated. The wavelength span is 1509.1 nm to 1524.4 nm with a channel spacing of approximately 5 nm. This is the first independently addressable, multiple wavelength 1.55  $\mu\text{m}$  VCSEL array. Threshold currents and other device parameters were similar to those of single-wavelength VCSELs. The maximum CW operating temperature achieved was 105°C. This is the highest CW operating temperature reported for a 1.55  $\mu\text{m}$  VCSEL. The maximum output power at 20°C was 0.65 mW. The maximum output power at 80°C was 0.22 mW. Threshold currents of 0.8 mA were obtained for a 5  $\mu\text{m}$  device. The lowest threshold current density measured was 1.7  $\text{kA}/\text{cm}^2$  for an 11  $\mu\text{m}$  device. The improvement in high-temperature performance relative to Generation A is due to a reduction in p-contact resistance.

## **5.4. Crosstalk**

Integration of multiple wavelength VCSELs on a single substrate enables increased functionality at lower cost. However, the effects of simultaneously operating individual VCSELs must be considered when evaluating array suitability for use in an optical transmission system. The simultaneous operation of array elements creates a situation in which the operating parameters of each VCSEL, including carrier density and temperature, are affected by changes in neighboring VCSELs. In this section, crosstalk between VCSEL array components is considered in detail. Optical and thermal crosstalk mechanisms are discussed and experimental results are used to validate device models. It is observed that the large distance between devices minimizes these forms of crosstalk.

### *5.4.1. Optical crosstalk*

Optical crosstalk in VCSEL arrays has been considered by other authors[10]. For devices on a common substrate, the primary concern is that spontaneous emission from one device may generate carriers in an adjacent device. In effect, this would “pre-bias” the second laser without current injection.



**Figure 5.26 Optical crosstalk between two VCSELs resulting in carrier generation**

It should be noted that this form of crosstalk depends only on spontaneous emission, not stimulated emission. The lasing mode is well-guided by the DBRs and index aperture, resulting in a narrow output beam normal to the substrate. Only spontaneous emission occurs over a broad angular spectrum. A further limitation is imposed by the bandgap energies of the semiconductor materials used to fabricate these long wavelength VCSELs. Spontaneous emission for 1.55  $\mu\text{m}$  diode lasers can be reasonably assumed to occur only at wavelengths greater

than  $1.50 \mu\text{m}$ . This light will not be absorbed by semiconductors with a bandgap energy greater than  $0.83 \text{ eV}$ . The GaAs DBR layers ( $E_g = 1.42 \text{ eV}$ ),  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}$  DBR layers ( $E_g = 2.08 \text{ eV}$ ) and InP cladding ( $E_g = 1.35 \text{ eV}$ ) all have bandgap energies far beyond this cutoff. Consequently, there will be no generation of electron-hole pairs in these areas of the device. Spontaneous emission will only be absorbed in the quantum well active region.

A simple model may be used to estimate the increase in carrier density caused by optical crosstalk. Assume that a certain spontaneous emission power,  $P_s$ , is emitted from the active region of VCSEL 1 in a narrow angular spectrum along the common MQW active region toward VCSEL 2. As discussed earlier, emission in other directions will not result in photo-generated carriers. For the sake of simplicity, it is assumed that no diffraction or scattering takes place as the spontaneous emission propagates toward the active region of VCSEL 2. This propagation path is treated as a waveguide with an effective absorption coefficient of  $\alpha_{12}$ . For the VCSEL structures in this work, this path includes active regions,  $\text{Si}_3\text{N}_4$  passivation layers, and free space. These assumptions clearly overstate the magnitude of the optical crosstalk. However, the purpose of these calculations is merely to estimate and provide an upper bound on the number of carriers generated in VCSEL 2. If the distance between active regions is given by  $L$ , then

the spontaneous emission power arriving at the active region of VCSEL 2 from VCSEL 1,  $P_{21}$  is given by

$$P_{21} = P_s e^{-\alpha_{12}L} \quad \text{Equation 5.4}$$

This arriving power is now partially absorbed by the active region of VCSEL 2. The absorption length in this device is given by  $d$ . The absorption coefficient is written as  $\alpha_{MQW}$ . The spontaneous emission power from VCSEL 1 absorbed in the active region of VCSEL 2 is given by

$$P_{12} = P_s e^{-\alpha_{12}L} (1 - e^{-\alpha_{MQW}D}) \quad \text{Equation 5.5}$$

This absorption generates carriers in the active region of VCSEL 2. Assuming that each absorbed photon generates an electron hole pair, the carrier generation rate is written as

$$\left. \frac{dN}{dt} \right|_{gen} = \frac{P_{12}}{E_p V} \quad \text{Equation 5.6}$$

where  $E_p$  is the photon energy and  $V$  is the active region volume and  $N$  is the carrier density. Assuming that VCSEL 2 is biased below threshold (no stimulated emission) and that there is no coupling between the electron and photon densities in VCSEL 2, the carrier recombination rate is given by

$$\left. \frac{dN}{dt} \right|_{rec} = \frac{N}{\tau} \quad \text{Equation 5.7}$$

where  $\tau$  is the carrier lifetime. Under steady-state condition, the generation and recombination rates are equal. The steady-state carrier density in the active region of VCSEL 2 is

$$N = \frac{P_{12}\tau}{E_p V} \quad \text{Equation 5.8}$$

Reasonable values for  $\tau$ ,  $E_p$  and  $V$  are 1 ns, 0.8 eV, and  $7.85 \mu\text{m}^3$ . The active region volume is calculated using a thickness of  $0.1 \mu\text{m}$  and a radius of  $5 \mu\text{m}$ . The photon energy given corresponds to an emission wavelength of  $1.55 \mu\text{m}$ .  $P_{12}$  may also be estimated by inserting device parameters. The active region radius of  $5 \mu\text{m}$  corresponds to an absorption length,  $D$ , of  $10 \mu\text{m}$  with an absorption coefficient,  $\alpha_{MQW}$ , of  $50 \text{cm}^{-1}$ . The distance between active regions,  $L$ , is  $250 \mu\text{m}$ . The majority of this distance is in air and may be considered lossless.

The silicon nitride layer also has a negligible loss coefficient. The only loss between devices is between the active region centers and the device sidewall. Assuming a pillar diameter of 50  $\mu\text{m}$ , this distance is 40  $\mu\text{m}$  for two devices and has a loss coefficient of 50  $\text{cm}^{-1}$ . Based on off-axis detection of the spontaneous emission power, a maximum value of 0.1 mW is assumed for  $P_s$ . Since this value was estimated using a broad-area detector, the estimate may be as much as an order of magnitude higher than the actual value. However, it should still be useful in estimating an upper bound for the induced carrier density in VCSEL 2. The parameters used to calculate the carrier density are summarized in Table 5.3.

Parameter	Value
$P_s$	0.1 mW
$\alpha_{12}$	50 $\text{cm}^{-1}$
L	40 $\mu\text{m}$
$\alpha_{\text{MQW}}$	50 $\text{cm}^{-1}$
D	10 $\mu\text{m}$
$E_p$	0.8 eV
V	7.85 $\mu\text{m}^3$
$\tau$	1 ns

**Table 5.3** Parameters and values used in optical crosstalk calculations

Using the values given above, it is determined that  $P_{12} = 3.99 \mu\text{W}$  and that  $N = 3.97 \times 10^{16} \text{ cm}^{-3}$ . This carrier density value may be used to extract an equivalent injected current density. For electrical injection below threshold, the carrier density may be written as

$$N = \frac{\eta_i J \tau}{qd} \quad \text{Equation 5.9}$$

where  $\eta_i$  is the internal quantum efficiency,  $J$  is the terminal current density,  $\tau$  is the carrier lifetime,  $q$  is the fundamental electronic charge and  $d$  is the active region thickness. Rewriting this expression in terms of  $J$ , the terminal current density is given by

$$J = \frac{Nqd}{\eta_i \tau} \quad \text{Equation 5.10}$$

The active region thickness,  $d$ , is  $0.1 \mu\text{m}$  and the internal quantum efficiency is approximately 0.8. The calculated carrier density induced in VCSEL 2 by spontaneous emission from VCSEL 1 is equivalent to an injection current density of  $0.079 \text{ kA/cm}^2$ . This is approximately 0.4% of the broad area threshold current density of  $1.9 \text{ kA/cm}^2$ . Despite the large value used for  $P_s$ , the calculated equivalent crosstalk current density barely exceeds measurement resolution. In

practice, the crosstalk power is much lower than this calculated value due to the exceptionally narrow angular spectrum of spontaneous emission that can produce carriers in adjacent devices. Diffraction, reflection and scattering losses are also significant along the crosstalk propagation path. No meaningful difference in threshold current was measured under pulsed operation between devices operated individually and devices operated with their nearest neighbor biased above threshold. The low optical crosstalk is attributed to wide pillar diameters, oxide-confined active regions and low spontaneous emission photon energy. This value could be reduced even further by depositing an absorptive film between devices and by improving the active region carrier clamping efficiency above threshold. However, no process improvements are required unless the device spacing is dramatically reduced.

#### *5.4.2. Thermal Crosstalk*

In sections 5.2 and 5.3, the mechanism and effects of device self-heating were considered. This treatment is appropriate when considering the operation of an individual device. However, the thermal effects of multiple device operation become relevant when discussing array operation. In long wavelength VCSEL arrays, thermal crosstalk is even more significant due to the temperature sensitivity of the active region.

In order to gauge the magnitude of temperature rise, the array temperature profile caused by operation of a single VCSEL was simulated using ANSYS finite element software. The VCSEL structure was approximated by a 10  $\mu\text{m}$  square heat source at 100°C on a GaAs/AlAs DBR and GaAs substrate. These are reasonable assumption as nearly all of the generated heat is dissipated through the bottom DBR to the substrate and heat sink. A two-dimensional map temperature distribution relative to the heat sink temperature is plotted in Figure 5.27.

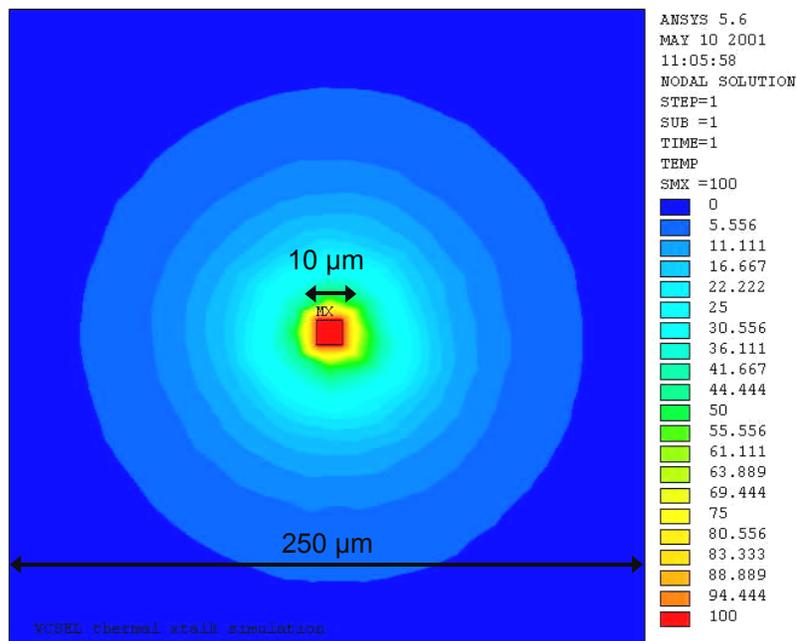


Figure 5.27 Two-dimensional map of VCSEL temperature distribution

The simulation indicates that the temperature rise caused by VCSEL operation is confined to a small area. At a distance of 250  $\mu\text{m}$ , equal to the device pitch, the temperature rise is only 0.5°C. Simulation results were tested experimentally by biasing the laser above threshold and using a thermal microprobe to measure surface temperature at different distances from the heat source. These experimental results are plotted in Figure 5.28, along with a one-dimensional profile of the map in Figure 5.27.

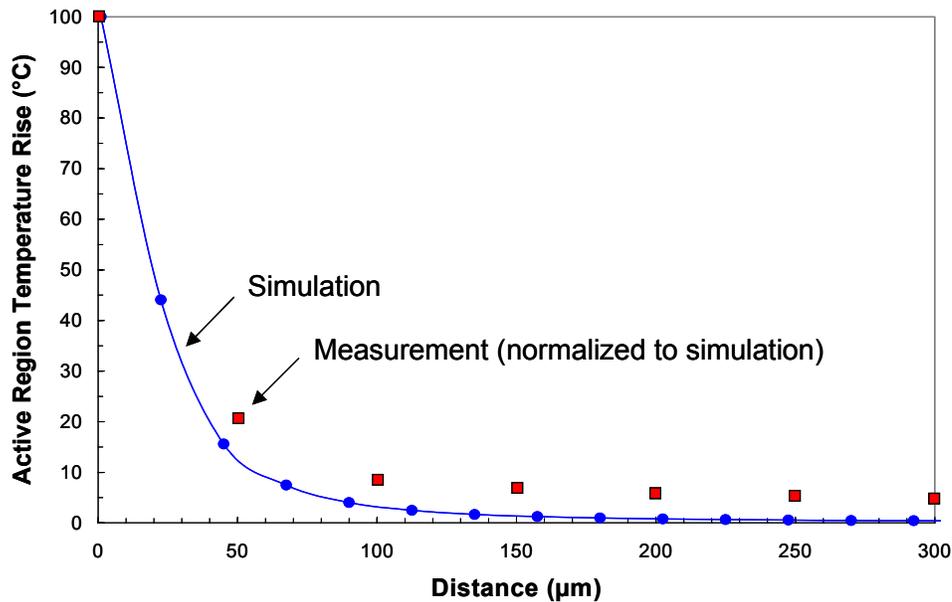


Figure 5.28 Comparison of thermal simulation and microprobe measurements

The two curves agree remarkably well. The difference in saturation temperature is due to the difference in heat sink conditions between theory and

experiment. In the simulation, an ideal heat sink was assumed. In practice, the heat sink under the substrate had finite thermal conductivity. The saturation value is also affected by pillar diameter, not included in the simulation.

The thermal crosstalk between array elements is measured by operating VCSEL 1 at a fixed current and voltage while varying the electrical power dissipated by VCSEL 2. The thermal isolation between VCSELs 1 and 2 is defined as[11]:

$$Z_{12} = \frac{\Delta P_2}{\Delta T_1} \quad \text{Equation 5.11}$$

where  $\Delta P_2$  is the change in dissipated power of VCSEL 2 and  $\Delta T_1$  is the corresponding change in temperature of VCSEL 1. The temperature of VCSEL 1 is monitored by observing the lasing wavelength as described in section 5.2. This local temperature rise is used to calculate the effective thermal conductivity,  $\sigma_{th}$ , between adjacent devices. The temperature rise,  $\Delta T$ , caused by a heat fluctuation,  $\Delta P$ , at a distance,  $r$ , in a semi-infinite medium is given by:

$$\Delta P = \frac{\Delta T}{2\pi\sigma_{th}r} \quad \text{Equation 5.12}$$

Equations 5.11 and 5.12 may be combined to yield:

$$Z_{12} = \frac{\Delta P_2}{\Delta T_1} = 2\pi\sigma_{th}r \quad \text{Equation 5.13}$$

This expression can be used to describe the thermal isolation between two array elements with indices  $i$  and  $j$ .

$$Z_{ij} = \frac{\Delta P_j}{\Delta T_i} \quad \text{Equation 5.14}$$

An optical spectrum analyzer was used to measure the wavelength of one VCSEL while dissipating 10 mW of electrical power in devices at a distance of 250-1000  $\mu\text{m}$ . Due to the small temperature rises, it was difficult to resolve changes in lasing wavelength. The measurements would benefit from the use of a wavelength meter rather than an optical spectrum analyzer. Results are shown in Figure 5.29, along with error bars that include the range of calculated temperature rises. Although it is not possible to quote a precise value for thermal isolation, it can be said with confidence that  $Z_{12} > 28 \text{ mW}/^\circ\text{C}$  and that  $Z_{1j} > 40 \text{ mW}/^\circ\text{C}$ . Using this value of  $Z_{12}$  in Equation 5.13 yields a lateral thermal conductivity between devices of 0.18 W/cm K. This low value is due to the high transverse thermal conductivity of the GaAs/AlAs DBR, the high thermal conductivity of the underlying GaAs substrate and the pillar etch that forces heat to flow through the

bottom DBR before reaching an adjacent device. The saturation value of thermal isolation depends heavily on the mounting conditions and could be improved further by etching trenches between devices.

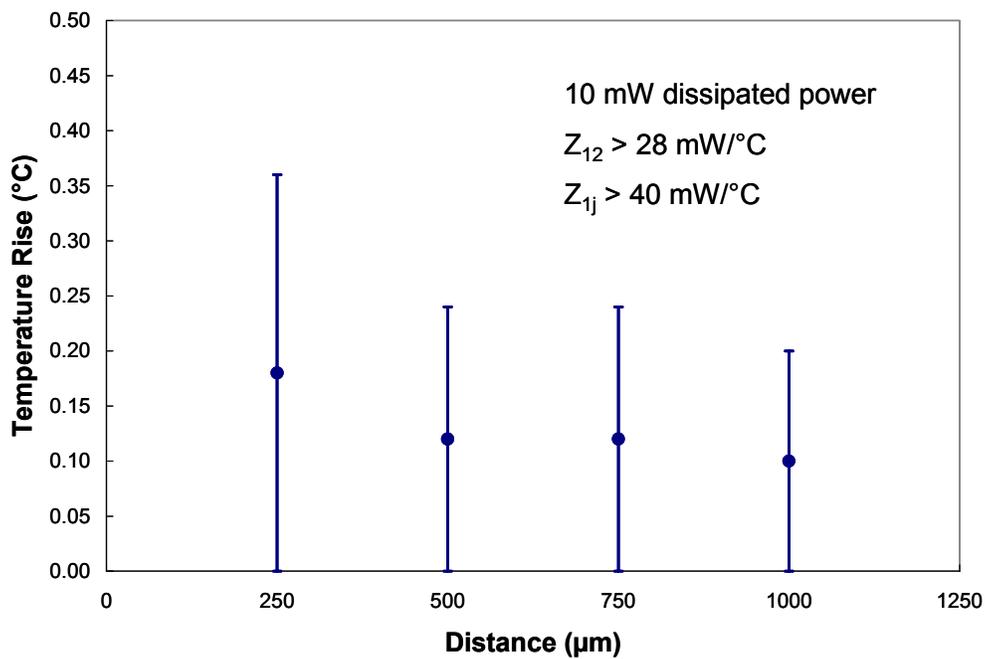


Figure 5.29 Temperature rise in VCSEL caused by 10 mW of dissipated power at varying distances

The effective thermal resistance may be considered in more detail by expanding on Equation 5.14. For simplicity of notation, the thermal resistance of an individual element in an array is denoted by  $1/Z_{ii}$ . It is assumed that all array elements operate at the same time and dissipate the same amount of power.

Therefore, the effective thermal resistance of element  $i$  in an array,  $R_i$ , in an  $N$  element array is given by:

$$R_i = \frac{1}{Z_{i1}} + \frac{1}{Z_{i2}} + \frac{1}{Z_{i3}} \dots = \sum_{j=1}^N \frac{1}{Z_{ij}} \quad \text{Equation 5.15}$$

This form of the expression relates  $R_i$  to  $\Delta T_i$ . An alternative, but equally valid formulation would relate  $R_i$  to  $\Delta P_i$ . Equation 5.14 may be extended to all array elements by re-writing it in matrix form. Equation 5.16 expresses the temperature rise for each element of the array in terms of the thermal isolation between elements and the power dissipated by each element.

$$\begin{bmatrix} \Delta T_1 \\ \Delta T_2 \\ \vdots \\ \Delta T_N \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_{11}} & \frac{1}{Z_{12}} & \dots & \frac{1}{Z_{1N}} \\ \frac{1}{Z_{21}} & \frac{1}{Z_{22}} & \dots & \frac{1}{Z_{2N}} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{1}{Z_{N1}} & \frac{1}{Z_{N2}} & \dots & \frac{1}{Z_{NN}} \end{bmatrix} \begin{bmatrix} \Delta P_1 \\ \Delta P_2 \\ \vdots \\ \Delta P_N \end{bmatrix} \quad \text{Equation 5.16}$$

It is apparent from Equations 5.15 and 5.16 that heat flow from neighboring devices increases the effective thermal resistance of individual lasers in the array. In the case of an isolated 1 x N array, center elements will experience a greater increase in temperature than the end elements for a given power

dissipation by each device. This effect is plotted in Figure 5.30, using 410 K/W as the individual VCSEL thermal resistance, as calculated in section 5.2

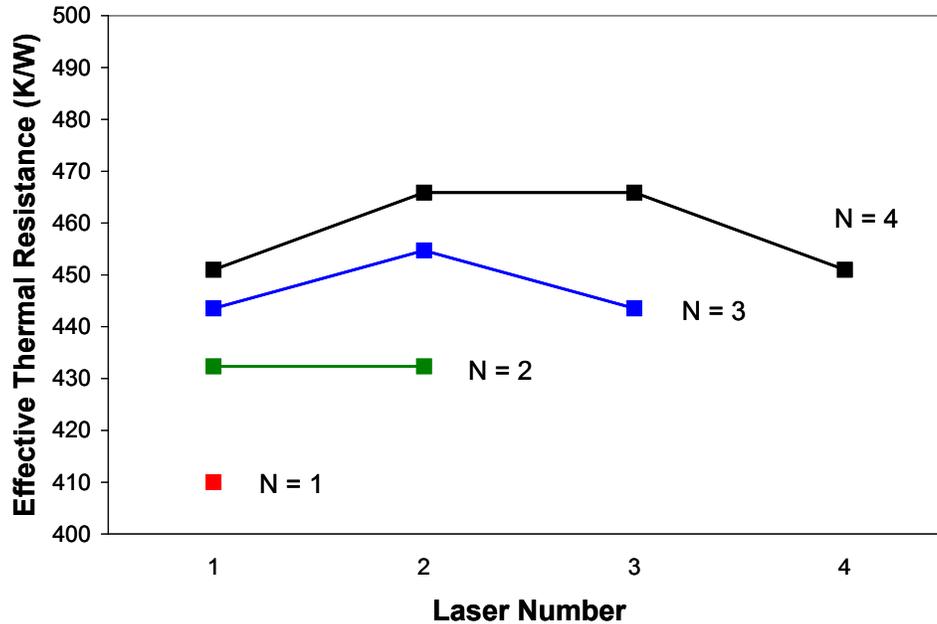


Figure 5.30 Effective thermal resistance for devices in 1 x N array, N = 1-4

The effective thermal resistance of a central element in a 1 x 4 array is 13% higher than that of an edge element. The increase would be even larger if not for the large device spacing and high transverse thermal conductivity of the GaAs/AlAs DBR. Although the effects of thermal crosstalk are not significant for this array, they could be further mitigated by improved heat sinking. Increasing the thermal isolation by etching a trench between devices would also reduce crosstalk.

## **5.5. Summary**

In this chapter, the results from two generations of wafer-bonded VCSELs were presented. The first generation of single wavelength devices was limited by high operating voltage. However, these devices were still capable of continuous-wave operation at ambient temperatures up to 85°C and threshold currents as low as 0.9 mA. The second generation of devices was fabricated using the same epitaxial material, but patterned in multiple-wavelength arrays. Due to reduced voltage, these devices lased under continuous-wave operation up to 105°C. This is the highest operating temperature reported for an electrically pumped 1.55  $\mu\text{m}$  VCSEL. The measured wavelength spacing was approximately 5 nm, consistent with expectations. This is the first demonstration of an electrically pumped, independently modulated multiple-wavelength VCSEL array at 1.55  $\mu\text{m}$ . Threshold currents were as low as 0.8 mA for a 5  $\mu\text{m}$  device. The highest output power measured was 0.65 mW. Current spreading was identified as a mechanism limiting low threshold operation. It is expected that device performance could be further improved with optimized aperture placement, lowered series resistance and reduced absorption losses in p-type material. Optical and thermal crosstalk

were analyzed. These effects are minimized by to the high thermal conductivity of the GaAs-based DBRs and the large distance between devices.

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## **6. Conclusions and Future Work**

### **6.1. Summary of Thesis**

The results presented in this dissertation represent significant achievement in the areas of wafer bonding and vertical cavity laser fabrication. The novel wafer bonding techniques developed were used to create high-performance vertical cavity lasers and enable a new class of multiple wavelength VCSEL arrays.

#### *6.1.1. Wafer bonding*

A superlattice barrier was used as a buffer layer during GaAs:InP bonding to reduce the number of non-radiative recombination centers propagating to the InP active region. The photoluminescence intensity from bonded active regions with the superlattice barrier is greater than that from bonded active regions without the superlattice barrier. This layer was incorporated into subsequent device structures.

The same superlattice barrier was patterned prior to bonding in order to define multiple wavelength VCSEL cavities. By selectively wet etching superlattice periods on a specific pitch, the cavity length may be tuned across the

wafer surface. Significantly, this technique allows wavelengths to be repeated as desired, rather than as one continuous grade. This intracavity tuning layer was used to fabricate multiple wavelength VCSEL arrays.

*6.1.2. 1.55  $\mu\text{m}$  vertical cavity lasers*

Continuous-wave operation was achieved at temperatures up to 105°C. This is the highest reported lasing temperature for a 1.55  $\mu\text{m}$  VCSEL. The wafer bonding technique facilitated the integration of highly reflective, thermally conductive GaAs/AlGaAs DBRs with InP/InGaAsP active regions. Threshold currents as low as 0.8 mA were measured for devices with a 5  $\mu\text{m}$  oxide aperture. The peak output power at 20°C was 0.65 mW. The peak output power at 80°C was 0.22 mW. Threshold current densities of 1.7 kA/cm<sup>2</sup> were measured for an 11  $\mu\text{m}$  device. Single-mode operation with a side-mode suppression ratio in excess of 40 dB was observed for a 5  $\mu\text{m}$  device. The improved device performance relative to previous generations is attributed to fewer non-radiative recombination centers in the bonded active region, lower operating voltages and reduced optical loss in the p-DBR.

*6.1.3. Multiple wavelength VCSEL arrays*

Four-channel WDM VCSEL arrays were fabricated. The wavelength span was 1509.1-1524.4 nm with channel spacing of approximately 5 nm. This is the first demonstration of an independently addressable, multiple-wavelength VCSEL array at 1.55  $\mu\text{m}$ . Threshold currents of 1.0 mA and peak output powers of 0.5 mW were measured. Thermal and optical crosstalk were negligible, due to high thermal conductivity in the vertical direction and 250  $\mu\text{m}$  device spacing.

**6.2. Future Work**

High temperature performance could be further improved by introducing new active region materials. Current spreading could be reduced by using a lithographically defined aperture on the InP side of the bonded junction. This aperture could also confine the optical mode. Tunnel junction injection would reduce device resistance and absorption loss due to high electron mobility and reduced absorption loss in n-type material. Closer channel spacing may be achieved with thinner tuning layers or through a combination of coarse and fine tuning mechanisms.

6.2.1. *AllnGaAs active region*

The traditional InGaAsP material system for long wavelength lasers is plagued by Auger recombination and poor electron confinement. Strained active regions have been introduced to reduce threshold current and increase differential gain, but the problem of poor high temperature performance remains. Most laser transmitters based on InGaAsP material require thermoelectric cooling in order to satisfy performance standards over the desired temperature range. In order to maintain a cost advantage over edge-emitting lasers, it is desirable for VCSELs to operate without a thermoelectric cooler. An alternative active region material is AllnGaAs. The conduction band offset in AllnGaAs ( $\Delta E_c = 0.72 \Delta E_g$ ) is significantly larger than in InGaAsP ( $\Delta E_c = 0.40 \Delta E_g$ ). Using AllnGaAs as an active region material can provide stronger electron confinement and reduced temperature sensitivity. The suitability of this material system for high-performance uncooled lasers has been studied extensively[1], but not yet applied to wafer bonded VCSELs at UCSB. Even without other design improvements, replacing the current InGaAsP active region with AllnGaAs should result in improved high-temperature operation.

### 6.2.2. Current confinement

In this work, it was calculated that 30% of the injected current was lost due to current spreading beneath the aperture. Although the oxide aperture does provide some current confinement, the bonded junction and low doping in the p-InP cladding cause significant spreading between the aperture and active region. At this time, a robust aperturing technology on InP similar to the lateral oxidation of AlGaAs on GaAs does not exist. A large device is desirable for low electrical and thermal resistance. A well-positioned aperture is required for low threshold current and high output power. It is proposed that a current confining aperture be defined in the InP cladding. Ion implantation can be used to selectively disorder the cladding and obtain lateral current confinement. Implantation prior to bonding allows the use of shallow implant depths and angles, reducing process complexity.

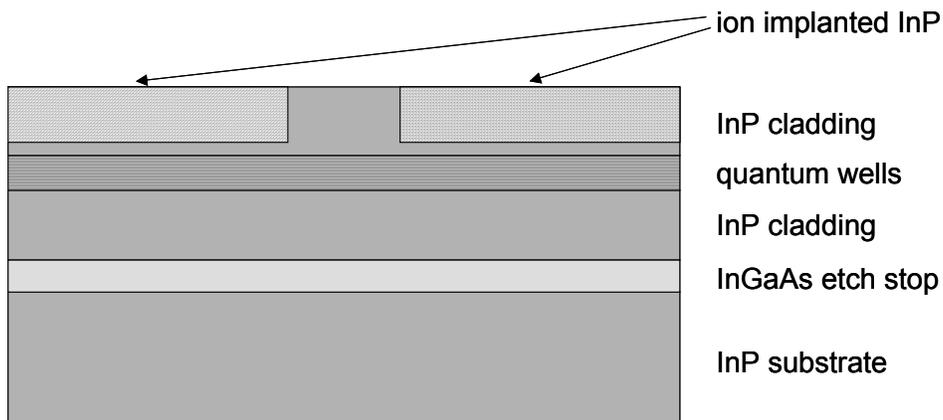


Figure 6.1 Ion implantation for InP current confinement

This technique yields a lithographically defined aperture that constricts current on the InP side of the bonded interface. Iron is suggested as an implant species due to the semi-insulating behavior of Fe:InP. The remaining process steps are identical to those discussed in Chapter 4, including lateral oxidation for mode confinement. The processed structure is shown below in Figure 6.2.

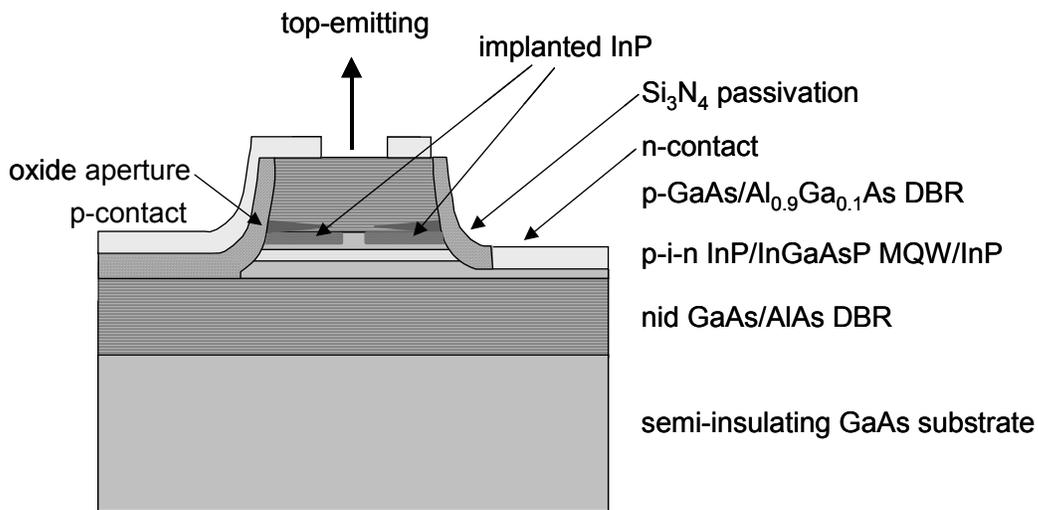


Figure 6.2 VCSEL device structure with ion implant in InP cladding

Ion implantation should not degrade the InP surface to an extent that prevents bonding. However, implantation could cause excessive damage to the quantum well region. An alternative current confining aperture could be defined by patterning a shallow mesa structure in the InP cladding prior to bonding, as

shown in Figure 6.3. This could be accomplished with selective wet etches of superlattice periods or an InP etch such as  $\text{H}_3\text{PO}_4:\text{HCl}$ .

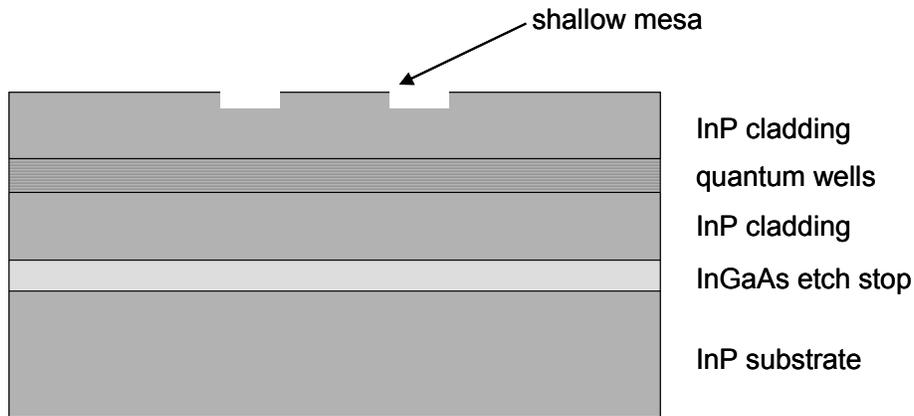
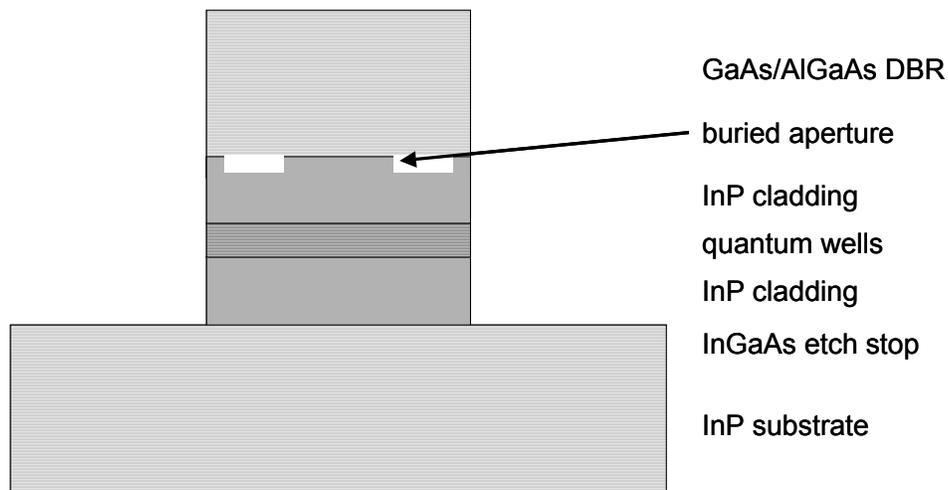


Figure 6.3 Etched mesa in InP cladding

A mesa depth of 1000-2000 Å should provide sufficient depth so that the mesa remains intact during the bonding process. This would result in a lateral InP:air interface, mechanically supported by unetched InP, as shown in Figure 6.4. This aperture dimension is also lithographically defined. Although some spreading into the support region is possible, current spreading should still be reduced compared to a device with no confinement on the InP side of the bonded junction. The mesa depth determines the aperture location and nature of the index perturbation. The index difference ( $n_{\text{InP}} = 3.17$ ,  $n_{\text{air}} = 1.00$  at 1550 nm) should provide proper modal confinement in a well-designed cavity. This technique

would provide modal and current confinement without implantation or oxidation. The active region would not be exposed to implant damage, thermal effects, or lateral etching.



**Figure 6.4 Buried aperture on InP side of bonded junction**

### 6.2.3. Tunnel junction injection

High contact resistance, low hole mobility, and high absorption loss in p-type material limit the performance of traditional p-i-n diodes in VCSEL structures. Tunnel junctions allow the use of two n-type DBRs and only a single thin layer of p-type material is needed in the entire structure. It should be noted that tunnel junction injection is compatible with either of the aperturing techniques discussed in Section 6.2.2. A tunnel junction aperture and current

blocking layer can be formed by taking advantage of mass transport at the bonded junction. Consider an InP-based active region with a tunnel junction in the top cladding. The tunnel junction may be etched away in the region where current blocking is desired.

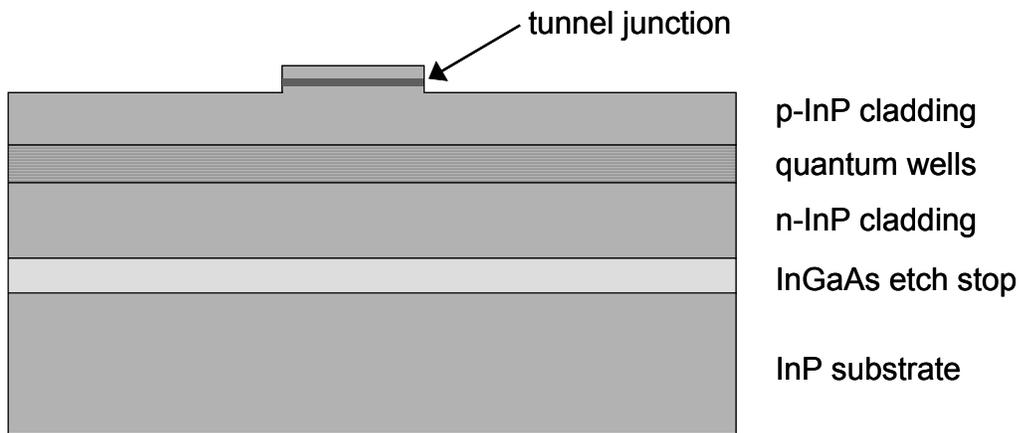
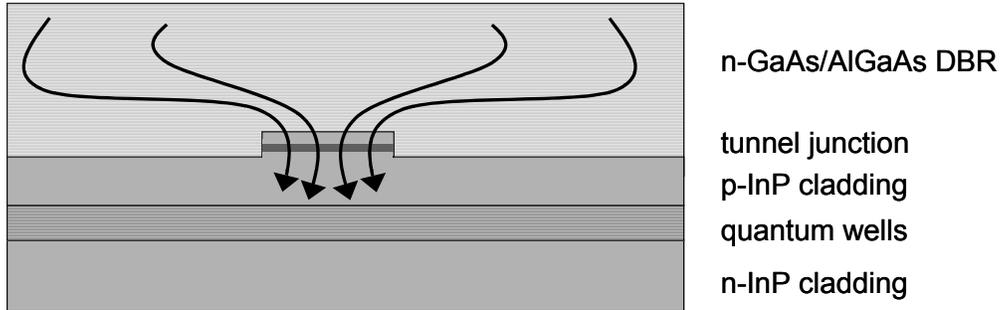


Figure 6.5 Patterned active region with tunnel junction

Based on the non-planar bonding work performed during the course of this research, it is expected that a shallow mesa of 200-500 Å in depth could be accommodated by mass transport during the bonding process. If an n-type GaAs/AlGaAs DBR is bonded to this surface, the p-InP cladding will block current flow outside the tunnel junction. Electrons injected across the bonded junction into the tunnel junction will produce holes in the quantum well region.



**Figure 6.6 Tunnel junction active region with n-type DBR and current blocking layer**

It may be possible to use the bonded junction itself as the n-type layer in a tunnel junction. Capacitance-voltage measurements and simulations have indicated a donor charge density in excess of  $10^{14} \text{ cm}^{-2}$  at the bonded interface. This structure should also provide lateral optical confinement due to the index difference between the tunnel junction material and  $\text{Al}_x\text{Ga}_{1-x}\text{As}$ .

There are numerous advantages to tunnel junction injection. The voltage drop across the p-InP:p-GaAs bonded junction is replaced with ohmic transport across n-InP:n-GaAs. This will reduce the operating voltage and series resistance of the device. The VCSEL can now have two n-type DBRs or one n-type and one undoped DBR. This further decreases electrical resistance and also reduces absorption loss. Device performance will improve dramatically provided that a suitable current confinement scheme is implemented.

#### 6.2.4. Wavelength division multiplexing

Coarsely spaced WDM channels are desired for 10 Gigabit Ethernet (10GbE) and other low-cost optical networks. In this work, four-channel VCSEL arrays with a wavelength spacing of 5 nm were fabricated. For certain applications, a higher number of more closely spaced wavelengths may be desired. It is possible that the superlattice tuning mechanism discussed in Chapter 3 may be extended to 8 or possibly 16 channel operation by using thinner tuning layers. However, it is unlikely that the wavelength spacing can be reduced to less than 2 nm. Lateral oxidation techniques have been used to define multiple wavelength cavities with smaller channel spacing but also a smaller wavelength span. These methods including tapered oxidation[2], anodic oxidation and regrowth[3], and variation of oxidation depth[4]. The combination of coarse vertical and fine lateral tuning mechanisms should allow for the fabrication of two-dimensional arrays with wide wavelength spans and narrow wavelength spacing. Any of the lateral tuning techniques mentioned above may prove suitable as a fine tuning mechanism. However, the lateral cavity size effect is of particular interest since it requires neither regrowth nor long oxidations. It may also be applied to the buried tunnel junction aperture discussed in Section 6.2.3. The lateral size of the lasing mode defines a transverse wavevector that determines the quasimode wavelength. If the normal component of the wave vector is  $k_z = 2\pi/\lambda_0$

and the radial component of the wavevector has magnitude  $\pi^2/w_n^2$ , where  $w_n$  is the transverse mode size of the  $n$ th array element, the lasing wavelength  $\lambda_n$  is given by[4]

$$\lambda_n = \frac{\lambda_0}{\sqrt{1 + \frac{\lambda_0^2}{4w_n^2}}} \quad \text{Equation 6.1}$$

For 1.55  $\mu\text{m}$  emission, it should be possible to tune the cavity wavelength with a precision of 0.5 nm with a 0.5-1.0  $\mu\text{m}$  shift in transverse mode size. The buried tunnel junction discussed earlier has the additional advantage of being lithographically defined, which would enable the transverse mode control necessary for such fine wavelength tuning. The effect of a change in transverse mode size on laser uniformity must be considered. It may be possible for the non-uniformities introduced by the mode size shift to be compensated elsewhere in a well-designed cavity. Tapered oxidation and regrowth approaches for fine tuning are more complicated, but do not require as sophisticated a handling of the transverse mode profile. A schematic of a two-dimensional, multiple wavelength VCSEL array is shown below. Vertical tuning is used to provide a coarse wavelength shift along one axis. Lateral tuning is used to provide a fine wavelength shift along the other.

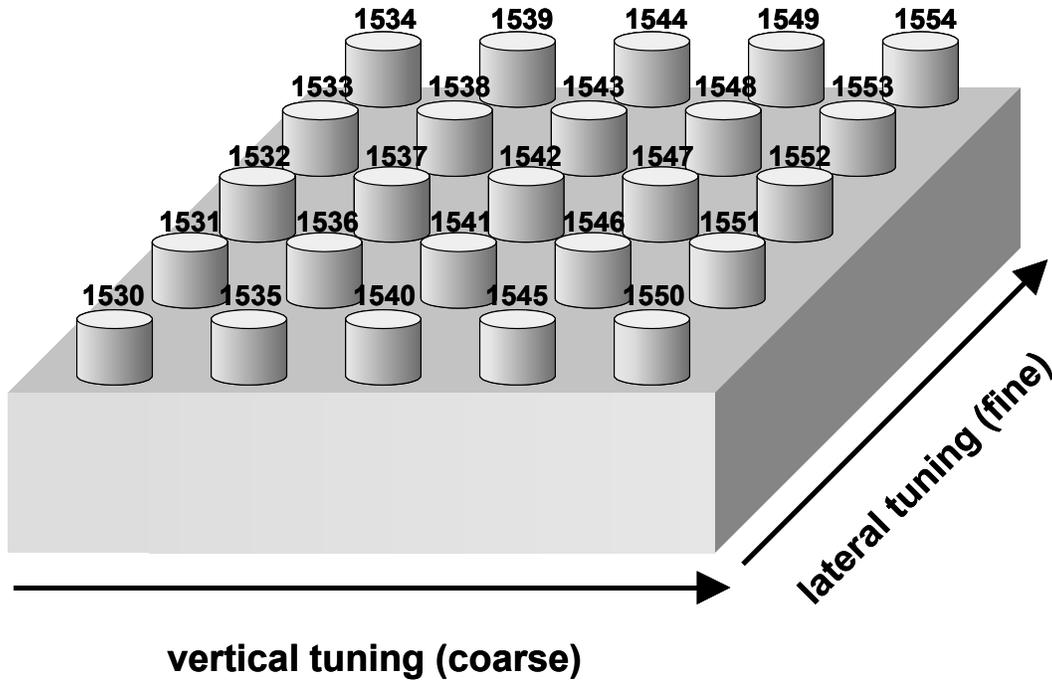


Figure 6.7 Two-dimensional WDM VCSEL array, with vertical tuning along one axis and lateral tuning along the other. Vertical tuning is a coarse spacing mechanism to increase wavelength span. Lateral tuning is a fine spacing mechanism to reduce channel spacing. The lasing wavelength in nm is shown above each device.

### 6.3. Conclusion

Wafer bonding has been used to create a new class of vertical cavity laser array, capable of multiple wavelength transmission in the 1.55  $\mu\text{m}$  wavelength band. These devices exhibit superior performance with continuous-wave operation up to 105°C and threshold currents as low as 0.8 mA. Applications such as local area networks (LANs), metropolitan area networks (MANs), and fiber to the home (FTTH) demand low cost, high performance sources. Long wavelength

vertical cavity lasers will be the components that enable this next generation of fiber optic networks.

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