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Silicon Microcoolers

A Dissertation submitted in partial satisfaction of the
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in

Electrical and Computer Engineering

by

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March 2002

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ABSTRACT

Silicon microcoolers

by

Xiaofeng Fan

There has been an increasing demand for localized cooling and temperature stabilization of microelectronic and optoelectronic devices. Monolithically integrated solid-state microcoolers are an attractive way to achieve compact localized cooling. SiGe is an important microelectronic material and also a good thermoelectric material for high temperature applications. SiGe and SiGe/Si superlattices were grown with molecular beam epitaxy (MBE) on silicon substrates. The superlattice structures are used for enhance thermoelectric cooling by thermal conductivity reduction and thermionic emission. SiGe/Si microcoolers were fabricated with standard integrated circuit (IC) processing. Both n- and p-type microcoolers were demonstrated, which paved the road to fabricate n- and p-type coolers in an array format electrically in series and thermally in parallel to achieve large cooling capacities with relatively small currents. The microcoolers ranged in size from 10×10 μm^2 to 150×150 μm^2, and a maximum cooling of 4.3K and 13.8 K was measured at

heat sink temperature of 25°C and 250 °C respectively. SiGe has a larger lattice constant than Si, and a buffer layer is needed to grow thick SiGe and SiGe/Si superlattice on Si. To improve this, carbon can be added to SiGe to reduce its lattice constant. Lattice matched SiGeC/Si microcoolers were demonstrated. Maximum cooling power densities on the order of hundreds of W/cm^2 were measured for both SiGe/Si and SiGeC/Si microcoolers.

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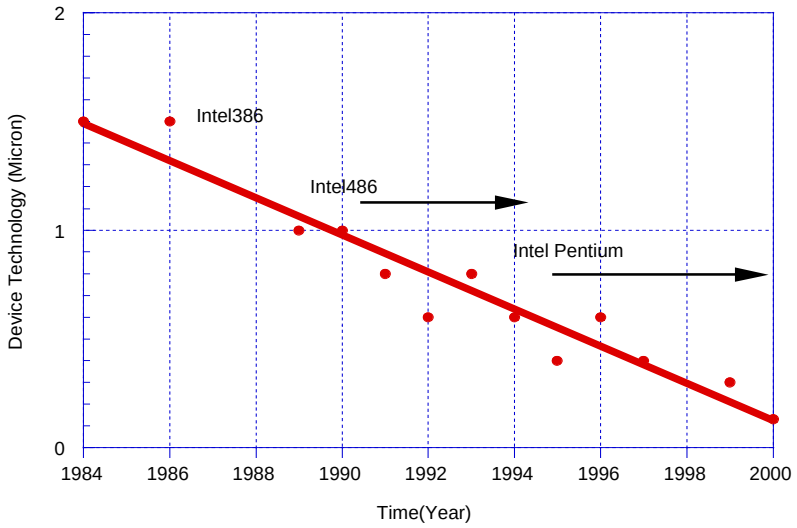
Chapter 1

Introduction

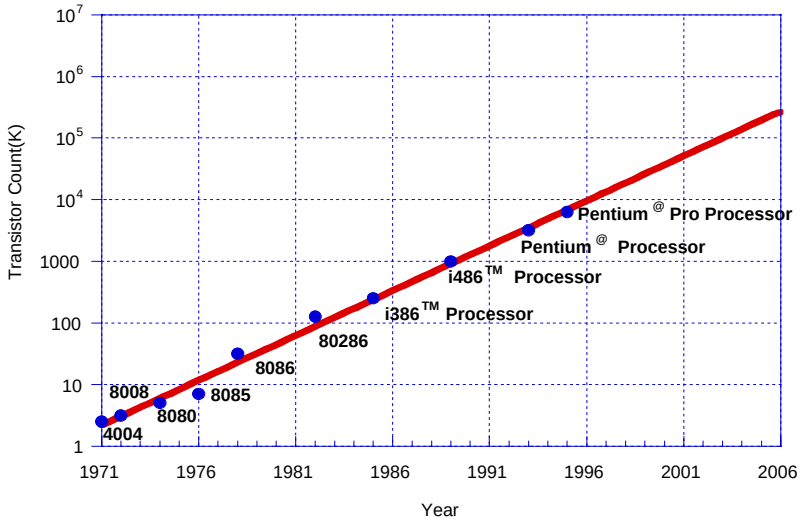
1.1 *Thermal management of microelectronics*

With the rapid development of the very-large-scale-integration (VLSI) and ultra-large-scale-integration (ULSI) technology, the minimum device size has gone into the deep sub-micron region and continues to shrink towards nano-technology. The number of components per integrated circuit (IC) chip is increasing at a very fast speed [1]. In the 1970s, Dr. Gordon Moore predicted that semiconductor transistor density, and hence performance, would double roughly every 18 months, which is referred as Moore's law. The microprocessor industry has followed Moore's law very well. Figure 1.1 shows the technology timeline for Intel corporation microprocessors. The smaller feature size and higher transistor density make the microelectronics faster and more functional, while at the same time they also come with higher power, as shown in Figure 1.1 (c).

(a)


Device Technology (Micron)
Time(Year)
Intel386
Intel486
Intel Pentium
2
1
0
1984
1986
1988
1990
1992
1994
1996
1998
2000

(b)


Transistor Count(K)
Year
10^7
10^6
10^5
10^4
1000
100
10
1
1971
1976
1981
1986
1991
1996
2001
2006
Pentium @ Pro Processor
Pentium @ Processor
i486™ Processor
i386™ Processor
80286
8086
8085
8008
8080
4004

(c)

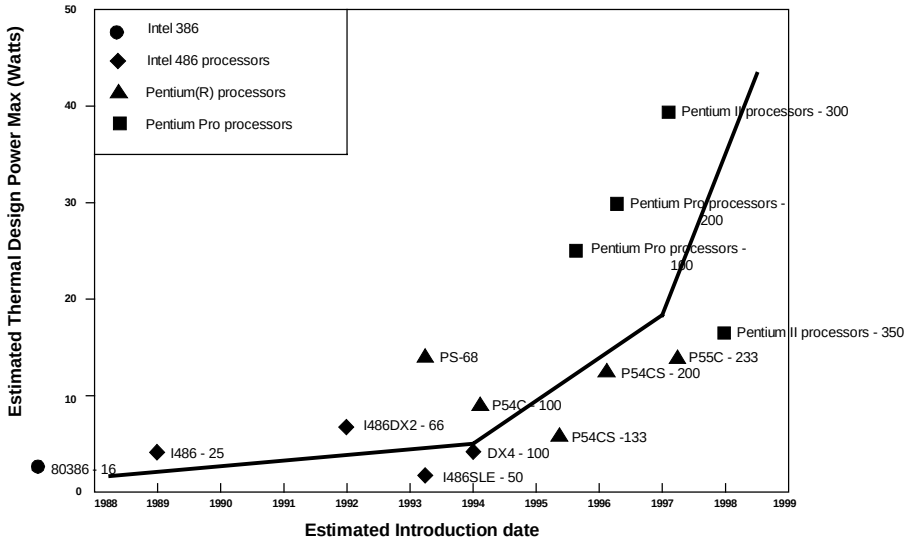


Figure 1.1 Timeline of device technology for Intel corporation microprocessors [1]: (a) minimum device size, (b) transistor counts and (c) power dissipation.

One consequence of higher power consumption is higher device operating temperature, which may in turn degrade device performance and reliability. Notebook computer users can easily feel the heat from the backsides of their computers. Device performance and reliability degrade significantly when devices are over heated. Heat generation and thermal management are becoming one of the barriers to further increases in clock speed and decreases of feature size. Many electronic devices, such as microprocessors and power amplifiers are operating at or near the edge of their reliability [2]. Even small

cooling is beneficial to these devices. It was reported that a 5~10 K cooling can double the device reliability [3].

In addition to upper limit operating temperature control, temperature stabilization is often required for temperature sensitive microelectronic and optoelectronic devices to achieve precise operational characteristics. One example is semiconductor lasers, whose output wavelength and power shift with operation temperature changes. In high dense wavelength division multiplexed (DWDM) optical communication network applications, adjacent channels are separated by a wavelength difference of only 0.2~0.4 nm, while typical temperature-dependent wavelength shifts for these laser sources are on the order of 0.1 nm/K. Therefore a temperature change of only a few degrees in a DWDM system would be enough to switch data from one channel to the adjacent one, and even less of a temperature change could dramatically increase the cross talk between two channels [4].

Many microelectronic and optoelectronic devices have better performance at lower temperatures. For example, infrared detectors have a higher signal to noise ratio at lower temperatures because the thermal noise decreases with decreasing the temperature. Low temperature operation is required for small signal detections. Low operating temperature can also improve CMOS electrical performance [5, 6]. The improvements from low temperature

operation include: faster switching time; increased speed due to higher mobility and lower electrical resistance of interconnecting materials; and a reduction in thermally induced failures of devices and components. Besides smaller feature size, lower temperature operation is also an important way to further increase device performance, as shown in Figure 1.2 for 0.1 μm gate length CMOS circuits [7].

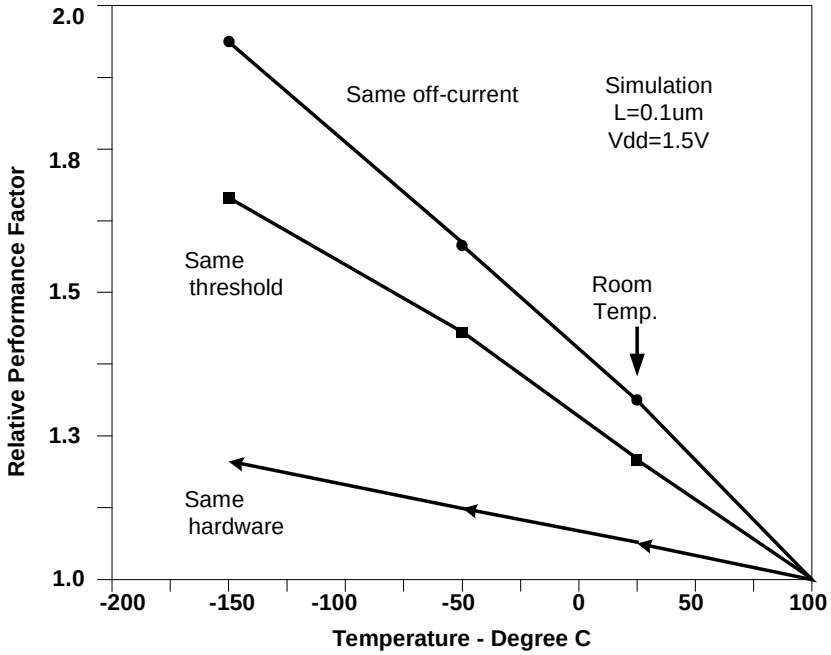


Figure 1.2 Relative performance factors (with respect to the 100 °C value) of 1.5 V CMOS circuits as a function of operating temperature [7].

Therefore, there are great needs for efficient cooling to improve the performance and reliability of microelectronic and optoelectronic devices. There are many cooling methods. Based on the cooling mechanism, these methods can be divided into active cooling and passive cooling.

Air cooling and liquid cooling are passive cooling. They transfer heat by conduction or convention. Air or liquid flow is used to enhance the heat conduction, but they can't cool the device below ambient temperature. Passive cooling is the most commonly used thermal management method for microelectronics. Its main research efforts are developing high thermal conductivity substrates, low thermal resistance heat sinks and packaging, efficient air or liquid flow to remove the heat. When a lower than ambient temperature is needed or passive cooling is not sufficient to fulfill the thermal management tasks, active cooling must be used.

Active cooling is a cooling method that actively pump heat out of its cooling target, the cooling can happen no matter the ambient temperature are lower or higher than the device temperature. Common active cooling includes compressor-based cooling and thermoelectric (TE) cooling. Compressor-based cooling is the most widely used active cooling method, which uses mechanical pumps to actuate the compression and expansion of specific working fluids, such as CFCs (chlorofluorocarbons) and HCFCs (hydrochloroflurocarbons),

according to the principle of thermodynamics. Ordinary household refrigerators and air conditioners are compressor-based cooling. However, CFCs and HCFCs can destroy the ozone layer and are harmful to the environment. One alternative to CFC refrigerators can be thermoelectric coolers which use thermoelectric cooling. Thermoelectric cooling is an environmentally friendly solid-state cooling method based on the Peltier effect. The thermoelectric cooler is an electrical device without moving parts. It uses electrical current instead of fluid or gas to pump out the heat. One fascinating property of thermoelectric devices is that they can work multifunctionally. In the application of temperature control, thermoelectric coolers can work as both coolers and heaters depending on the electric current flow direction; in the application of energy conversion, electrical current can cause temperature difference across the thermoelectric module, and temperature difference across the thermoelectric module can generate electrical current or voltage. Thermoelectric devices make possible cooling without the use of CFCs and electricity generation under naturally occurring temperature-differences. The TE module is a very simple device to convert electric energy into heat and vice versa directly. However, the use of the thermoelectric modules had been limited because of the low efficiency of energy conversion. There have been

many efforts in the research on thermoelectrics including increasing the efficiency of thermoelectric cooling.

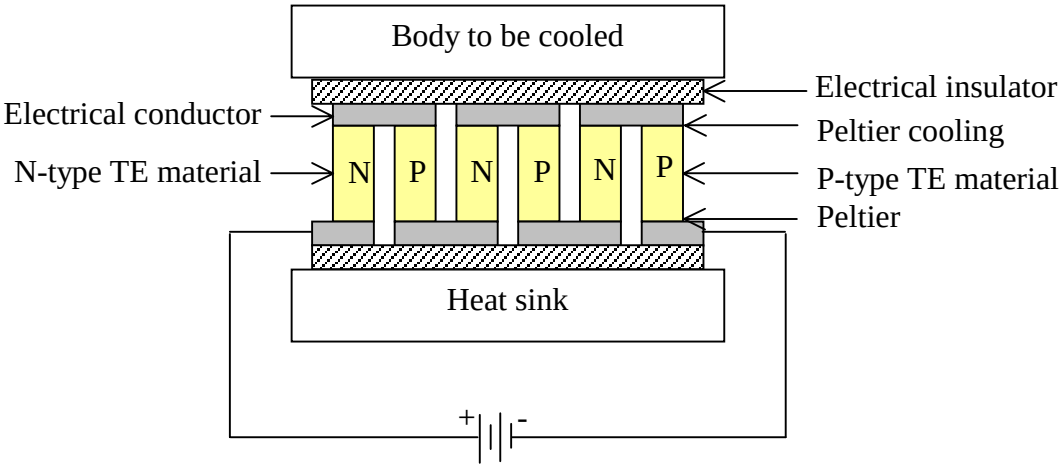
Besides efficiency, the cooler size and weight are also an important consideration for the thermal management of microelectronic devices, especially for portable devices. One of the development directions of microelectronic devices is more powerful but with smaller sizes. Today laptop computers can be more powerful than the house-size super computers fifty years ago. The typical size of today's microelectronic chip is in the order of millimeters to centimeters and their device components such as transistors are in the order of sub-microns to microns. Compressor-based refrigerators are generally too big to cool semiconductor chips. It is hard to imagine applying compressor cooling in handheld devices like palm computers or cell phones. Thermoelectric coolers are compact and lightweight and they can fit the size of semiconductor chips easily. Thermoelectric cooling is an attractive way for spot and portable temperature control. If we want to cool smaller spots, such as individual transistors, microcoolers are needed.

Microcoolers are a new research area. It is highly preferable to integrate the microcoolers directly with microelectronic devices. About 95% of the current microelectronic devices are based on silicon. People are familiar with the heat generation associated with the microelectronics devices. However, is it possible

to use conventional silicon-based semiconductor material to make integrated coolers to cool microelectronic devices? This is an interesting topic and this is what this thesis explores. In this chapter, we present an overview of the research in thermoelectric cooling and microcoolers and give the outline of this thesis.

1.2 Thermoelectric cooling

The thermoelectric cooling is based on Peltier effect which was discovered by the French scientist Peltier in the early 19^{th} century [8]. When electrical current passes through the junction between two dissimilar conductors, there will be a Peltier cooling or heating effect at the junction depending on the current direction. By properly thermoelectric material selection, thermoelectric coolers can be made. Figure 1.3 shows a typical thermoelectric cooler structure, it is a single stage thermoelectric cooler. If more cooling temperature is needed beyond the capacity of a single stage thermoelectric cooler, two or more coolers can be stacked together to achieve more cooling temperature, and these are called multi-stage TE coolers.



(a)

(b)

Figure 1.3 (a) The schematic dıagram of a thermoelectric cooler (b) A photograph of a commercial thermoelectric cooler and its structure.

Compared with compressor-based refrigerators, TE coolers have following advantages: (1) TE coolers are solid state and have no moving parts. This makes them highly reliable, silent and no vibration during operation. (2) TE

coolers are compact, light weight and capable of spot cooling. The size of typical commercial thermoelectric coolers is in the order of millimeters to centimeters, much smaller than conventional compressor-based refrigerators. Smaller sizes TE microcoolers are possible [9-11]. (3) TE coolers can have fast response speed. In TE cooling, the heat is carried away by electrical current. This is a high-speed process. In addition, the compact structure of TE cooler also reduces the thermal equilibrium time of the TE cooler. (4) TE coolers are environmental friendly. There are no volatile gases like CFCs and HCFCs.

TE coolers also have their limitations. First, their efficiency is relatively low. Like other active cooling methods, thermoelectric cooling consumes electrical power. The efficiency is usually characterized by the coefficient of performance (COP), which is defined as the ratio between the cooling power and the electrical power dissipation of the cooler. It is highly preferable to maximize the COP and lower the cooler electrical power consumption. The COP depends on the temperatures of the cold and hot sides of the coolers, the cooling methods, cooler materials and structures, etc. Unfortunately, the COP of conventional thermoelectric coolers is only about 1/3 to 1/5 of that of compressor-based refrigerators. Improving the efficiency of thermoelectric coolers is one of the main research focuses on thermoelectric cooling. Second, they have relatively low cooling power density. With increasing the heat load,

the maximum cooling temperature will decrease. At zero cooling temperature, the maximum heat load can be applied to the cooler is called the maximum cooling power. When the heat load exceeds the maximum cooling power, the TE cooler actually becomes a heater, and the device to be cooled will work at a higher temperature the circumstance without the TE cooler. The maximum cooling power is proportional to the cooling area of the TE cooler. The cooling power density (cooling power per unit area) is a more comparable parameter between different coolers. The typical maximum cooling power density is below 10 W/cm^2 for commercial TE coolers. However, the power density of some modern high power microelectronics is already in the order of tens of W/cm^2. Increasing the maximum cooling power density of TE cooler is essential to cool these high power devices.

1.3 Ways to enhance thermoelectric cooling

Thermoelectric cooling is a promising cooling method for many applications. It has been widely used to cool optoelectronic devices, such as semiconductor lasers. It has a distinct advantage or potential for reliable spot cooling, which is very attractive for cooling microelectronic devices. However,

due to its relatively low efficiency and limited cooling power density, the application of thermoelectric cooling to microelectronic devices is still limited. Trying to overcome these limitations has been the research focus on thermoelectric cooling. Current research on thermoelectric cooling can be divided into three areas: new TE materials; ways to enhance thermoelectric cooling; TE cooler device.

1.3.1 New TE materials

The performance of thermoelectric coolers depends on the thermoelectric properties of the TE materials used. Thermoelectric materials are generally evaluated by the dimensionless TE figure of merit $ZT = S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity and T is absolute temperature. Good thermoelectric materials require high figure of merit ZT. Since the discovery of the thermoelectric effect, there has been a continuing effort to find better thermoelectric materials. Alloys based on the Bi-Te system have been the best TE material for over thirty years and little improvement in ZT has been achieved in the time period. With the development of new methods of material synthesis and new theories for enhancing thermoelectric cooling, there has been a renewed interest in thermoelectric materials [2].

High figure of merit requires high Seebeck coefficient, high electrical conductivity and low thermal conductivity. However, these three parameters are interconnected at some degree and they can't all go in the direction of high figure of merit. High electrical conductivity often comes with high thermal conductivity and low Seebeck coefficient. Metal materials are a good example of this, and they are generally not very good materials for thermoelectric cooling. One hot area of thermoelectric research is to make "electron-crystal, phonon-glass" materials originally proposed by Slack [12]. In this picture, a loosely bound atom scatters phonons much more strongly than electrons, thus permitting a "glasslike" thermal conductivity to coexist with the high electron motilities found in crystals. One example for this concept is filled skutterudite antimonides, like $LaFe_3CoSb_{12}$.

1.3.2 Quantum confinement to increase TE figure of merit

Semiconductor heterostructures and superlattices have been widely used in optoelectronic and microelectronic devices for better performance. It is natural to think if these material structures can be useful for thermoelectric cooling. In 1993, Hicks and Dresselhaus proposed that large increases in ZT could be achieved in quantum well structures [13]. Since then much work has been in the study of thermoelectric properties of low dimensional materials, such as

superlattices, quantum wells, quantum wires and quantum dots, both theoretically and experimentally [14-19]. The reasons of the enhancement of ZT from low dimensionality include: (1) enhancement of the density of states near fermi energy leading to an enhancement of the Seebeck coefficient, (2) increased carrier mobility at a given carrier due to quantum confinement, modulation doping and δ-doping phenomena, (3) opportunities to take advantage of the anisotropic Fermi surfaces, (4) increased boundary scattering of phonons at the barrier-well interfaces, while effectively preserving carrier mobility by exploiting the different length scale for phonon and electron scattering, and (5) the different temperature dependences of the transport properties and intrinsic carrier excitation in low dimensional systems relative to 3D systems [20].

1.3.3 Carrier pocket engineering

For in-plane electrical transport, the Seebeck coefficient enhancement comes from the quantum confinement in the quantum wells. The barrier layers generally don't contribute to the thermoelectric figure of merit improvement, and they conduct heat which actually reduces the overall figure of merit. One way to solve this problem is to use "carrier pocket engineering" proposed by Koga et al [21-24]. Carrier pocket engineering is a systematic process by which

low dimensional superlattice of given constituents are designed to optimize their 3D thermoelectric properties. The design parameters optimized in this process include: the thickness of the barrier layer and quantum well; the growth direction of the superlattice; the lattice strain of the quantum well and barrier layers as controlled by the composition and lattice constant of the substrate; and the carrier density.

1.3.4 Phonon engineering

Unlike usual microelectronic materials, thermoelectric materials require low thermal conductivity. Heat conduction is through phonon transport. One approach to reduce thermal conductivity is to use nanostructures such as quantum wires and quantum wells. It is possible to reduce thermal conductivity through phonon boundary scattering. Superlattices and nanostructures have been used to reduce thermal conductivity [25, 26].

1.3.5 Transient cooling

At steady state, the maximum cooling temperature is determined by the figure of merit of the thermoelectric material. There is an optimized current to get the maximum cooling in the thermoelectric cooler. With smaller current, there will be less Peltier cooling; with larger current, the Peltier cooling will

increase, but the Joule heating will increase even more, which makes the cooling temperature smaller. The Peltier cooling happens at the cold side of the thermoelectric leg of the cooler, while Joule heating happens throughout the whole thermoelectric and it takes some time to get thermal equilibrium at the cold side of the thermoelectric element. It is possible to get large cooling temperature transiently. Thermoelectromechanical refrigeration based on transient thermoelectric effects was proposed by Miner et al [27-29]. In this method, as shown in Figure 1.4, a periodic pulse current (larger than the optimal steady cooler current) is used to drive the cooler and the cold side of the cooler is controlled by a mechanical cantilever to contact the cold side of the thermoelectric legs only when they are cold. Calculation on Bi_2Te_3 shows 35% increase in maximum cooling is possible with this method [27]. This kind of cooler is more complicated than conventional thermoelectric coolers and it is still in the research stage.

1.4 Thermionic cooling

Besides thermoelectric cooling, thermionic cooling in semiconductors is another promising solid state cooling method. In 1994, thermionic cooling in

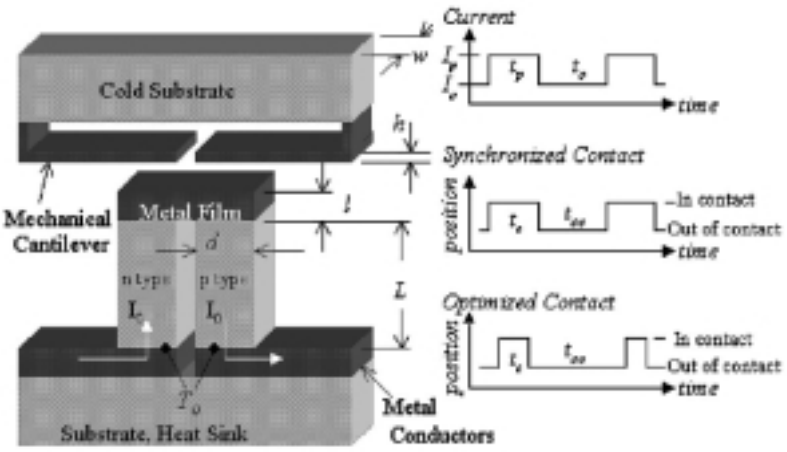


Figure 1.4 Schematic diagram of a thermoelectromechanical cooler based on transient TE effects. Diagram of the pulsed current applied to the cooler, and the two modes of cantilever contact: synchronized contact, for which pulse width is equal to contact time; and optimized contact, for which pulse width is longer than contact time. Contact time of optimized operation is designed such that heat flow is only from the cantilever to the cold junction [27].

air or vacuum was proposed by Mahan using cathode-vacuum(or air)-anode structure [30]. Electrical carriers like electrons whose thermal energy larger than the material's work function will be emitted to the anode under certain voltage bias. For electrical carriers that their thermal energy is below the work function will be left in the cathode. Thermionic emission can be used for thermionic cooling by selectively removing hot electrons. However, the work functions of current materials are too high for enough electrons to be thermally emitted at room temperature. In 1997, Shakouri and Bowers proposed heterostructure thermionic cooling [31]. In this idea, a semiconductor

heterostructure is used in place of the cathode vacuum structure. A small barrier can be easily achieved in semiconductor heterostructures. Many calculations show that efficient thermionic cooling is possible with heterostructures [32-36]. Another important feature about heterostructure thermionic cooling is that it can be achieved efficiently with conventional semiconductor heterostructures such as GaAs/AlGaAsSb, InP/InGaAsP, Si/SiGe, etc. This makes it possible to make integrated thermionic micro cooler similar to the fabrication of integrated circuits [31, 37].

Thermionic energy conversion is based on the idea that a high work function cathode in contact with a heat source will emit electrons. These electrons are absorbed by a cold, low work function anode, and they can flow back to the cathode through an external load where they perform useful work. Practical thermionic generators are limited by the work function of available metals or other materials that are used for the cathodes. Another important limitation is the space charge effect. The presence of charged electrons in the space between the cathode and anode will create an extra potential barrier which reduce the thermionic current. Recently, Mahan proposed these vacuum diodes for thermionic refrigeration. The same vacuum diodes that are used for generators under applied bias will work as a cooler on the cathode side and a heater on the anode side. Mahan predicted efficiencies of over 80% of the

Carnot value, but these refrigerators only work at high temperatures (>500 K). We will look at the prospects of heterostructure for thermionic refrigeration in the following.

In cooling by thermionic emission, the amount of heat absorbed in the cathode is the total current times the average energy of carriers that are emitted over the barrier. As the energy distribution of emitted electrons is almost exclusively on one side of Fermi energy, upon current flow, the strong carrier-carrier and carrier-lattice scatterings tend to restore the "quasiequilibrium" Fermi distribution in the cathode by absorbing energy from the lattice, and thus cooling the emitter junction.

One of the main benefits of heterostructure integrated thermionic cooling is the fact that there are fewer constrains on the materials to be used. Thermoelectric cooling using semiconductors in the linearized Boltzmann transport regime requires a material with high electrical conductivity and thermopower but low thermal conductivity. In the case of thermionic cooling, the barrier material should have a reasonably good electrical conductivity and very low thermal conductivity, but there is no requirement for high thermopower; the band edge discontinuities at the anode and cathode will do the job sufficiently.

One could combine the advantages of heterostructure thermionic cooling with lower dimensional structures by considering thermionic emission in multiquantum well structures. The changes in density-of –states will affect the thermionic current and its cooling capacity. The cascading of heterostructures in order to reach lower temperatures can easily be done during the crystal growth and by fabrication of extra electrical contacts for intermediate layers. With existing sophisticated semiconductor processing techniques, if in some applications the thermal conductivity of the barrier is a limiting factor, one could selectively remove the barrier layer and recover the old vacuum thermionic generator with extremely small and precise cathode-anode separation. This also gives the possibility of negative electron affinity semiconductors or microfield emission devices as the cathode; or to use dipole doping and band gap engineering to modify the work function of the materials. It is expected that these heterostructure thermionic coolers would require small voltages and high currents. The possibility of using hole thermionic emission opens the way to put many devices thermally parallel and electrically in series, similar to TE cooler devices.

1.5 Miniaturization of TE coolers

Although TE coolers are much smaller than any other commercial coolers, they are still much lager than individual microelectronic or optoelectronic devices. Recently, there are many efforts to further miniaturize the TE coolers. Besides trying to cool smaller spot, there is much interests in making TE cooler thinner towards thin film coolers. The main advantage of thin film coolers is their high cooling power densities. The cooling power density Q of a single element cooler can be expressed as

$$Q = \kappa(\Delta T_{max}-\Delta T)/d \qquad (1.1)$$

where κ is the thermal conductivity of the TE element, ΔT_{max} is the maximum cooling temperature, ΔT is the cooling temperature, d is the thickness of the TE element. The cooling power density decreases as the cooling temperature increases. When $\Delta T = \Delta T_{max}$, there will be no cooling power available. When $\Delta T = 0$, the TE cooler will have the largest cooling power density $Q_{max} = \kappa\Delta T_{max}/d$. Compared with the bulk cooler, ΔT_{max} of thin film coolers can be the same as bulk coolers while the thickness d is much smaller. The cooling power density is inversely proportional to the cooler thickness d. So thin film coolers

have a much larger cooling power density than bulk coolers. Figure 1.5 shows the cooling power vs. TE element thickness for ΔT_{max} = 70 K and κ = 0.015 W/cmK.

Conventional TE materials are Bi_2Te_3 based. The processing of them is a bulk technology. The material is polycrystalline and very fragile. It is very difficult to make a cooler less that 100 μm thick with the bulk materials. One approach to solve this problem is to grow TE thin film materials and make a cooler with them. There are many material studies, but experimental device work is limited.

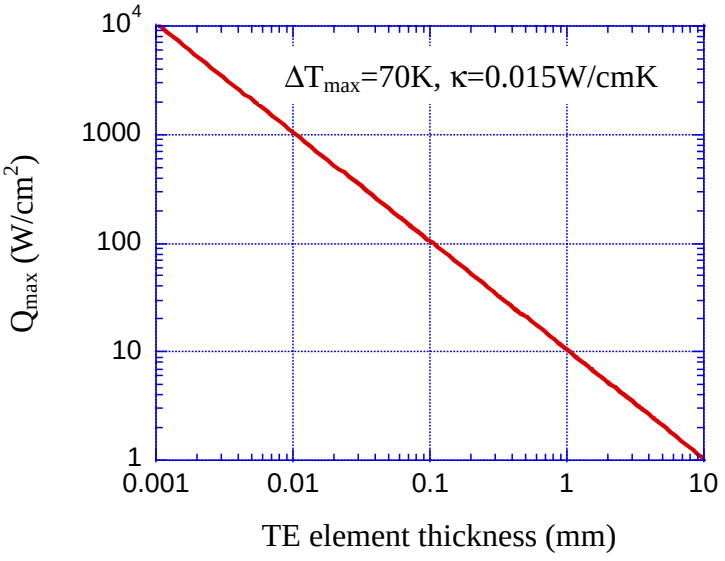


Figure 1.5 Maximum cooling power at ΔT=0 for ΔT_{max} = 70 K and κ = 0.015 W/cmK.

1.6 Integrated coolers

Most TE coolers are made individually and need to be packaged and contact properly with the devices to cool. This will require much labor and a cost for packaging. There are also reliability issues associated with the packaging. An ideal way to solve these problems would be to make thermoelectric coolers in an integrated way, like the fabrication of integrated circuits, and preferably make the coolers monolithically integrated with the devices that need to be cooled. Conventional TE materials, like Bi_2Te_3, cannot be processed the same way as conventional semiconductors, like Si and GaAs. Their processing is a bulk technology.

One integration approach is proposed by Min [38]. The device structure is shown in Figure 1.6. A very thin amorphous SiC film is deposited on a silicon substrate. A membrane is formed by removing the silicon substrate over a desired region using micro-machining. Thermoelectric elements are then deposited on the membrane, using conventional thin film deposition and patterning techniques, and configured so that its central region witch is to be cooler, is surrounded by the cold junctions of the Peltier thermoelectric elements while the hot junctions are located on the outer peripheral area which rests on the silicon substrate rim. Heat is pumped laterally from the central

region to the silicon substrate rim and then dissipated vertically through it to an external heat sink.

The SiC film works as a mechanical support for the TE elements. However, it also conducts heat from the heat sink side to the cooling side, which reduces the maximum cooling. Due to the heat conduction is in the in-plane direction in the TE element, the heat transfer cross-section area is very small, thus the cooling power is small. It is estimated that the maximum cooling power for the 0.3 mm long and 5 μm thick elements is about 2 mW.

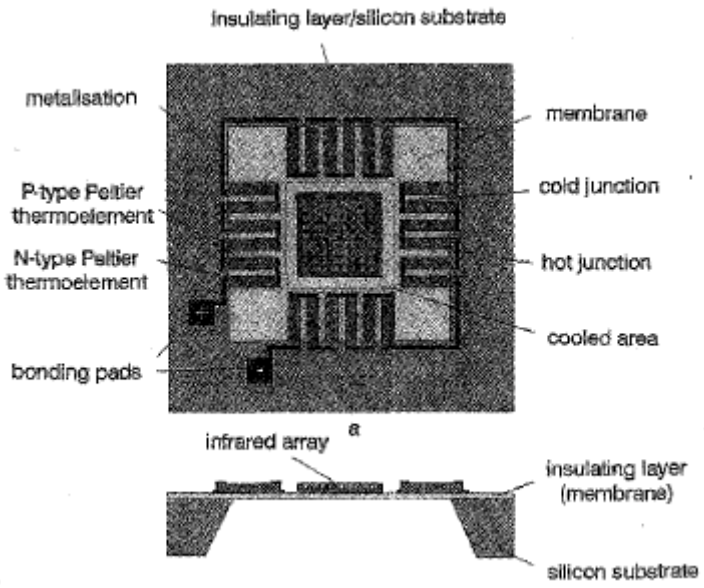


Figure 1.6 Schematic diagrams showing thin film thermoelectric coolers with infrared elements integrated onto cooled central region. From Min [38].

For large cooling power, large area and thin electrical transport length is required. This is relatively easier to achieve with cross plane transport structures, which is our main effort in this thesis.

1.7 Silicon microcoolers

The ideal way to integrate microcoolers with microelectronic devices is monolithic integration. It requires fabricating the microcooler and microelectronic on the same chip and preferably still use the standard integrated circuit (IC) processing technology. To realize this, conventional semiconductor materials need to be used as cooler materials. Unfortunately, most of the conventional semiconductor materials, like silicon and GaAs, have very low figure of merit at room temperature. This makes very low thermoelectric cooling performance. The state-of-art Bi_2Te_3 based thermoelectric materials can make good thermoelectric cooling, but their material growth and device processing are incompatible with IC processing, which makes them very difficult for monolithic integration with other microelectronic devices if not possible. This is a dilemma in the selection of microcooler materials for monolithic integration. Recent advances in the

research of thermoelectric materials and theories (as described in section 1.3), especially for superlattice materials, give us the hope to solve this dilemma. With the development of materials technology, such as molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), superlattice structures can be precisely controlled and grown to make high performance microelectronic and optoelectronic devices. Theoretical analysis and experimental results have shown superlattice structures can enhance the thermoelectric figure of merit through quantum confinement, carrier pocket engineering, thermionic emission and phonon engineering. The concepts apply for both conventional microelectronic materials and the state-of-art thermoelectric materials. The latest breakthrough in thermoelectric materials was reported by Venkatasubramanian et al. in Nature [39]. A figure of merit of 2.4 was obtained on p-type Bi_2Te_3/Sb_2Te_3 superlattices at 300 K, this is over twice that of the best present bulk thermoelectric materials at room temperature. With the thermoelectric enhancements from superlattices or heterostructures, it may now possible to make high performance microcoolers with conventional semiconductors.

Since silicon is the dominant semiconductor material for microelectronic devices, silicon-based microcoolers can have wide potential applications in integrated local thermal management. Silicon is an excellent microelectronic

material, but it is a poor thermoelectric material with a maximum figure of merit of only 0.014 [23]. This implies the maximum cooling temperature is only about 2 K, which is too small for any meaningful practical applications. This low figure of merit of silicon mainly comes from its high thermal conductivity 150 W/mK (compared with that of about 1 W/mK for Bi_2Te_3). Alloy and superlattice structures can reduce elemental material's thermal conductivity sharply by phonon alloy scattering, interface scattering, etc. This can be seen in Figure 1.7, which shows the thermal conductivity for some typical materials.

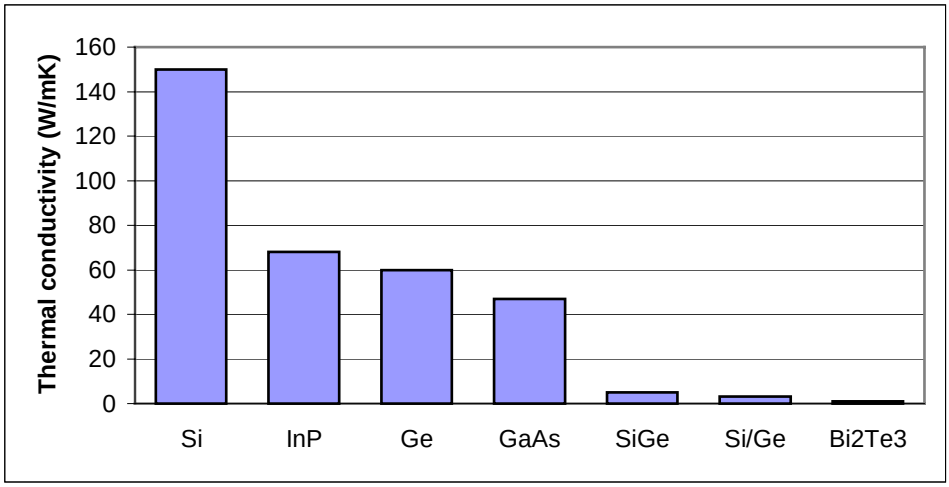


Figure 1.7 Thermal conductivity of some common semiconductor materials.

Among the commonly used semiconductor materials in microelectronics and optoelectronics, SiGe has the best figure of merit. SiGe is one of the best thermoelectric materials for high temperature refrigeration and power generation applications [40]. It has been used for thermo-nuclear power generation in satellites for deep space missions [41]. In this thesis, we use SiGe and SiGe/Si superlattice to make microcoolers for room temperature applications [10, 42-44]. At room temperature, the thermoelectric figure of merit of bulk SiGe alloy is around 0.1, which can give a maximum cooling of over 10 K. Although this cooling is much less than that of Bi_2Te_3 coolers, SiGe coolers can be monolithically integrated with other silicon devices and have many potential applications. To pursue better device performance, superlattice structures are used to take advantage of the recent process in thermoelectrics, such as quantum confinement, carrier pocket engineering, phonon engineering and thermionic emission. Figure of merit ZT up to 0.96 and 1.25 has been predicted on (111) oriented strain-symmetrized and strain-nonsymmetrized Si/Ge superlattices at 300 K, respectively, through carrier pocket engineering [22]. This makes the integrated superlattice microcooler research very promising.

Since the lattice constant of Ge and SiGe is larger than that of silicon, a buffer layer is required for thick Ge or SiGe layer on silicon. This adds some

complexities in both materials growth and the integration between the cooler and other microelectronic devices. To solve this problem, carbon can be added to SiGe to reduce its lattice constant to match with that of silicon. Lattice matched SiGeC/Si superlattice and SiGeC microcoolers are also fabricated and characterized [11].

1.8 Outline

In this thesis, we will explore silicon based solid-state microcoolers, including both theoretical modeling and experimental work. The outline of this thesis is as following: Chapter 1 gives the introduction of the current research on thermoelectric materials and coolers. Integrated microcoolers can be based on thermoelectric and thermionic cooling. Chapter 2 gives the theoretical modeling and material optimization for thermoelectric and thermionic cooling. With decreasing the cooler size to microcoolers, some non-ideal effects, such as contact resistance, can't be ignored anymore. The design of microcoolers is discussed in Chapter 3. Chapter 4 describes the thermoelectric properties characterization of thin film and superlattice materials that will be used in thermoelectric cooling, with emphasize on the thermal conductivity

measurement. In Chapter 5, SiGe/Si microcoolers will be described, including design, processing, characterization and analysis. In Chapter 6, the SiGeC and SiGeC/Si system will be studied for integrated cooling. The advantage of SiGeC is that its lattice constant can be adjusted to match that of Si by properly selecting the Ge and C ratio, thus makes it possible to integrated the microcooler with silicon microelectronic devices without the use of SiGe buffer layers. Chapter 7 gives the summary of the work and future work.

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Chapter 2

Thermoelectric cooling and thermionic cooling

The compressor refrigerators are generally large and not suitable for spot cooling. Solid-state active cooling is an attractive way for localized cooling and temperature control. Thermoelectric (TE) cooling is the most commonly used solid-state active cooling method. Thermoelectric coolers are compact, lightweight and very reliable. They have been widely used to cool microelectronic and optoelectronic devices. Another active cooling method is thermionic cooling. The thermoelectric cooling was originally based on thermionic emission through vacuum [1]. In 1997, Shakouri and Bowers proposed integrated heterostructure thermionic cooling, which uses common semiconductor materials and no vacuum is needed [2]. Since then, much work has been done in thermionic cooling and some work showed it is possible for thermionic cooling to outperform thermoelectric cooling [3-12]. Both thermoelectric cooling and thermionic cooling can be used for integrated microcoolers. In this chapter, we will discuss the theories for thermoelectric cooling and thermionic cooling and their material and device requirements.

Chapter 2. Thermoelectric and thermionic cooling

2.1 Thermoelectric effects

There are three thermoelectric effects: Peltier effect, Seebeck effect and Thomson effect. They were discovered by Jean Peltier, Thomas Seebeck and William Thomson respectively between 1821 and 1855 [13]. Thermoelectric devices are based on these effects.

2.1.1 Peltier effect

As shown in Figure 2.1, when two materials A and B are joined together and a current I flows through the junction, then heat is generated or absorbed at the junction at a constant rate. The rate Q is directly proportional to the current and changes sign if the current changes sign.

$$Q = \Pi_{AB} I \tag{2.1}$$

where the notation Π_{AB} indicates the current flow from conductor A to conductor B. Obviously,

$$\Pi_{AB} = -\Pi_{BA} \tag{2.2}$$

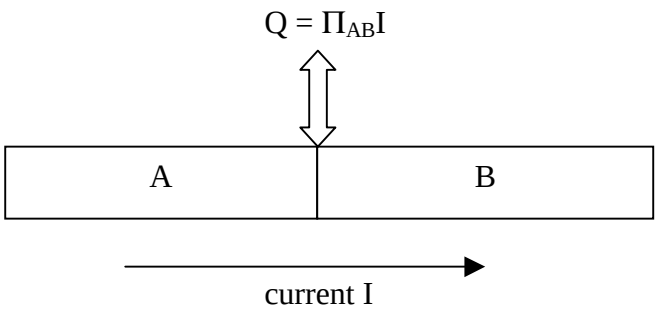


Figure 2.1 Peltier effect

This effect is called Peltier effect, the rate of heat generation Q is known as Peltier heat, and the coefficient Π_{AB} is known as the Peltier coefficient. Peltier effect has been used for thermal management applications. Thermoelectric cooling is in fact Peltier cooling.

To illustrate the physical origin of Peltier effect, we take an ohmic metal-semiconductor contact as an example. Figure 2.2 shows an ohmic metal-n-type contact, and we assume that positive current is flowing from the metal into the semiconductor. Electrons thus flow from the semiconductor into the metal. The electrons enter the metal with a kinetic energy 2kT, 0.5kT for two perpendicular directions of motion parallel to the contact and kT for the direction of motion perpendicular to the contact (as in the thermionic case). Their average energy is thus $|E_f|$+2kT above the Fermi level of the metal, and

so an electron gives an average energy $|E_f|+2kT$ to the metal. If a current I is flowing, the rate at which energy is developing at the junction is

$$Q = \frac{I}{e}(|E_f|+2kT) \tag{2.3}$$

Hence,

$$\Pi_{mn} = \frac{|E_f| + 2kT}{e} \tag{2.4}$$

The symbol Π_{mn} indicates that current flows from the metal to the n-type semiconductor and the positive sign indicates that heat is extracted from the semiconductor and supplied to the metal.

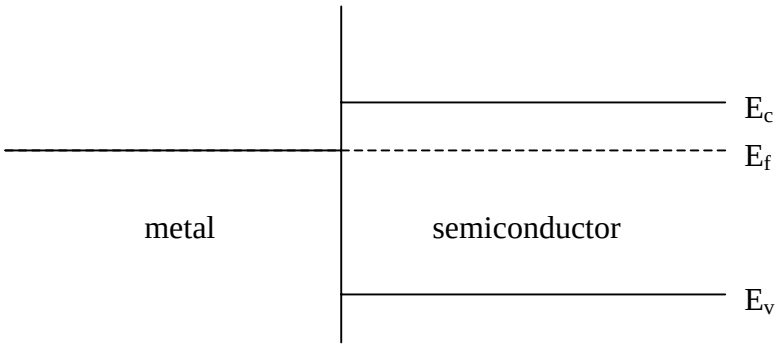


Figure 2.2 Metal and n-type semiconductor contact

If the direction of current flow is changed, heat is extracted from the metal. The electrons now enter the semiconductor with an energy 2kT and have to climb a potential barrier $|E_f|+2kT$, and hence the rate at which the rate at which energy is supplied to the junction is

$$Q = -\frac{I}{e}(|E_f|+2kT) \tag{2.5}$$

so that the effect has indeed changed sign and

$$\Pi_{nm} = -\frac{|E_f| + 2kT}{e} = -\Pi_{mn} \tag{2.6}$$

Next, we turn to an ohmic metal-p-type contact and we assume that positive current is flowing from the metal into the semiconductor. Holes are now emitted into the p-type semiconductor with an average energy of 2kT, and holes generated at the Fermi level have to climb a potential barrier $E_g-|E_f|$. Consequently, the average supplied by the metal to a hole crossing the contact is $E_g-|E_f|+2kT$. The rate Q at which heat is supplied to the junction if a current I is flowing is therefore

$$Q = -\frac{I}{e}(E_g - |E_f| + 2kT) \tag{2.7}$$

and hence

$$\Pi_{mp} = -\frac{E_g - |E_f| + 2kT}{e} \tag{2.8}$$

The above Peltier cooling model is valid for non-degenerate semiconductor materials. It can be seen that the higher doping, the closer Fermi level to the band edge, the smaller the Peltier coefficient will be. For degenerate semiconductors, the Peltier effect can be explained with differential electrical conductivity as in reference [3, 14]. It also shows that the Peltier coefficient decreases with increasing the material doping.

2.1.2 Seebeck effect

As shown in Figure 2.3, if two materials A and B are joined at two points 1 and 2 and a temperature difference ΔT is maintained between the two junctions, then an open-circuit potential difference ΔV is developed. This effect is called the Seebeck effect. The Seebeck coefficient S_{AB} is defined by

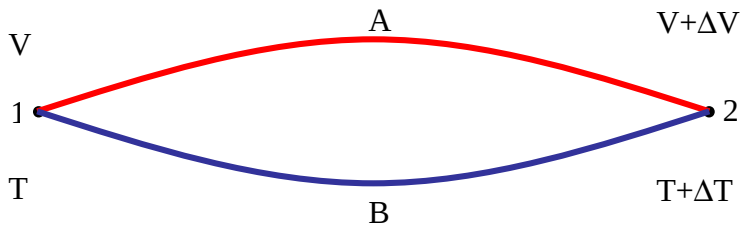


Figure 2.3 Seebeck effect

$$S_{AB} = \lim_{\Delta T \to 0} \frac{\Delta V}{\Delta T} \tag{2.9}$$

If the Seebeck coefficient is known, the temperature difference can be measured through measuring the Seebeck voltage. This is how thermocouples work for temperature measurements. In a closed circuit, the temperature difference induced Seebeck voltage can also be used to drive other electronic devices. This is how thermoelectric power generators work.

2.1.3 Thomson effect

As shown in Figure 2.4, a current I passes through a portion of a single homogeneous conductor over which there is a temperature difference ΔT. It is found that heat is emitted or absorbed at a rate ΔQ that is proportional to the

current I and to the temperature difference ΔT. This effect is called Thomson effect. The Thomson coefficient τ is defined by

$$\tau = \lim_{\Delta T \to 0} \frac{\Delta Q}{I \Delta T} \qquad (2.10)$$

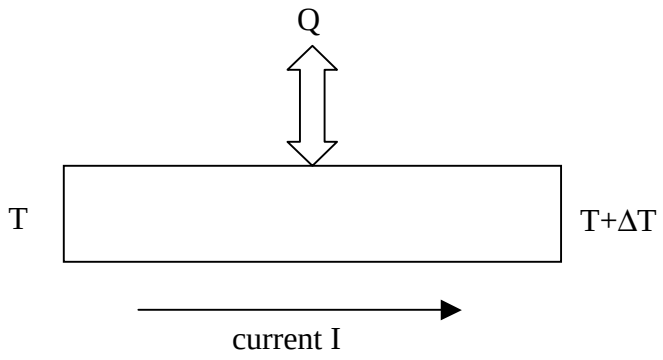


Figure 2.4 Thompson effect

The Thomson coefficient is taken to be positive if heat is evolved when a positive current passes from a higher to a lower temperature.

2.1.4 Kelvin relations

The three thermoelectric effects are thermodynamically related by means of the so-called Kelvin relations [13]:

$$\Pi_{AB} = S_{AB} T \qquad (2.11)$$

and

$$\tau_A - \tau_B = T\frac{dS_{AB}}{dT} \tag{2.12}$$

where T is the absolute temperature, Π is Peltier coefficient, S is Seebeck coefficient and τ is Thompson coefficient.

Of the three TE effects, the Seebeck coefficient is the easiest to measure. In addition, from Kelvin relations, both Peltier coefficient and Thompson coefficient can be expressed with Seebeck coefficient. Therefore, the Seebeck coefficient is the most frequently used one in thermoelectric property descriptions of materials.

2.2 Thermoelectric cooling

Thermoelectric coolers are based on Peltier cooling. To illustrate their working principle, we take a p-type single element TE cooler as an example, as shown in Figure 2.5.

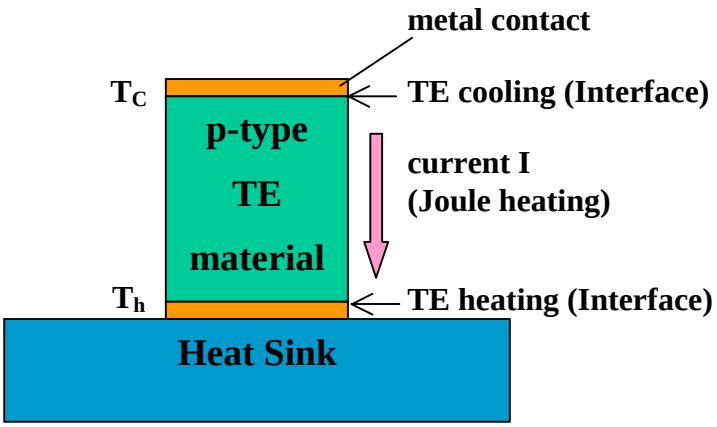


Figure 2.5 Schematic diagram of a p-type single element TE cooler.

When electrical current I goes from the top metal contact into the p-type thermoelectric material, Peltier cooling (TE cooling) will happen at the interface between the top contact metal and the TE material. At the same time, there will be joule heating in TE material and Peltier heating (TE heating) at interface between the TE material and the bottom metal contact. In addition, there will be heat conduction due to the temperature difference between the two ends of the TE material. Here we assume the heat sink is an ideal heat sink and its temperature is kept constant T_h. With the ideal heat sink, the heat dissipation at the hot side of the cooler will not affect the cooler performance at

the cold side of the cooler. The overall rate at which heat is removed from the topside of the cooler can be written as

$$Q_c = \underbrace{ST_cI}_{\text{Peltier cooling}} - \underbrace{0.5I^2d/(\sigma A)}_{\text{Joule heating}} - \underbrace{\Delta T\kappa d/A}_{\text{heat conduction}} \qquad (2.13)$$

where S is the Seebeck coefficient, T_c is the temperature of the cold side (top side in this case) of the cooler, σ is the electrical conductivity of the TE leg, κ is the thermal conductance of the TE material, A is the cross section area of the TE leg and ΔT is cooling temperature (T_h-T_c).

The overall cooling power is driven by the Peltier cooling and reduced by Joule heating in the TE leg and the heat back flow from the hot side of the cooler to the cold side of the cooler. To have maximum cooling power or cooling temperature, an optimal current I_{opt} is required:

$$\left(\frac{dQ_c}{dI}\right)_{Iopt} = 0 \quad \Rightarrow \quad I_{opt} = \frac{ST_cA\sigma}{d} \qquad (2.14)$$

When $I = I_{opt}$, the heat-pumping rate has a maximum value $(Q_c)_{max}$ for a certain cooling temperature ΔT [15].

$$(Q_c)_{max} = (\frac{S^2 T_c^2 \sigma}{2} - \Delta T \kappa)\frac{A}{d} \qquad (2.15)$$

It can be seen that the maximum cooling power density $(Q_c)_{max}/A$ is inversely proportional to the cooler thickness d. Therefore, compared with bulk TE coolers, thin film microcoolers are advantageous for high cooling power densities.

If we set the heat removed from the cold reservoir equal to zero, the temperature difference that the refrigerator maintains becomes a maximum. Hence

$$(\Delta T)_{max} = \frac{S^2 T_c^2 \sigma}{2\kappa}$$

$$= 0.5 Z T_c^2 \qquad (2.16)$$

where Z is the figure of merit

$$Z = S^2\sigma/\kappa \qquad (2.17)$$

It is interesting to note that the maximum cooling temperature only depends on the figure of merit Z and the temperature of the cold side of the cooler, the maximum cooling temperature doesn't change with the geometry of the cooler including the area and thickness of the TE material. To have high maximum cooling temperature, thermoelectric materials with high figure of merit is required. The figure of merit Z is the key parameter to evaluate the overall performance of a thermoelectric material; its dimension is 1/K. ZT is a dimensionless TE figure of merit and is more commonly used in describing TE materials and devices.

Besides cooling temperature, cooling efficiency is another important parameter to characterize the performance of a thermoelectric cooler. The cooling efficiency is usually expressed with the coefficient of performance ϕ which is defined as the ratio between the cooling power Q_c and the electric power consumption w for driving the cooler [13, 15].

$$\phi = \frac{Q_c}{W} = \frac{SIT_c - \frac{1}{2}I^2\frac{d}{A\sigma} - \kappa\frac{\Delta T}{d}}{SI\Delta T + I^2\frac{d}{A\sigma}} \tag{2.18}$$

To get maximum coefficient of performance ϕ_{max},

$$(\frac{d\phi}{dI})_{T_\phi} = 0 \;\Rightarrow\; I_\phi = \frac{S\Delta TA\sigma}{d(\sqrt{1+ZT_M}-1)} \tag{2.19}$$

$$\phi_{max} = \frac{T_c}{\Delta T}\frac{\sqrt{1+ZT_M}-T_h/T_c}{\sqrt{1+ZT_M}+1} \tag{2.20}$$

where Z is the figure of merit and $T_M = (T_c + T_h)/2$.

Like the maximum cooling temperature, the maximum coefficient of performance is also only depends on the figure of merit and the cooler temperatures and independent of cooler size and thickness.

Now it is clear that the figure of merit is the most important parameter for TE coolers. To make high performance TE cooler, it is necessary to select TE materials with high figure of merit.

Although we take a single element p-type TE cooler to illustrate the TE cooler working principle, the analysis and results also apply to n-type TE coolers and n- and p-type cooler arrays. Commercial TE coolers are all in the form of n- and p-type TE element arrays with TE legs electrically in series and thermally in parallel to achieve large cooling area and large cooling power with small currents.

2.3 Material optimization for thermoelectric cooling

In order to achieve high figure of merit Z, it requires a high Seebeck coefficient S, a high electrical conductivity σ, and a low thermal conductivity κ. High electrical conductivity requires high mobility and high doping concentration. For a certain material, doping concentration is the main controllable item to modify Z.

As shown in Figure 2.6, increasing the doping can increase the electrical conductivity, however, it reduce Seebeck coefficient at the same time, and an increase in σ also leads to an increase in the electronic contribution to κ according to the Wiedemann-Franz law [16]. So there is an optimal doping for the maximum Z of a certain material. It has been shown that the optimal doping is to make the Fermi level around the band edge.

Currently, the bulk materials with the highest ZT are the Bi_2Te_3 based alloys such as $Bi_{0.5}Sb_{1.5}Te_3$, with ZT≈1.0 at 300 K. Only small increases in ZT have been achieved on bulk materials in the last three decades.

In contrast to the slow progress in improving figure merit of bulk materials, the thermoelectric research on superlattice materials develops very fast in the past ten years. Recent progress includes the measured ZT up to 2.4 on p-type Bi_2Te_3/Sb_2Te_3 superlattice at room temperature [17]. Superlattices can give

more freedom in engineering the material both thermally and electrically, such as phonon engineering, carrier quantum confinement and carrier pocket engineering [18-23]. Superlattices can also be used for thermionic cooling [2, 9].

Due to the limitations from materials growth, superlattices are generally thin film materials. Currently, they are too thin to make TE cooler legs of millimeter thick, but they can be promising materials for microcoolers. [24-26]

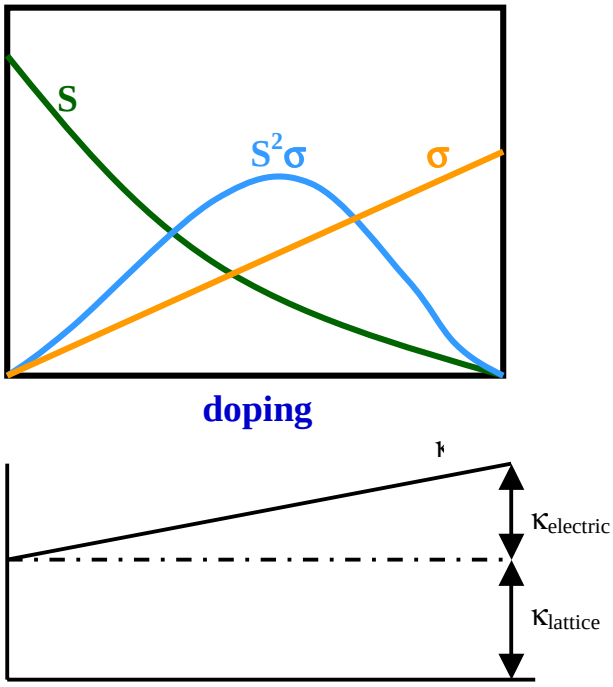


Figure 2.6 Doping concentration vs. S, σ, κ and $S^2\sigma$

2.4 Thermionic cooling

Thermionic cooling is a relatively new solid-state cooling method. Space (vacuum or air) thermionic cooling was proposed by Mahan in 1994 [1] and integrated heterostructure thermionic cooling was proposed by Shakouri and Bowers in 1997 [2]. Thermionic cooling is a process that selectively removes hot electrons through thermionic emission, thus cools the cathode.

2.4.1 Space thermionic cooling

The first generation thermionic cooler consists of a cathode and an anode and they are separated by a small distance (mostly in vacuum space). The cathode and anode can be made of the same or different materials and their work functions can be equal or unequal. For simplicity, we use the equal work functions here to illustrate its working principle. Figure 2.7 shows the schematic diagram of the electron potential energy in the thermionic cooler.

When a bias applied on the cooler structure, as shown in Figure 2.7 (b), there will be a current flow and thermionic cooling and heat will happen at the cathode and anode respectively.

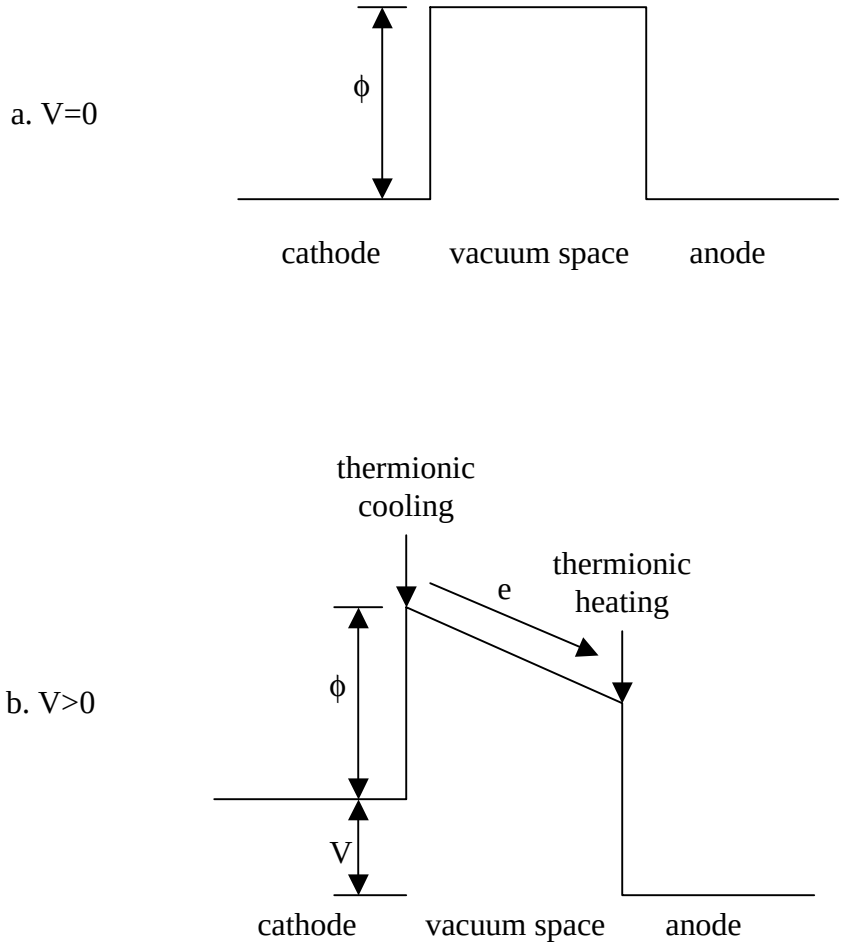


Figure 2.7 Schematic diagram of the potential energy of an electron in the first generation thermionic cooler structure. (a) Equilibrium with V=0; (b) V>0, thermionic cooling happens at the cathode and thermionic heating happens at the anode.

The physical origin of the thermionic cooling or heating is from the difference between the transport energy of the current and the Fermi energy of

the cathode or anode. The electrical current in thermionic coolers is thermionic current; only electrons have energy higher than the potential barrier (here is the work function ϕ) can go through the vacuum space region. In the cathode, hot electrons is removed through thermionic emission and thus reduce average energy in cathode, thus this is a thermionic cooling process; in the anode, hot electrons are injected in from the cathode and thus increase the average energy in anode, thus this is a thermionic heating process. A cooling efficiency of over 80% of the Carnot value was predicted by Mahan, which is very high [1].

The cooling power in cathode is proportional to the thermionic current density J:

$$J(\phi,T) = AT^2 e^{-e\phi / k_B T} \tag{2.21}$$

$$A = \frac{emk_B^{\ 2}}{2\pi^2 \hbar_3} \approx 120 A/cm^2 \tag{2.22}$$

where A is the Richardson constant.

For room temperature refrigeration, the work function should not be larger than 0.3-0.4 eV for efficient cooling. Surface science has searched such a cathode for over 50 years, but none has been found yet. The current available

lowest work function is 0.7-0.8 eV, which is too high for room temperature thermionic emission. To make them useful in thermionic cooling, an operation temperature of at least 500K is required. Otherwise, there would be too little electrons having energy larger than the cathode work function to participate in the thermionic cooling.

Besides lack of low work function materials, the space charge effect is also an important limitation to the vacuum thermionic cooling. The space charges are electrons that are thermally excited from the cathode into the space between the cathode and anode. These changes create an extra potential barrier V_s, which reduces the thermionic current. Figure 2.8 shows space charge effect on the thermionic cooler potential diagram.

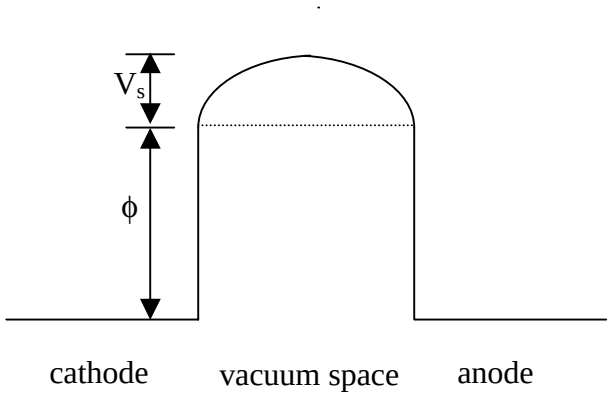


Figure 2.8 Potential diagram of the thermionic cooler with space charges. The space charges increase the effective potential barrier for thermionic emission.

One way to reduce effective cathode barrier height and space charges is to make the cathode and anode very close to each other. The close spacing between the two electrodes can reduce the extra potential introduced by the space charge. At a certain voltage bias, the electric field increases as the spacing between cathode and anode decreases. High electrical field can reduce the effective surface barrier. When the electric field is high enough, electrons go through the barrier through Fowler-Nordheim tunneling. This is generally called field emission instead of thermionic emission. The electron transport energy can be different from the Fermi energy, thus there will be energy transfers associates with the field emission. These energy exchange processes are called Nottingham effects [27, 28]. If the average energy of the emitted electrons is less than that of the replacement electrons of the circuit, the cathode tends to be heated during the emission; if the average energy of the emitted electrons is larger than the replacement of electrons of the circuit, the cathode tends to be cooled. It is possible to make coolers based on Nottingham effects. However, the tunneling usually pulls out electrons within a broad range that results in heating rather than in cooling. To solve this problem, recently, Kortkov and Likharev proposed cooling by resonant Fowler-Nordheim emission [29, 30]. In this method as shown in Figure 2.9, the bulk emitter (a

metal or a heavily doped semiconductor) is covered with a thin layer of a wide band gap semiconductor. As shown in Figure 2.9 (b), applied electric field can create a triangular-shape potential well and the discrete levels localized at the semiconductor film surface. If the lowest subband is aligned with the hot electrons in the emitter, their resonant tunneling to vacuum may lead to the efficient heat removal, and hence to emitter cooling.

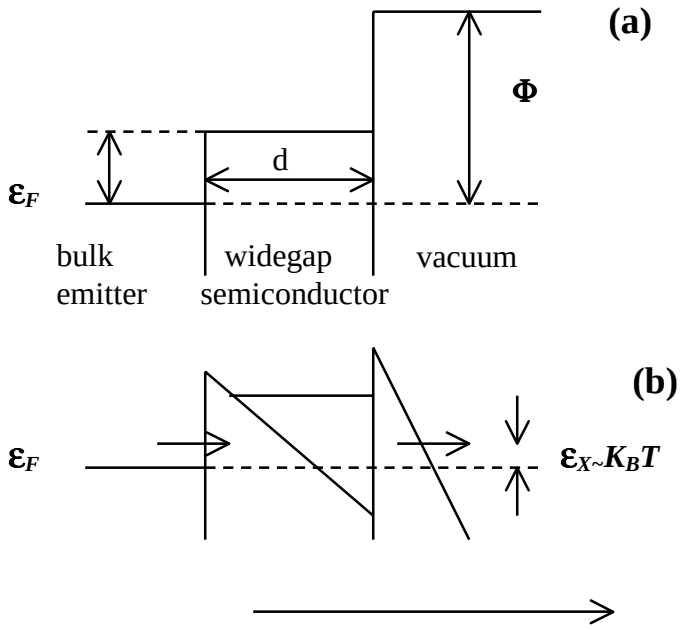
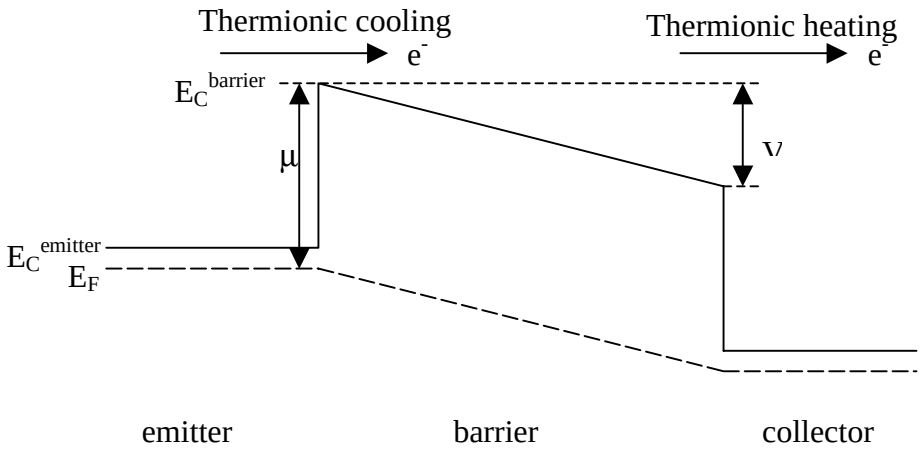


Figure 2.9 The energy band diagram of the resonant Fowler-Nordheim emission cooler. (a) in the absence of applied voltage (b) in a proper electric field. Resonant tunneling via the lower subband removes hot electrons above the Fermi surface, thus cooling the emitter.

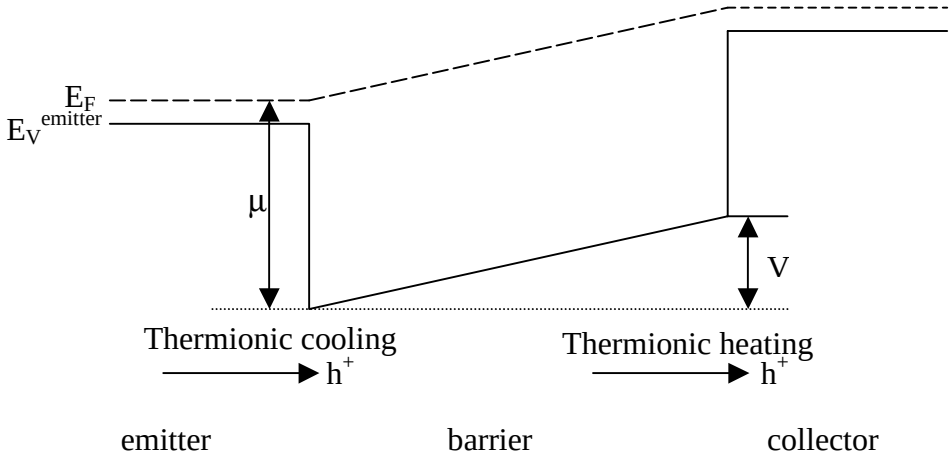
2.4.2 Heterostructure thermionic cooling

Another way to solve the high work function and space charge problem of thermionic coolers is integrated heterostructure thermionic cooling which was first proposed by Shakouri and Bowers in 1997. [2, 31] In this cooling method, semiconductor heterostructures are used instead of the vacuum space. Figure 2.10 shows its band structure.

The band structure of heterostructure thermionic cooling is very similar to the potential diagram of vacuum space thermionic cooler. The main difference is that the vacuum space is replaced by a semiconductor layer, and the potential barrier becomes the heterostructure energy barrier instead of the material work function. Small barriers can be easily obtained from conventional semiconductor heterostructure like GaS/AlAs, InGaAs/InP, SiGe/Si etc. As shown in Figure 2.10, both n-type and p-type materials can be used. This gives more freedom in thermionic material selection make it possible to make n- and p-type integrated thermionic cooler arrays thermally in parallel and electrically in series to achieve large cooling power with relatively small electrical current, similar to the conventional thermoelectric cooler configuration.



(a) Conduction band structure for n-type heterostructure thermionic cooler



(b) Valance band structure for p-type heterostructure thermionic cooler

Figure 2.10 Band structure of heterostructure thermionic cooling. (a) conduction band structure for n-type heterostructure thermionic cooler (b) valance band structure for p-type heterostructure thermionic cooler.

Theoretical calculations show that efficient cooling could be achieved with heterostructure thermionic cooling and it is possible for integrated thermionic coolers to outperform thermoelectric coolers [2, 3, 6, 8, 9, 11, 31]. As shown in Figures 2.11 and 2.12, cooling power density in the order of thousands of watts per square centimeter and cooling of tens of degree could be achieved with integrated heterostructure thermionic cooling at room temperature.

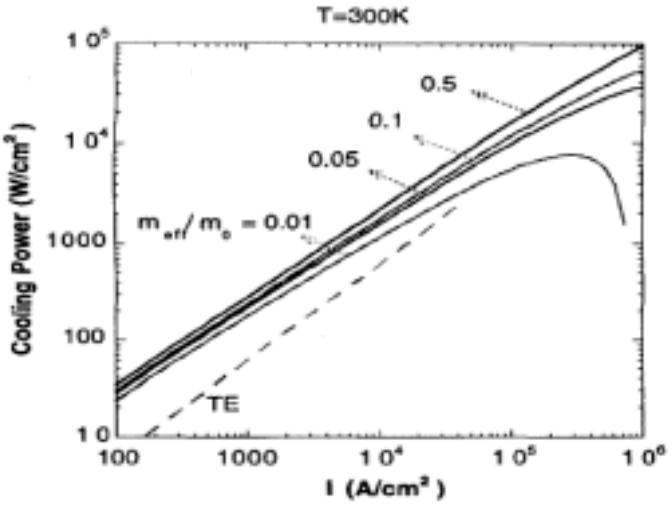


Figure 2.11 Thermionic cooling power as a function of current for different values of electron effective mass at room temperature. The dashed curve corresponds to TE cooling power for a typical Bi_2Te_3 material. From Shakouri and Bowers [31].

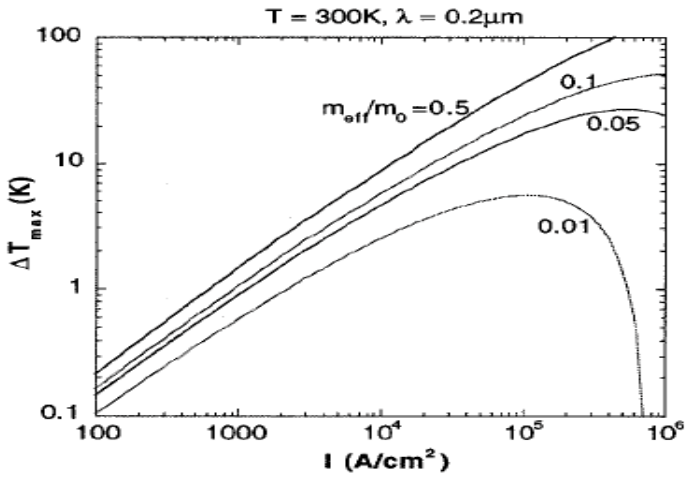


Figure 2.12 Maximum cooling temperature as a function of current for different values of the electron effective mass with an electron mean-free-path of 0.2 μm in the barrier. From Shakouri and Bowers [31].

Semiconductor heterostructures have been widely used in microelectronics and optoelectronics for better device performance. The rapid development of the materials technology, such as molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), paves the road to make high quality heterostructures, including precise control of layer thickness and compositions of thin film growth. Using various materials (such as GaAs/AlGaAsSb, InP/InGaAsP, Si/SiGe, HgCdTe/CdTe), one can produce different barrier heights in the cathode and anode to have efficient thermionic emission.

2.4.3 Material optimization for heterostructure thermionic cooling

For a single barrier heterostructure thermionic cooler, the thermionic cooling power Q_{TI} can be expressed as [6]

$$Q_{TI} = \underbrace{[\phi + 2\frac{k_B T_c}{e}]I}_{\text{thermionic cooling}} - \underbrace{IV[(\frac{1}{2} - \frac{\lambda}{d}) - \frac{\lambda^2}{d^2}(e^{-d/\lambda} - 1)]}_{\text{Joule heating}} - \underbrace{\frac{\kappa}{d}\Delta T}_{\text{heat conduction}} \qquad (2.23)$$

where ϕ is the emitter side barrier height, d is the barrier thickness, κ is the barrier thermal conductivity and λ is the carrier mean free path in the barrier. The three parts in the equation are thermionic cooling, Joule heating and heat conduction respectively. High performance thermionic cooler requires high thermionic cooling, low Joule heating and low heat conduction.

To reduce the heat conduction from hot side of the cooler to the cold side, low thermal conductivity κ is required. To reduce the Joule heating, materials with high mobility, thus long carrier mean free path, is required. To have high thermionic cooling, high ϕI is required. However, increasing the barrier height ϕ will cause less thermionic current according to thermionic emission Equation 2.21. It can be shown that the optimal barrier height is in the order of $k_B T/e$. One way to enhance thermionic emission is to select materials with high carrier

effective mass m_{eff}. High m_{eff} will increase the effective Richardson constant for thermionic current, thus better thermionic cooling performance. This can be seen in Figures 2.11 and 2.12.

Recently Shakouri et al. proposed high barrier heterostructures to enhance thermionic emission [3, 6]. In this method, tall barriers in a highly degenerate semiconductor are used to selectivity emit hot electrons and to achieve thermionic cooling similar to the original small barrier heterostructure thermionic coolers. With the large number of carriers involved in the conduction process, small electric field can be applied to achieve substantial cooling.

Unlike ideal thermoelectric coolers, single barrier thermionic cooler has an optimized barrier thickness for largest cooling. The optimal barrier thickness can be obtained from the derivative of equation for thickness on Equation 2.23. It is usually on the order of carrier electrical mean free pass. If the thickness is too small, the heat conduction from the hot side would be too large. If the thickness is too thick, it will become the same as thermoelectric cooler. As we will discuss in the next chapter, thin film coolers have some non-ideal effects, such as contact resistance etc, which will reduce the cooler performance. The thinner the cooler material, the stronger maximum cooling temperature reduction by the non-ideal effects. To reduce this problem, multilayer or

superlattice thermionic cooler can be used. In addition, superlattice can be used to reduce thermal conductivity through interface phonon scattering.

2.5 Comparison of heterostructure thermionic cooling with space thermionic cooling and thermoelectric cooling

Integrated thermionic cooling is different from space thermionic cooling in that it uses a semiconductor layer to take place the space layer (vacuum or air space). The advantage of this is that low barriers can be easily obtained and adjusted with the heterostructures and it is possible to have monolithic integration with microelectronic and optoelectronic devices. The disadvantage of this heterostructure structure is also from its non-vacuum structure. The vacuum doesn't conduct heat and vacuum structure is the most effective way to prevent heat conduction. Even using air space taking place the vacuum, the heat conduction is far less than any solid materials. The thermal conductivity of air is 0.026 W/mK, which is about two orders smaller than those of common thermoelectric materials [32]. Considering currently no suitable low work function material available, heterostructure thermionic cooling looks more promising than current space thermionic emission cooling.

In terms of cooler structure, heterostructure thermionic coolers are similar to thermoelectric coolers. They cool at the heterostructure junction of metal-semiconductor junctions with current pass through them. One basic difference is whether the current flow is ballistic or diffusive. In thermionic cooling, the device has relatively high efficiency if the carriers ballistically go over and across the barrier. They carry all of their kinetic energy from one electrode to the other. In thermoelectric cooling, the motion of carriers is quasiequilibrium and diffusive [8].

One of the main difficulties in increasing the figure of merit of thermoelectric materials is that the Seebeck coefficient decreases with increasing electrical conductivity. In thermionic cooling, the barrier material should have reasonably good electrical conductivity and very low thermal conductivity, but there is no direct requirement for high Seebeck coefficient; the band edge discontinuities at the heterostructure junctions will do the job sufficiently. Therefore, heterostructure thermionic cooling has fewer constrains on the materials to be used and it is possible to use conventional semiconductor heterostructures or superlattice, like GaAs/AlAs, InP/InGaAs and Si/SiGe, to make integrated thermionic coolers.

Integrated thermionic cooling is still a new research area. Many theoretical calculations with Boltzmann approximation show that it can outperform

thermoelectric cooling [2, 3, 6, 9, 14]; there are also some calculations with Fermi-Dirac statistics show that single barrier thermionic cooling can't outperform thermoelectric cooling [33, 34]. Despite their cooling mechanism difference, they both require the materials having low thermal conductivity, high electrical conductivity and high carrier effective mass etc. Both thermoelectric cooling and thermionic cooling can coexist in a heterostructure or superlattice cooler structure. For superlattice thermionic cooling, it can be modeled as an effective thermoelectric material with effective Seebeck coefficient and effective electrical conductivity. They can use the same microcooler design principles in Chapter 3.

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Chapter 3

Microcooler design

Thermoelectric coolers are much smaller and lighter than compressor refrigerators. They are a reliable method for spot cooling. TE coolers in the order of millimeters to centimeters are commercially available and they have been widely used to optoelectronic devices, such as semiconductor lasers. Microcoolers are attractive for their smaller sizes and higher cooling power densities from shorter thermoelectric legs [1-3]. However, microcoolers, below one millimeter, are rarely seen in the market. One reason for this is that the processing of conventional thermoelectric materials, like Bi_2Te_3, is a bulk technology [4]. It is very difficult to machine and assemble the tiny thermoelectric electric legs for microcoolers. In addition, with smaller cooler thickness, non-ideal effects, such as electric and thermal contact resistance, begin to show adverse impacts on microcooler performance and more comprehensive theoretical model are needed in microcooler device design [5, 6]. In this chapter, we will start with the material selection for silicon microcoolers, and then the non-ideal effects in thin film microcoolers, and

finally discuss the issues that need to be taken into the TE cooler model for further minimize the cooler thickness down to below 100 μm.

3.1 Material selection

From the general theory of thermoelectric cooling in chapter 2, the material's TE properties are the key parameters in determining the cooler performance. This is true for both bulk TE coolers and thin film microcoolers. In the ideal thermoelectric cooler model, the maximum cooling temperature ΔT_{max0} and the maximum coefficient of performance ϕ_{max0} all depends on the material's TE figure of merit Z [7, 8].

$$\Delta T_{max0} = 0.5 Z T_c^2 \tag{3.1}$$

$$\phi_{max0} = \frac{T_c}{\Delta T} \frac{\sqrt{1+ZT_M} - T_h / T_c}{\sqrt{1+ZT_M} + 1} \tag{3.2}$$

where $T_M = (T_c + T_h)/2$.

To have high cooling performance, materials with high TE figure of merit are required for the cooler material selection. Figure 3.1 shows the dimensionless figure of merit ZT for some best bulk TE materials at different temperatures [9]. TE figure of merit is temperature dependent and different materials have different best working temperature ranges for thermoelectric applications. At room temperature, Bi_2Te_3 based materials the most commonly used TE materials.

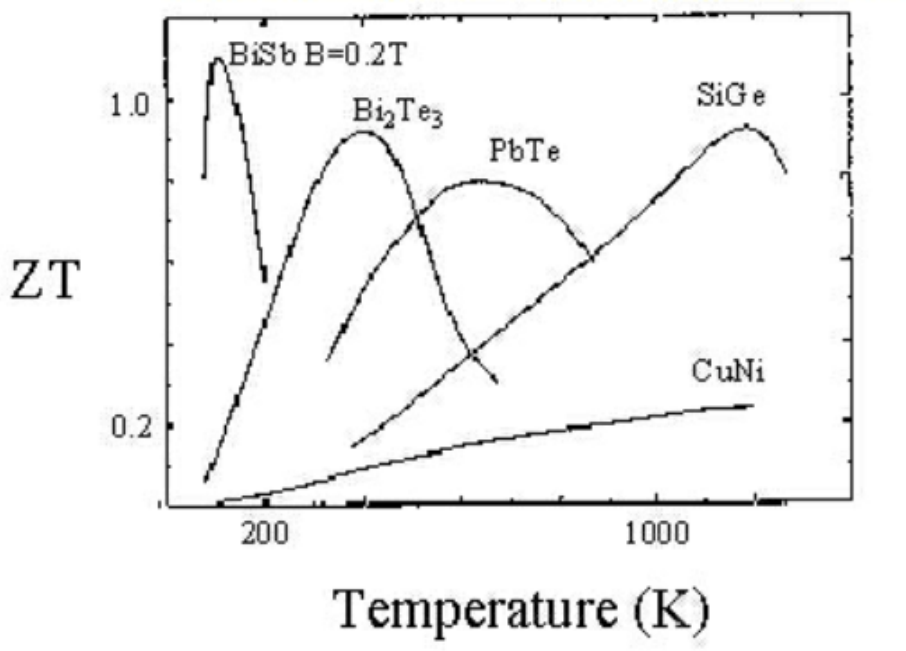


Figure 3.1 The dimensionless TE figure of merit ZT vs. temperature for some of the best thermoelectric materials [9].

Besides TE figure of merit, the processing compatibility with integrated circuit (IC) processing is another important consideration in the material selection for microcoolers. Since the processing of conventional TE coolers is a bulk technology, it is not suitable for the thin film microcooler fabrication. To make silicon microcoolers, it requires the materials processing compatible with IC processing. Table 3.1 lists some possible materials for silicon microcoolers.

Table 3.1 Some possible materials for silicon microcoolers.

Material	ZT (T=300K)	ΔT_{max} (K)	IC processing
Bi_2Te_3	0.9	70	×
Si	0.014	2	✔
SiGe	0.1~0.15	15~20	✔
SiGe/Si superlattice		(>20)	✔
Si/Ge superlattice		(>20)	✔

Bi_2Te_3-based material has been the state of art thermoelectric material for about four decays. They can have a maximum cooling of 70 K with hot side at room temperature. However, the processing of Bi_2Te_3, especially bulk Bi_2Te_3, is not compatible with IC processing. Bulk Bi_2Te_3 is difficult to be machined to thin film and assemble into microcoolers. Recent developments in material

growth have made it possible to grow the Bi_2Te_3-based thin materials directly. This eliminates the need for machining bulk TE materials, but the microcooler processing and packaging are still very challenging. On the other hand, the processing of common microelectronic and optoelectronic materials is comparable with the IC processing and these materials are ideal for integration, but their TE figure of merit is low for room temperature TE cooling applications. For example, the dimensionless figure of merit ZT of silicon is only up to 0.014, this only get a maximum cooling of about 2 K, which is too small for practical applications. One reason for the low ZT of silicon is from it high thermal conductivity (1.5 W/cmK, about two orders larger than the thermal conductivity of Bi_2Te_3). Among the currently commonly used IC processing compatible materials, SiGe is the best thermoelectric material. It can be seen from Figure 3.6 that SiGe is a good thermal electric material for high temperature applications [9, 10]. It has been used for nuclear power generation in spacecrafts [7]. At room temperature, its ZT is much lower than that of Bi_2Te_3 based materials, but over 10 K cooling should be obtainable. Although this cooling is not big, the processing of SiGe is compatible with silicon IC processing and SiGe microcoolers can still be useful for many applications.

Chapter 3. Microcooler design

In recent years, there has been rapid progress in superlattice materials for thermoelectric applications [11-20]. It is possible to design the superlattices to have higher TE figure of merit than their corresponding bulk materials. Compared with bulk TE materials, superlattice can give us more freedom in engineering their thermoelectric properties both thermally and electrically. First, the thermal conductivity can be reduced with superlattice structures through phonon engineering [21, 22]. One mechanism for thermal conductivity reduction is phonon scattering at the layer interfaces of the superlattice. Second, the band structure of superlattices can be engineered to improve the figure of merit through recent thermoelectric theory developments such as quantum confinements, carrier pocket engineering and thermionic emission [23-27]. ZT up to 2.4 has been measured on Bi_2Te_3/Sb_2Te_3 superlattices, which is over two-fold improvement over the state of act bulk TE materials [13]. It should be possible apply the same principles on silicon based superlattices, such as SiGe/Si and Si/Ge superlattice, to improve their TE properties.

In order to make integrated silicon microcooler and take advantage of the latest developments of superlattice thermoelectrics, we use SiGe and Si-based superlattices as the primary materials for the experimental study of integrated microcoolers.[28-30] To solve the problem of lattice mismatch between SiGe

and Si, SiGeC and SiGeC/Si are also used for the microcooler study in this thesis [31].

After selecting the material system, the materials need to be optimized for maximum figure of merit. The material optimization includes composition and doping adjustments. For superlattices, the band structure and periods also need to be optimized to reduce thermal conductivity and maximize thermionic cooling, etc.

3.2. Non-ideal effects in thin film microcoolers

Microcoolers are coolers whose sizes are below 1 mm. In other works, the microcoolers is mainly for thin film coolers. The main advantage of thin film coolers vs. bulk coolers is its high cooling power density. As shown in Eq. 2.15, the cooling power density is inversely proportional to the thickness of the TE material. The cooling power density of conventional bulk coolers is limited and is not enough to fit the fast increasing power dissipation density of modern microelectronic and optoelectronic devices. Thin film coolers are a promising way to solve this problem. Another advantage of thin film coolers is that their processing is different from bulk processing technology and it is possible to be

compatible with semiconductor thin film processing. Therefore, it is possible to achieve integrated thin film coolers.

The working principle for thin film cookers is the same as bulk coolers. However, there are differences in thin film cooler device modeling. The device modeling in Chapter 2 doesn't consider the non-ideal effects, such as contact resistance and the heat sink resistance etc. However, for thin film coolers these non-ideal effects can't be ignored anymore due to the small electrical and thermal resistance of the thermoelectric elements (TE legs). In the device detailed modeling, there is an important factor called aspect ratio, which is defined as ratio between the area and length of the thermoelectric leg. The lower the aspect ratio, the closer to the ideal TE cooler model and the better device performance. For example, for a certain area cooler, when the length is very long, the electrical and thermal resistance of the TE leg is much larger than the contact resistance and heat sink thermal resistance. In this case, the contact resistance and heat sink resistance can be ignored and the ideal cooler model can be valid. However, with reducing the TE leg thickness and going to a thin film cooler, the electrical and thermal resistance of the TE leg gets very small while the contact resistance and the heat sink resistance remain unchanged. Therefore, the non-ideal effects become relatively big and they must be considered for microcooler device modeling.

As in Chapter 2, we take single element p-type thermoelectric cooler as an examples to show the non-ideal effect influences on thin film cooler performance. The schematic diagram of the device structure is shown in Figure 3.2 (a) and its equivalent thermal circuit is shown in Figure 3.2 (b). At each node in Figure 3.2 (b), the net heat flow should be zero at thermal equilibrium.

$$Q_c = \Delta T_1 / R_{th\_pac} \tag{3.3}$$

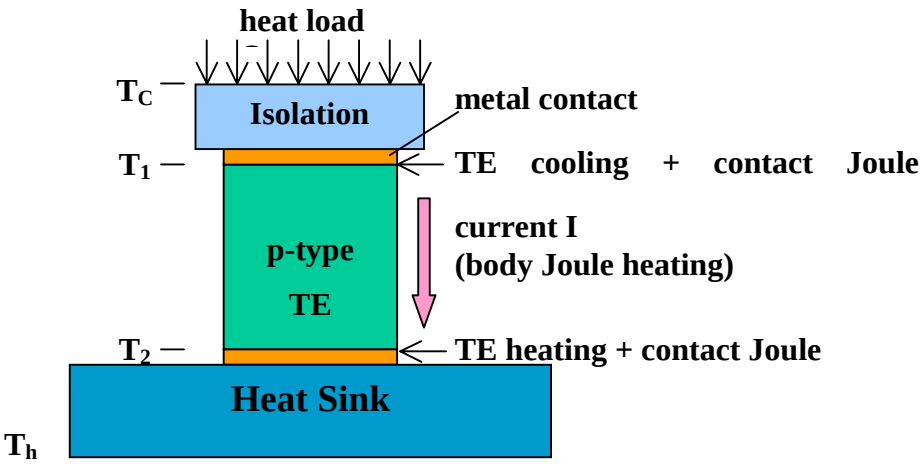
$$Q_c - ST_1 I + R_{c1} I^2 + 0.5RI^2 + \Delta T_2 / R_{th2} = 0 \tag{3.4}$$

$$ST_2 I + R_{c2} I^2 + 0.5RI^2 - \Delta T_2 / R_{th2} - \Delta T_3 / R_{th3} = 0 \tag{3.5}$$

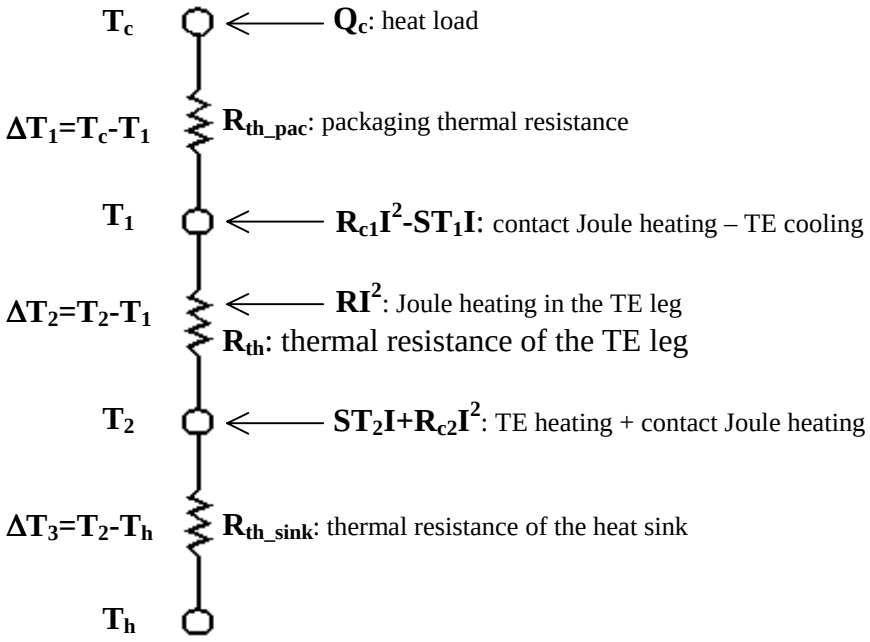
where R is the electrical resistance of the TE leg, R_{c1} and R_{c2} are the top and bottom electrical contact resistance, other parameters are defined in Figure 3.2.

The cooling temperature of the TE cooler is

$$\Delta T = T_h - T_c = \Delta T_2 - \Delta T_1 - \Delta T_3 \tag{3.6}$$



(a)



(b)

Figure 3.2 Thermoelectric cooler with non-deal effects. (a) TE cooler device structure. (b) Thermal equivalent circuit of the TE cooler.

There are several non-ideal effects in microcooler design, such as electrical contact resistance, heat sink thermal resistance, the packaging thermal resistance, etc. They make less cooling than ideal TE coolers. We will discuss them respectively.

3.2.1 Electrical contact resistance

Generally, thermoelectric materials are semiconductor materials and the electrodes are metals. When they are connected, there is always some electrical contact resistance exists at the interface. The contact resistance is usually small. However, for thin film coolers, the TE leg resistance is very small too and contact resistance can't be neglected anymore. The contact resistance will cause Joule heating at the cool side of the cooler during cooler operation, which works as an extra heat load and reduces the maximum cooling. If we ignore other non-ideal effects and only consider contact resistance,

$$Q_c = ST_cI - 0.5(R+2R_c)I^2 - \Delta T/R_{th} \quad (3.7)$$

$$R = \rho \frac{d}{A} \quad (3.8)$$

$$R_c = \frac{r_c}{A} \quad (3.9)$$

$$R_{th} = \frac{d}{\kappa A} \quad (3.10)$$

where Q_c is the cooling power, R is the electrical resistance of the TE leg, R_{th} is the thermal resistance of the TE leg, S is the Seebeck coefficient, T_c is the cold side temperature of the cooler, ρ is the electric resistivity of the TE material, d is the length of the TE leg, A is the cross section area of the TE leg, r_c is the specific electric contact resistance, κ is the thermal conductivity of the TE material.

To get the maximum cooling temperature ΔT_{max},

$$\frac{d\Delta T}{dI} = 0 \quad \Rightarrow \qquad I_{opt} = \frac{ST_c}{R + 2R_c} = I_0 \frac{1}{1 + 2\frac{R_c}{R}} = I_0 \frac{1}{1 + 2\frac{r_c}{\rho d}} \qquad (3.11)$$

When $Q_c = 0$,

$$\Delta T_{max} = R_{th} \frac{S^2 T_c^2}{R + 2R_c} = \Delta T_{max0} \frac{1}{1 + 2\frac{R_c}{R}} = \Delta T_{max0} \frac{1}{1 + 2\frac{r_c}{\rho d}} \qquad (3.12)$$

where $I_0 = ST_c/R$ and $\Delta T_{max0} = 0.5ZT_c^2$. They are the working current and maximum cooling respectively for zero contact resistance (r_c=0) condition.

From Equation 3.12, it can be seen that the maximum cooling decreases with increasing contact resistance. For the same contact resistance, the maximum cooling decreases with decreasing the TE leg length or resistivity.

The ratio between contact resistance and the TE leg resistance is the determining factor for the contact resistance's influence on cooler performance. Figure 3.3 shows the maximum cooling vs. the ratio between contact resistance and the TE leg resistance.

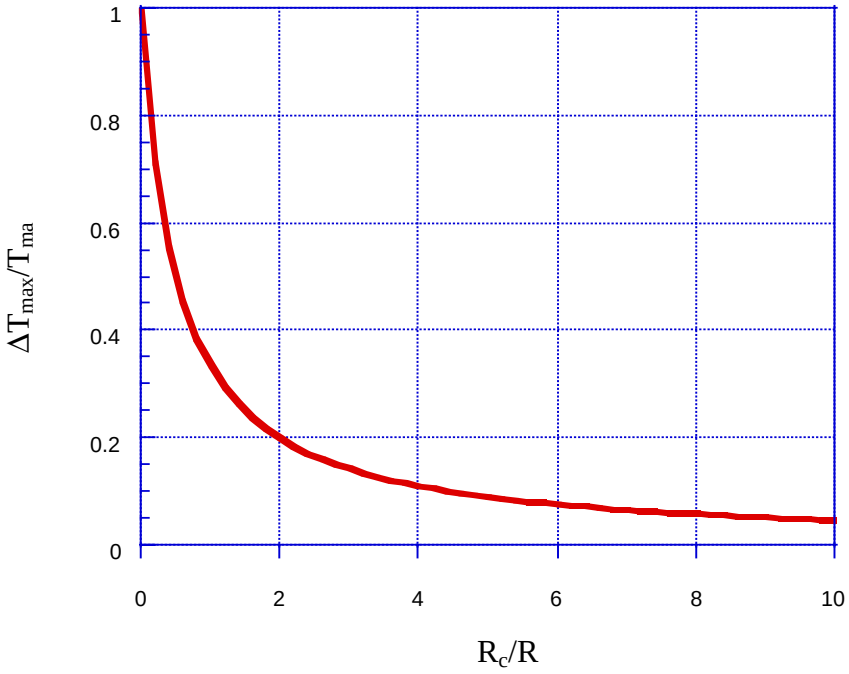
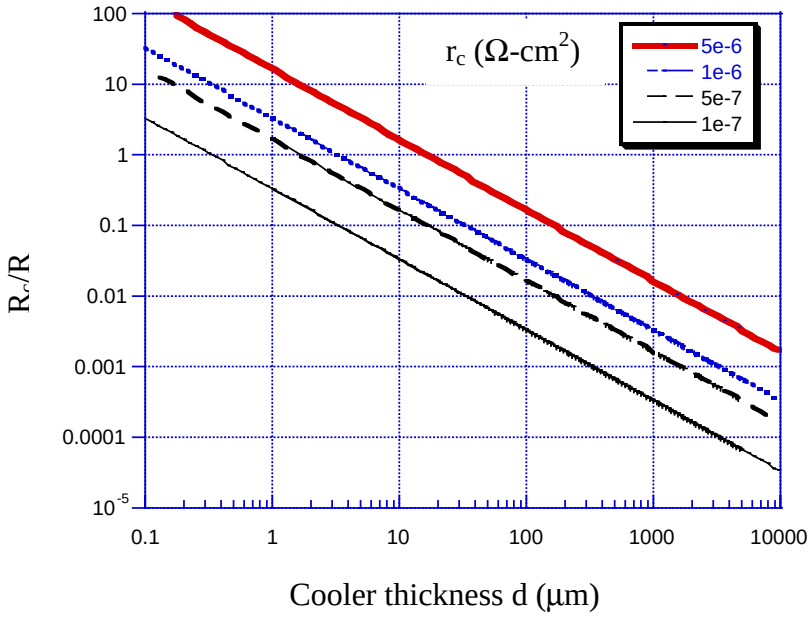


Figure 3.3 Maximum cooling temperature vs. the ratio between the contact resistance and the TE leg resistance of the cooler.

For bulk TE coolers, the length of the TE legs is in the order of millimeters. Their electrical resistance is generally much larger than the contact resistance and the contact resistance is not a big issue. However, when the cooler structure goes from bulk cooler to thin film cooler, the cooler thickness has 1 to

3 orders reduction while the contact resistance unchanged. This make the ratio between contact resistance and TE leg resistance increase 1 to 3 orders accordingly. As shown in Figure 3.4, for thin film coolers on the order of micron thick, the contact resistance will become comparable with or even larger than the TE material resistance and cooling performance will be limited by contact resistance. Therefore, low contact resistance is crucial in thin film cooler design. From Figure 3.4 and Equation (3.12), it can be also seen that the larger the specific contact resistance and the lower resistivity of the TE material, the larger contact resistance impact on thin film cooler performance.

(a)



(b)

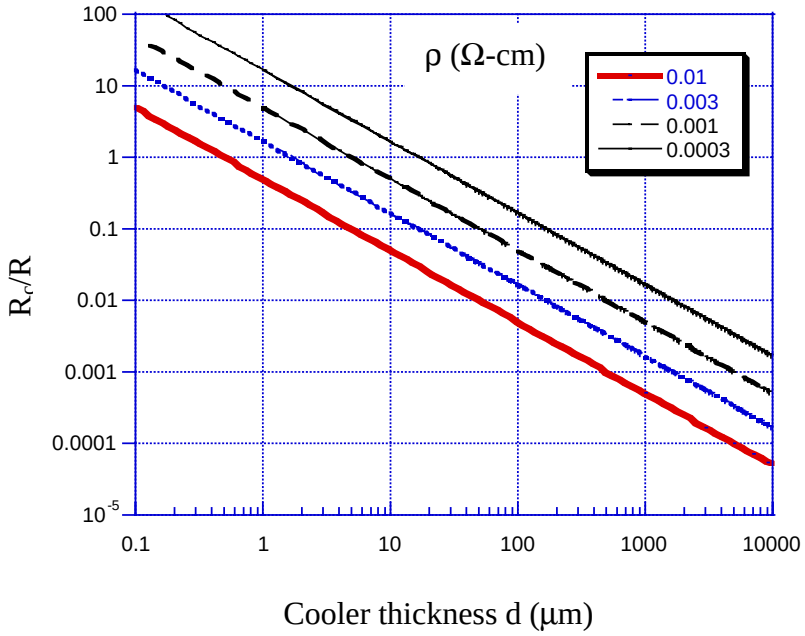


Figure 3.4 The ratio between electric contact resistance and TE leg resistance (R_c/R) vs. the thickness d. (a) ρ=0.003 Ω-cm, for various specific contact resistivity r_c: 5×10^{-6}, 1×10^{-6}, 5×10^{-7} and 1×10^{-7} Ω-cm^2. (b) $r_c=5\times10^{-7}$ Ω-cm^2, for various electrical resistivity of the TE material ρ: 0.01, 0.003, 0.001 and 0.0003 Ω-cm.

As an example, taking ρ=0.003 Ω-cm, Figure 3.5 shows the maximum cooling temperature vs. specific contact resistivity for various TE cooler thickness: 100 μm, 20 μm, 6 μm and 3 μm. It can be clearly seen that the maximum cooling is very sensitive to the electrical contact resistance for thin film coolers. The electrical contact resistance reduces the maximum cooling,

and the thinner TE cooler is, the more reduction there is in maximum cooling. In this example, the maximum cooling reduce almost 70% for a 3 μm thick cooler with a specific contact resistivity of 1.0×10^{-6} Ω-cm^2. To get efficient cooling, a specific contact resistivity of low 10^{-7} Ω-cm^2 or better is required for thin film coolers in the order of several micron thick [29].

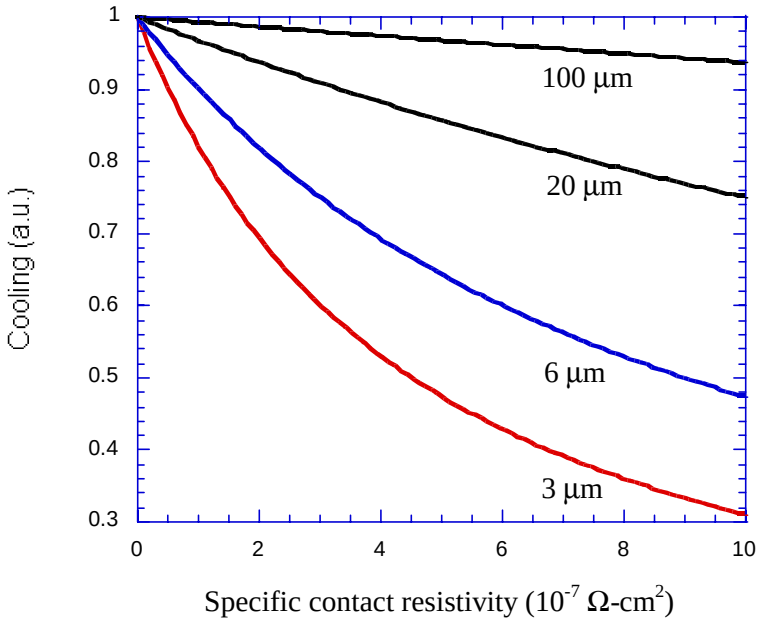


Figure 3.5 Cooling vs. specific contact resistivity for various TE film thicknesses: 100 μm, 20 μm, 6 μm and 3 μm. (assuming the TE film resistivity 0.003 Ω-cm and ideal heat sink)

3.2.2 Heat sink thermal resistance

In the last section, the heat sink was assumed an ideal one whose thermal resistance is zero and its temperature is kept constant during cooler operation. However, the ideal heat sink doesn't exist in reality and there is always some thermal resistance at the cooler's heat sink side. This thermal resistance includes both the thermal resistance of heat sink itself and the thermal resistance between the TE material of the cooler and the heat sink. Here we just call this total thermal resistance as the heat sink thermal resistance R_{th_sink}. When heat passes through the heat sink, the temperature of the heat sink at the cooler side will increase ΔT_{sink}:

$$\Delta T_{sink} = QR_{th\_sink} \tag{3.13}$$

where Q is the heat dissipated through the heat sink, including the cooler heat load Q_c and the electrical power consumption in the cooler:

$$Q = Q_c + (R+2R_c)I^2 + S\Delta T_0 I \tag{3.14}$$

where ΔT_0 is the cooling temperature with ideal heat sink.

$$\Delta T_0 = R_{th}\left[ST_cI - 0.5(R+2R_c)I^2 - Q_c \right] \quad (3.15)$$

The cooler cooling temperature ΔT will be reduced due to the heat sink temperature increase ΔT_{sink}:

$$\Delta T = \Delta T_0 - \Delta T_{sink} \quad (3.16)$$

From Equations 3.13~3.16, it can be shown:

$$\frac{\Delta T}{\Delta T_0} = 1 - \frac{R_{th\_sink}}{R_{th}} \frac{(R+2R_c)I^2 + S\Delta T_0 I + Q_c}{ST_cI - 0.5(R+2R_c)I^2 - Q_c} \quad (3.17)$$

$$\approx 1 - \frac{R_{th\_sink}}{R_{th}} \frac{(R+2R_c)I^2 + Q_c}{ST_cI - 0.5(R+2R_c)I^2 - Q_c} \text{ (for } S\Delta T_0 I << (R+2R_c)I^2 + Q_c)$$

As an example to see the heat sink resistance on cooling temperature of the cooler, we assume S=200 μV/K, ρ=0.003 Ω-cm, k=0.08 W/cmK, $r_c=4\times10^{-7}$ Ω-cm2, A=2500 μm^2, Q_c=0, d=3μm, T=300K. The calculated cooling temperature is shown in Figure 3.6. It can be seen that the cooling temperature decreases with increasing the thermal resistance ratio between the heat sink and TE leg.

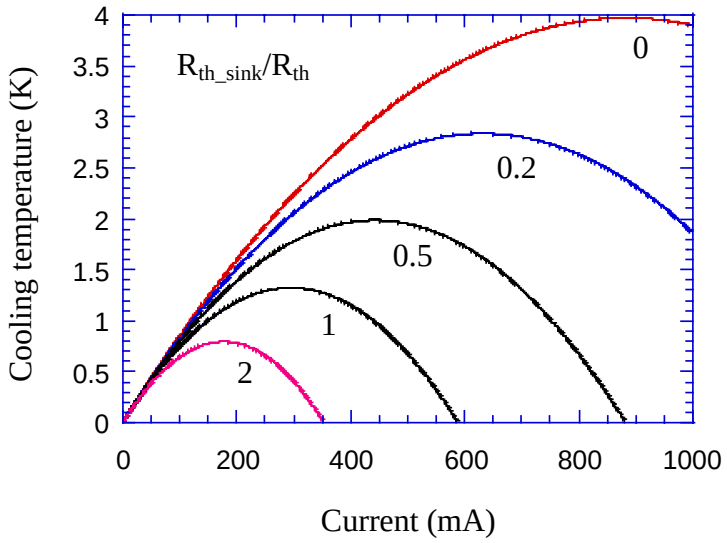


Figure 3.6 Cooling temperature vs. current for various R_{th_sink}/R_{th}. (Taking S=200 μV/K, r=0.003 Ω-cm, k=0.08 W/cmK, $r_c=4\times10^{-7}$ Ω-cm^2, A=2500 μm^2, Q_c=0, d=3μm, T=300K)

For bulk TE cooler, the TE leg thermal resistance is usually much larger than the heat sink thermal resistance. When the cooler goes from bulk cooler to thin film cooler, the TE leg thermal resistance goes down with the cooler thickness, while there is no much change in the heat sink thermal resistance. This increases the thermal resistance ratio between the heat sink resistance and TE leg thermal resistance, thus reduces maximum cooling.

3.2.3 Packaging thermal resistance

The main advantage of a thin film cooler is its large cooling power density, which is inversely proportional to the cooler thickness. One of its important applications is to cool high power devices beyond the capability of bulk TE coolers. When dealing with high power or high power density, low thermal resistance is required to avoid excess temperature increase. In the last section, we discussed the importance of heat sink thermal resistance in thin film cooler design. In this section, we will discuss the thermal resistance between the device to be cooled and the cold side of the TE leg of the cooler.

Conventional TE coolers are discrete devices and they need to be packaged with the cooling target for TE cooling. Here we call the thermal resistance between the cooling target and the TE leg cold side of the cooler as packaging thermal resistance R_{th_pac}. It will reduce the effective cooling temperature ΔT especially for high heat load Q_c.

$$\Delta T = \Delta T_0 - Q_c R_{th\_pac} \tag{3.18}$$

where ΔT_0 is the cooling temperature with ideal packaging ($R_{th\_pac}=0$), and $Q_c R_{th\_pac}$ is the temperature increase at the packaging junction.

From Chapter 2, we know that the maximum cooling of an ideal TE cooler is independent of cooler thickness, while its cooling power density is inversely proportional to the cooler thickness. So when the TE cooler goes from bulk cooler to thin film cooler, the maximum cooling doesn't improve (in fact its decreases due to non-ideal effects such as contact resistance), but it can handle more heat load. With higher heat load, there is a higher requirement for low packaging thermal resistance.

3.2.4 Thermal radiation and air heat conduction

When a cooler works at large cooling temperature, the cold side of the cooler can be well below its environmental temperature. This large temperature difference can induce extra heat loads to the cooler. One heat source is the heat radiation, which is very small at room temperature and below. It is generally negligible in cooler design. Another heat source is air heat conduction or convention when the cooler doesn't work in vacuum environment. Usually, TE coolers work in the air at ordinary air pressure. The air can conduct heat to the cold side of the cooler and the airflow greatly enhances the heat conduction or convention. This heat load reduces the maximum obtainable cooling of the cooler. For bulk TE coolers, their maximum cooling can be reduced up to 10% with in the air operation compared with in vacuum operation.

Compared with bulk TE coolers, thin film coolers are advantageous in their much higher cooling power density. For a similar amount of extra heat load from thermal radiation and heat conduction, the cooler performance should be less affected for thin film coolers than for bulk coolers. This can be also be seen from the following relation between cooling temperature ΔT and the extra heat load Q_{ex}:

$$\Delta T = \Delta T_0 - R_{th} Q_{ex} \qquad (3.19)$$

where ΔT_0 is the cooling temperature without extra heat load and R_{th} is the thermal resistance of the cooler. With reducing the cooler thickness, R_{th} gets smaller and thus the extra heat load, such as heat radiation and air heat conduction, will have less adverse impact on the cooling temperature.

3.3. Silicon microcooler device design

Some design principles of bulk TE coolers still apply to the design of microcoolers, such as selecting high ZT materials, using n- and p-type TE leg array structure, etc. In the last section, we discussed the non-ideal effects for

thin film microcoolers. In the microcooler design, we need to address these issues along with some device fabrication issues.

3.3.1 Minimize the non-ideal effects

First, the electrical contact resistance needs to be minimized for thin film microcoolers. As shown in Equation 3.11, contact resistance is one of the main limitations for thin film coolers. For thin film cooler on the order of several micron thick, specific contact resistance on the order 10^{-7} Ω-cm^2 or lower is required. Ways of reducing contact resistance include increasing contact layer doping of the semiconductor, selecting suitable contact metal and annealing temperature, etc. Depending on the material systems, state of art contact resistances are on the order of 10^{-7} to 10^{-8} Ω-cm^2. One possible way to further reduce contact resistance is to increase the contact area at the cold side of the cooler using the mushroom structure, as shown in Figure 3.7.

Second, the packaging thermal resistance and heat sink thermal resistance need to be minimized for thin film microcoolers. Thin film coolers have high cooling power density, but it also requires very low packaging thermal resistance and heat sink resistance to avoid excess temperature increases when large heat flux pass through these non-ideal thermal resistances. In bulk TE coolers, the two sides of the TE legs are packaged with ceramic plates, such as

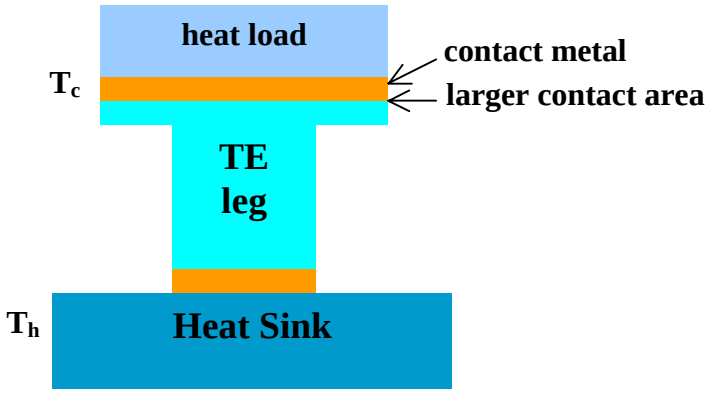


Figure 3.7 The mushroom structure to reduce the contact resistance at the cold side of the cooler.

alumina (Al_2O_3), for the cold side and hot side thermal contacts. For thin film coolers, their thermal resistance becomes relatively large. Using better thermal conductive materials can reduce these non-ideal thermal resistances. The material with highest thermal conductivity is diamond. CVD grown diamond films have been used as the short leg cooler substrates.[2, 3, 32-34] However, this may greatly increase the cost of the microcoolers and the interface thermal resistance between the TE legs and the diamond films remain unsolved.

One way to solve the packing related interface thermal resistance is to make integrated microcoolers. Monolithic integration of microcooler and microelectronic devices that need to be cooled can eliminate the packaging of

the cold side of the cooler. On the cold side of the cooler, the material substrate may also work as the heat sink. Integrated microcoolers not only reduce packaging cost, but also reduce the cooler fabrication cost. Integration is the preferred way to make microcoolers.

3.3.2 Integrated microcoolers

The fabrication for microcoolers is difference from that of bulk coolers. The processing of conventional TE coolers is a bulk technology and it is difficult to be used in the fabrication of thin film microcoolers. Thin film materials are very difficult to be processed and assembled like bulk TE legs. An integrated thin film microcooler is an ideal way for both its fabrication and its cooling applications. Microelectronic devices are mostly based on silicon and there has been an increasing demand for their thermal management. Integrated silicon-based microcoolers have great potential in localized cooling for silicon devices.

To make integrated silicon microcoolers, it requires the cooler materials to be grown on silicon and be compatible with silicon IC processing. SiGe, SiGeC and their superlattices with satisfy these requirements. Their microcooler fabrication will be described in Chapters 5 and 6.

3.3.3 Localized cooling

So far, we have been focused on the cooler thickness for microcoolers. Small thickness tends to have large cooling power density. Cooler size or cooling area is also an important parameter in microcooler design. Localized cooling, such as cooling individual devices instead of the whole chip, requires small cooler size. Integrated silicon microcoolers can be fabricated with IC processing. Small cooler sizes can be obtained and controlled with photolithography and etching. Microcoolers don't have higher coefficient of performance than larger TE coolers. However, with selectively localized cooling, microcoolers may be a more efficient way to solve some thermal issues.

For ideal TE cooler model, the cooler performance, such as maximum cooling temperature and cooling power density, is independent of the cooler size. However, non-ideal effects, such as the heat sink resistance and some non-ideal heat loads, can make the cooler performance size dependent. Detailed discussion will be given in Chapter 5.

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Chapter 4

Thermoelectric property characterization

The thermoelectric properties are the most important factors for the TE cooler performance. Even for thermionic cooling, it still requires the same thermoelectric properties as thermoelectric cooling [1]. Ideally, the maximum cooling temperature ΔT_{max} of the TE cooler is determined by the figure of merit Z of the TE material [2, 3].

$$\Delta T_{max} = 0.5ZT^2 \quad (4.1)$$

$$Z = S^2\sigma/\kappa \quad (4.2)$$

where T is the absolute temperature, S is the Seebeck coefficient, σ is the electrical conductivity and κ is the thermal conductivity. High thermoelectric performance requires a high figure of merit Z. The dimension of Z is K^{-1}. ZT is dimensionless and is called the dimensionless figure of merit. To have high Z, it requires high Seebeck coefficient, high electrical conductivity and low thermal conductivity. The ways to enhance the TE figure of merit were introduced in Chapter 1. In this chapter, the ways to measure the thermoelectric

properties will be discussed, especially for thin film materials that would be used for microcoolers.

4.1 Seebeck coefficient measurement

The Seebeck effect is one of the three thermoelectric effects. The principle of thermocouples is based on the Seebeck effect. When the two ends of a material are at a temperature difference ΔT, there will be a voltage ΔV across the two ends, and their ratio is called the Seebeck coefficient S.

$$S = \Delta V/\Delta T \tag{4.3}$$

The Seebeck coefficient is generally positive for p-type materials and negative for n-type materials. Our setup for Seebeck coefficient measurement is shown in Figure 4.1. Two thermoelectric coolers (TECs) were set at two different temperatures T_1 and T_2 respectively. The sample was cleaved to a strip shape (e.g. 3×10 mm^2) and put across the two TECs. The voltage across the two end of the sample is measured by a voltage meter. The corresponding

temperature difference at these two points is measured by thermocouples. The Seebeck coefficient is calculated as

$$S = \Delta V/\Delta T \qquad (4.4)$$

where $\Delta T = T_1 - T_2$.

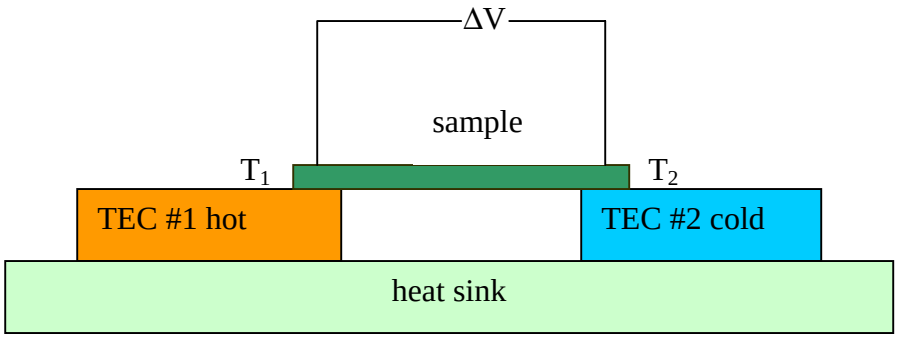


Figure 4.1 Schematic diagram for the measurement of Seebeck coefficient

Thin film materials are usually on the substrates instead of standing alone. The voltage ΔV measured from the above setup comes from both the thin film and substrate contributions. Figure 4.2 gives its equivalent circuit.

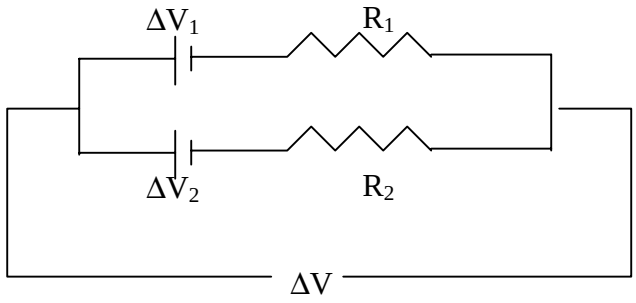


Figure 4.2 Equivalent circuit for the Seebeck measurement

It can be easily shown that

$$\Delta V = \frac{\Delta V_1 R_2 + \Delta V_2 R_1}{R_1 + R_2} \tag{4.5}$$

where ΔV_1 and R_1 is the Seebeck voltage and electrical resistance of the thin film layer, ΔV_2 and R_2 is the Seebeck voltage and electrical resistance of the substrate layer, ΔV is the measured effective voltage. The Seebeck coefficients of the thin layer and the substrate can be expressed as:

$$S_1 = \Delta V_1/\Delta T \tag{4.6}$$

$$S_2 = \Delta V_2/\Delta T \tag{4.7}$$

From Equations 4.4~4.7, the effective Seebeck coefficient of the sample including both the thin film layer and the substrate would be

$$S = \Delta V/\Delta T = \frac{S_1 R_2 + S_2 R_1}{R_1 + R_2} = S_1 \frac{1+\frac{S_2}{S_1}\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}} \quad (4.8)$$

If R_1, R_2 and S_2 are all known, we can deduce the value of S_1 from measured S. Under the following condition:

$$\frac{R_1}{R_2} << 1 \text{ and } \frac{S_2}{S_1}\frac{R_1}{R_2} << 1 \quad (4.9)$$

Equation 4.8 can be simplifies as

$$S_1 \approx S = \Delta V/\Delta T \quad (4.10)$$

When a material has a lower doping, both its electrical resistivity and Seebeck coefficient will increase. However, the electrical resistivity generally increases faster than that of the Seebeck coefficient at low doping levels. To make the measurement and calculation easier, we used semi-insulating silicon

as the substrate, whose resistivity is above 100 Ωcm. For thermoelectric cooling applications, the TE materials are usually highly doped. The doping levels in our SiGe, SiGe/Si superlattice, SiGeC and SiGeC/Si superlattice are in the order of 10^{18}~10^{20} cm^{-3}. It satisfies the Condition 4.9: $\frac{R_1}{R_2} << 1$ and $\frac{S_2}{S_1}\frac{R_1}{R_2} << 1$. Therefore, we can use $\Delta V/\Delta T$ (Equation 4.10) as the Seebeck coefficient of the thin film materials. In this way, we do not need to know the exact the thermoelectric properties of the substrate, and this avoids the need for substrate removal to separate the thin and substrate effects.

Figure 4.3 shows an example of our Seebeck coefficient measurement results on sample HA99.103 and HA99.106. The Seebeck coefficient is the slope of the curve. Sample HA99.103 is a 200 × (5nm $Si_{0.7}Ge_{0.3}$/10nm Si) p-type superlattice, its measured boron doping is 6×10^{19} cm^{-3} (through Hall measurement). Its Seebeck coefficient is 198 μV/K. Sample HA99.106 is a 100 × (10nm $Si_{0.89}Ge_{0.10}C_{0.01}$/10nm Si) n-type superlattice, its measured Sb doping is 1×10^{19} cm^{-3}. Its Seebeck coefficient is –380 μV/K. Both materials were grown with MBE on silicon substrates. More Seebeck coefficient measurement results will be listed in Section 4.3.

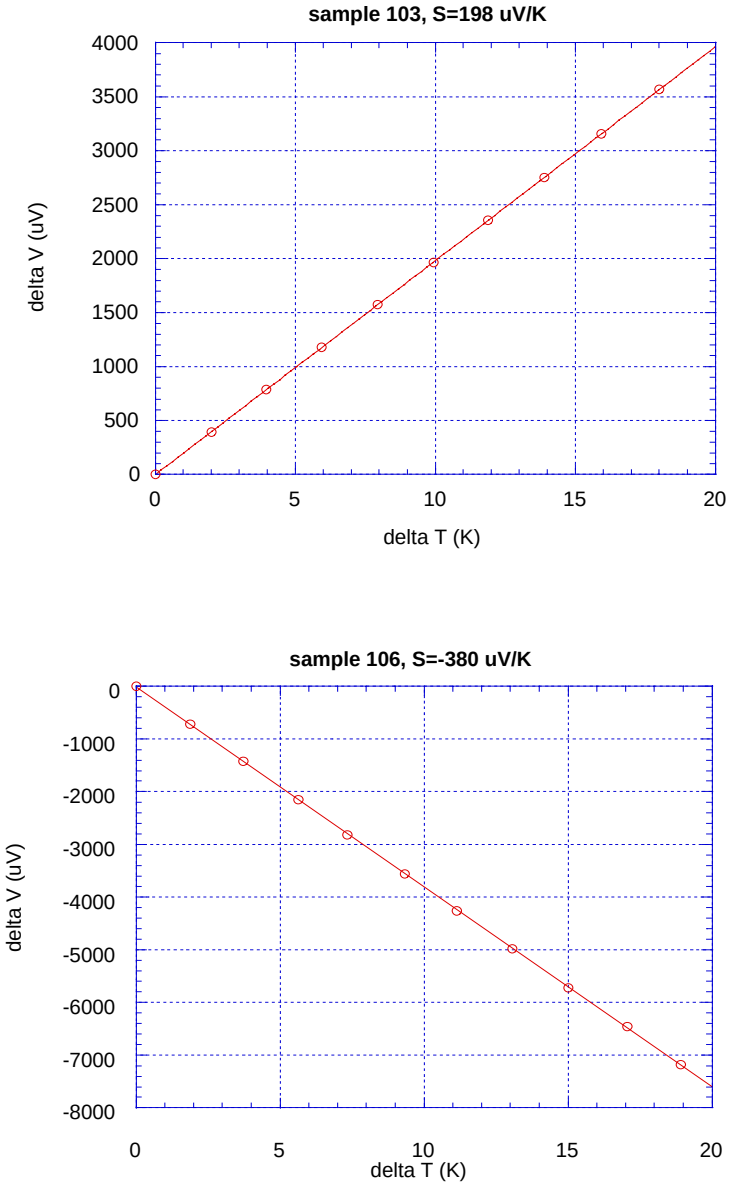


Figure 4.3 Seebeck coefficient measurement result on samples HA99.103 and HA99.106. Sample HA99.103: 200 × (5nm $Si_{0.7}Ge_{0.3}$/10nm Si) superlattice, p-type, $p=6\times10^{19}$ cm^{-3}; Sample HA99.106: 100 × (10nm $Si_{0.89}Ge_{0.10}C_{0.01}$/10nm Si) n-type superlattice, $n=1\times10^{19}$ cm^{-3}.

4.2 Electrical conductivity measurement

A thermoelectric cooler is an electronic device in which thermoelectric cooling is coming with joule heating. To have efficient thermoelectric cooling, high electrical conductivity is required for the thermoelectric materials to minimize the joule heating. As shown in Equation 4.1, the thermoelectric figure of merit is proportional to the electrical conductivity. In semiconductor, the electrical conductivity σ can be expressed as following:

$$\sigma = eN\mu \tag{4.11}$$

where e is the electron charge (1.6×10^{-19} C), N is the doping concentration and μ is the mobility.

The common mobility measurement method is Hall measurement. To measure the mobility of thin film, we used undoped substrates. This method is valid for the mobility measurement of the in-plane direction. Mobility of cross-plane direction can be different from that of in-plane direction. At this time, we don't have a good way to measure the cross-plane mobility of thin films.

4.3 Experimental results on thermoelectric power factor

Both the electrical conductivity and the Seebeck coefficient depend on the material doping concentration. With increasing doping, the electrical conductivity increases, while the Seebeck coefficient decreases. The thermal electric power factor is defined as $S^2\sigma$. It is different from thermoelectric figure of merit Z just by a factor of thermal conductivity κ. The power factor is a better way to describe the over all electrical properties of a thermoelectric material than just electrical conductivity or just Seebeck coefficient.

Table 4.1 shows the experimental results of doping, mobility, Seebeck coefficient and thermoelectric power factor of some Si, SiGe and SiGeC materials. There materials were grown on semi-insulating silicon substrates with MBE in HRL Laboratory by Edward Croke. The doping and mobility were also measured by Edward Croke with Hall measurement. When the doping is very low, such as sample HA00.076, HA00.078 and HA00.089, the Seebeck coefficient and mobility is large, but the power factor is low. Low doping is generally not suitable for microcooler applications. Good thermal electric power factor requires the doping in the order of 10^{19} or 10^{20} cm^{-3}. For the materials in Table 4.1, heavily doped silicon samples (HA99.072 and HA99.073) show the highest power factor, but since their thermal conductivity

Table 4.1 Measured doping, mobility, Seebeck coefficient and thermoelectric power factor. All materials were grown by MBE.

sample number	type	structure	doping (cm^{-3})	$\mu(cm^2/Vs)$	S ($\mu V/K$)	$S^2\sigma$ (W/cmK^2)
HA99.072	n	0.25μm Si	1.04×10^{20}	81.48	-210	5.98×10^{-5}
HA99.073	p	0.25μm Si	2.10×10^{20}	30.81	330	1.13×10^{-4}
HA99.101	n	3μm 200×(50Å $Si_{0.7}Ge_{0.3}$/100Å Si)	3.42×10^{19}	58.05	-210	1.40×10^{-5}
HA99.103	p	3μm 200×(50Å $Si_{0.7}Ge_{0.3}$/100Å Si)	6.47×10^{19}	28.61	200	1.18×10^{-5}
HA99.104	n	2.0μm $Si_{0.89}Ge_{0.1}C_{0.01}$	4.31×10^{18}	80.53	-470	1.23×10^{-5}
HA99.105	n	2μm 100×(100Å $Si_{0.89}Ge_{0.10}C_{0.01}$/100 Å Si)	1.86×10^{19}	79.76	-340	2.74×10^{-5}
HA99.106	n	2μm 100×(100Å $Si_{0.89}Ge_{0.10}C_{0.01}$/100 Å Si)	1.03×10^{19}	93.06	-380	2.21×10^{-5}
HA00.076	n-	1μm $Si_{0.8}Ge_{0.2}$	9.7×10^{14}	136.6	-5750	7.01×10^{-7}
HA00.077	n	1μm $Si_{0.8}Ge_{0.2}$	6.2×10^{19}	62.8	-210	2.75×10^{-5}
HA00.078	n-	1μm 67×(120Å $Si_{0.75}Ge_{0.25}$/30 Å Si)	2.8×10^{15}	530.5	-3750	3.34×10^{-6}
HA00.080	n	1μm 67×(120Å $Si_{0.75}Ge_{0.25}$/30 Å Si)	6.8×10^{19}	70.5	-160	1.96×10^{-5}
HA00.081	p	1μm $Si_{0.8}Ge_{0.2}$	7.9×10^{19}	28.8	210	1.61×10^{-5}
HA00.082	p	1μm 67×(120Å $Si_{0.75}Ge_{0.25}$/30Å Si)	8.0×10^{19}	29.7	180	1.23×10^{-5}
HA00.083	p	3μm graded $Si_{0.8}Ge_{0.2}$ buffer	3.0×10^{19}	35.0	330	1.83×10^{-5}
HA00.089	n-	0.968μm $Si_{0.8925}Ge_{0.1}C_{0.0075}$	9.0×10^{14}	205	-4630	6.33×10^{-7}
HA00.090	p	0.613μm $Si_{0.8925}Ge_{0.1}C_{0.0075}$	6.3×10^{19}	10.6	230	5.65×10^{-6}

is 10 to 30 times larger than that of SiGe and SiGeC materials, their figure of merits are lower than those SiGe and SiGeC samples with power factor in the order of 10^{-5} W/cmK^2.

4.4 Thermal conductivity

Thermal conductivity is another key parameter for thermoelectric materials. During the cooling operation of thermoelectric coolers, there is a heat flow from the hot sides to the cooling side of the cooler through thermal conduction. This heat conduction reduces the cooler performance. As shown in Equation 4.2, thermoelectric figure of merit is inversely proportional to the thermal conductivity. Low thermal conductivity is highly desirable for thermoelectric applications.

The thermal conductivity κ of solids includes two parts: lattice component κ_{latt} and electronic component κ_{el}.

$$\kappa = \kappa_{latt} + \kappa_{el} \qquad (4.12)$$

The lattice thermal conduction comes from phonons (lattice vibration), while the electronic thermal conduction comes from free movable electrons (or holes). The electronic thermal conductivity κ_{el} is related to the electrical conductivity σ through the Wiedemann-Franz law [4]:

$$\kappa_{el} = L_0 T \sigma \tag{4.13}$$

where $L_0 = \frac{\pi^2}{3}(\frac{k_B}{e})^2 = 2.45\times10^{-8}\ V^2/K^2$ is the Lorentz number.

The electronic thermal conductivity increases with increasing the electrical conductivity. For metals, the electronic thermal conductivity is usually much larger than the lattice thermal conductivity; for insulators and semiconductors, the lattice component usually dominates the material's thermal conductivity.

The thermal conductivity of solids is usually determined by measuring the temperature gradient produced by a steady flow of heat in a one-dimensional geometry. This can be achieved relatively easily on large bulk materials. [3] For thin film materials, the thermal conductivity measurement needs some special techniques, such as AC calorimetric method [5-7], 3ω method [8-10] and optical pump-and-probe technique [11-14]. 3ω method is a relatively direct way to measure thermal conductivity, while AC calorimetric method and

optical pump-and-probe method actually measure the thermal diffusivity. Thermal conductivity κ is related to the thermal diffusivity D through the following relation:

$$\kappa = \rho c_v D \tag{4.14}$$

where ρ is material density and c_v is specific heat.

In this section we will discuss the three commonly used thin film thermal conductivity methods: AC calorimetric method, optical pump-probe method and 3ϖ method.

4.4.1 AC calorimetric method

AC calorimetric method is usually used for measuring the thin film or superlattice thermal conductivity at the in-plane direction. A schematic diagram of this method is shown in Figure 4.4.

A modulated uniform light beam $Qe^{i\omega t}$ is applied perpendicularly to the surface of the thin film sample that is partly shadowed by a mask moving along the x direction. The light energy absorbed by the sample produces a temperature wave that propagates along the sample length. A fine thermocouple with a diameter smaller than the thermal diffusion length is

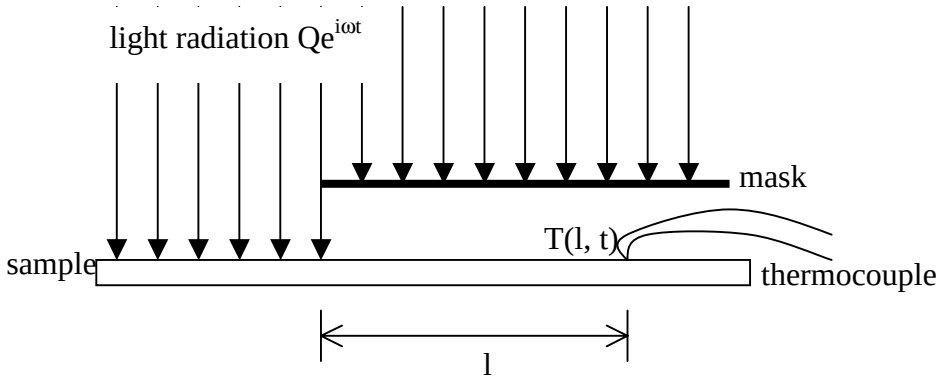


Figure 4.4 Schematic diagram of the AC calorimetric method

attached to a point of the sample surface lying under the mask. The AC temperature amplitude |T(l,t)| and phase arg[T(l,t)] can be measured as a function of the distance l. For the one-dimensional model (no heat conduction component perpendicular to the film surface), the thermal diffusivity D along the sample length can be obtained as follows [5]:

Amplitude method:

$$D = \frac{1}{2}\omega\left[\frac{d \ln |T(l,t)|}{dl}\right]^{-2} \qquad (4.15)$$

Phase method:

$$D = \frac{1}{2}\omega\{\frac{d \arg[T(l,t)]}{dl}\} \quad (4.16)$$

The one-dimensional model requires the sample thickness d<0.1/k, where k is the thermal decay constant $(\omega/2D)^{1/2}$. The thermal diffusivity measured here is for the in-plane direction of the thin film, thus the thermal conductivity measured here is also for the in-plane direction.

In this measurement, the ac temperature is observed using a lock-in amplifier with which, notwithstanding the periodic deformation in the shape, only the fundamental sine-wave component is detected. Therefore, the deformation of waves does not affect the measurement at all.

This method can also be applied to a multiplayer material as far as the following condition is satisfied:

$$k_i d_i < 1 \quad (4.17)$$

where k_i means k of the ith layer and d_i is the thickness of the ith layer. Under the condition of Eq. (4.17), we can obtain the thermal diffusivity of such a composite material. The overall thermal diffusivity is given as

$$D = \Sigma c_i D_i d_i / \Sigma_i d_i \quad (4.18)$$

where c_i and D_i are c and D for the ith layer, respectively.

In the case where a sample is not optically opaque, the surface of the sample should be coated to absorb the optical energy at the surface.

Since the microcooler structure in this work mainly use cross-plane heat transport, the cross-plane thermal conductivity measurement is needed. Optical pump-probe method and 3ϖ method were used in our thermal conductivity measurements for the cross-plane direction.

4.4.2 Optical pump-and-probe method

The optical pump-and-probe technique has been used in many optical and electrical characterization applications. Capinski and Maris applied this method in thin film thermal conductivity measurement [11-14]. As shown in Figure 4.5(a), a opaque thin film (e.g. aluminum) is deposited as the transducer on the sample (e.g. superlattice) to be measured. The pump laser pulse creates a sudden temperature increase of the metal film. The temperature cools down as the heat dissipates through the sample. The temperature change causes a proportional change in the optical reflectivity. This change is measured by means of a time-delayed probe pulse that is focused onto the same area of sample as the pump pulse. From the cooling curve, as shown in Figure 4.5 (b), the thermal diffusivity can be calculated from a numerical simulation of the

heat flow. If the specific heat is known, the thermal conductivity value can be obtained.

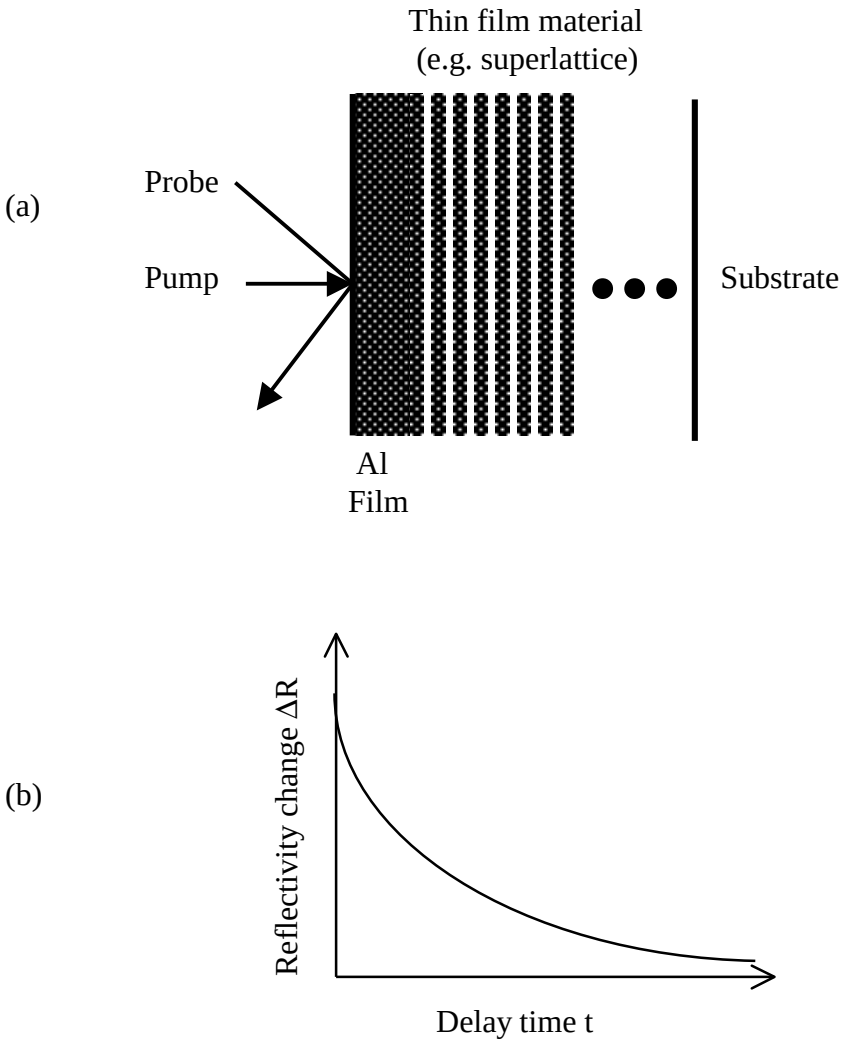


Figure 4.5 Schematic diagram of pump-and-probe method. (a) experiment (b) result.

There are two main reasons for using the transducer thin film, such as Al film, instead of letting the pump laser directly hitting the sample. First, this is to make sure the pump light is absorbed at the surface, solving non-opaque material problem. Second, even if the material is opaque to the pump light, the pump light may cause some electron excitation in the material, thus cause changes in its reflectivity [15]. The use of the Al film as thermal transducer can avoid this problem and make reflectivity change mainly coming from the temperature change. The schematic diagram of our experimental setup is shown in Figure 4.6.

We used a mode-locked Ti:sapphire laser pumped by a Ar ion laser as the light source. The laser wavelength is centered at around 800 nm, and its pulse width and repetition rate are 100 fs and 105 MHz respectively. The laser beam is split into pump light and probe light by a beam splitter. The pump light is modulated by an acousto-optic modulator (AOM) and a mechanical chopper. The probe light is delayed by the delay stage. The delay time is controlled by the delay stage position which determines the optical pass length of the probe light. The pump light and probe light were focused on the same spot of the sample. The reflected beam of the probe light went to a photo detector to measure the reflectivity.

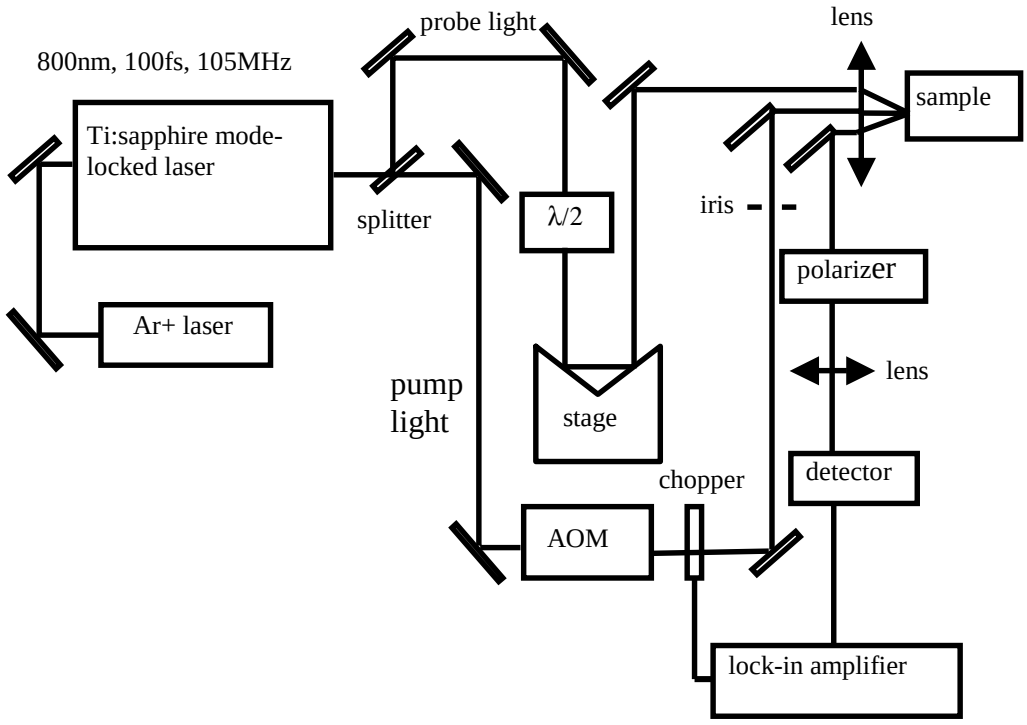


Figure 4.6 The experiment set up for the pump-and-probe measurement.

The pump beam can raise the sample temperature a few degrees. The reflectivity change of Al films is on the order 10^{-5}. So this is a very small signal measurement. The AOM, chopper and lock-in amplifier were used to increase the signal to noise ratio. To prevent to pump light going into the detector, a half wave plate ($\lambda/2$) was used to rotate the polarization of the probe light by 90° and a polarizer was used in front of the detector to filter out the pump light and only let reflected probe light into the photodetector.

The laser beam spot size is usually 20~30 μm, while the thin film material thickness is on the order of microns. Thus, the heat dissipation through the thin film sample is mainly through the cross-plane direction. Therefore, the thermal diffusivity and thermal conductivity measured with the pump-and-probe method is for the cross-plane direction of the thin film.

Figure 4.7 shows the experimental results on three samples: bulk InP, 1 μm InGaAs on InP substrate and 1 μm InGaAs/InP superlattice 40×(18nm InGaAs/7nm InP) on InP substrate. The InGaAs and InGaAs/InP were grown on InP substrates by metal-organic chemical vapor deposition (MOCVD). All the samples were coated with 50 nm Al through thermal evaporation. There are some bump features in the first 50 ps, which come from the acoustic echoes between the Al surface and Al/semiconductor interface. Since the delay stage used in this experiment has a maximum travel length of only a few centimeters, we could only measure the reflectivity change up to a delay time of 140 ps. This time is too short to get the accurate decay rate of the reflectivity, thus we can't get the thermal diffusivity quantitatively. Qualitatively, from Figure 4.7, the InGaAs/InP superlattice has smaller thermal diffusivity than InGaAs, and InGaAs has smaller thermal diffusivity than bulk InP. This is confirmed with our thermal conductivity measurements on these samples with 3ω method [16, 17].

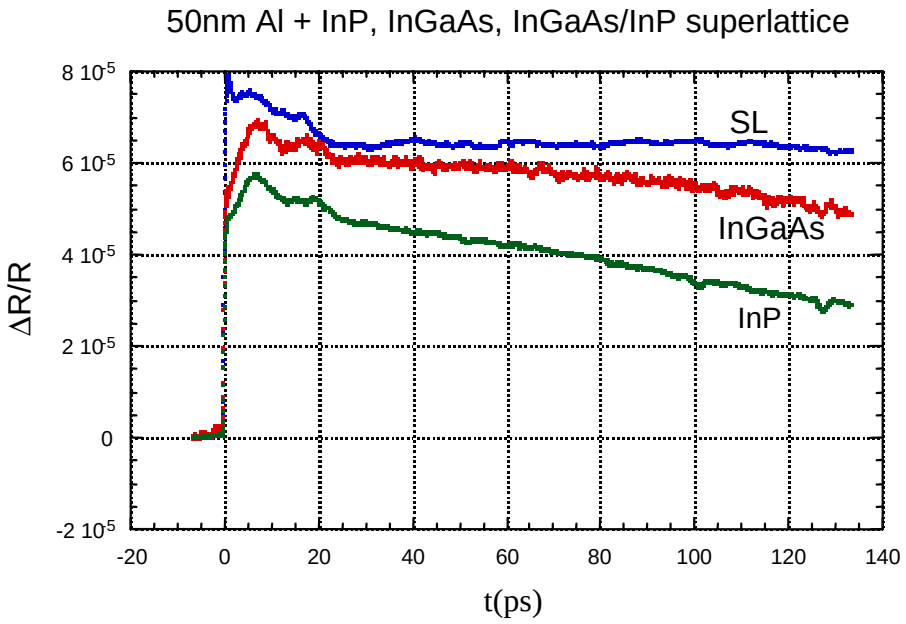


Figure 4.7 Experimental results for the reflectivity change as a function of time. The samples are InP, InGaAs and InGaAs/InP superlattice 40×(18nm InGaAs/7nm InP). They are all coated with 50 nm Al thin film. The bump features in the first 50ps come from the acoustic echoes between the Al surface and Al/semiconductor interface.

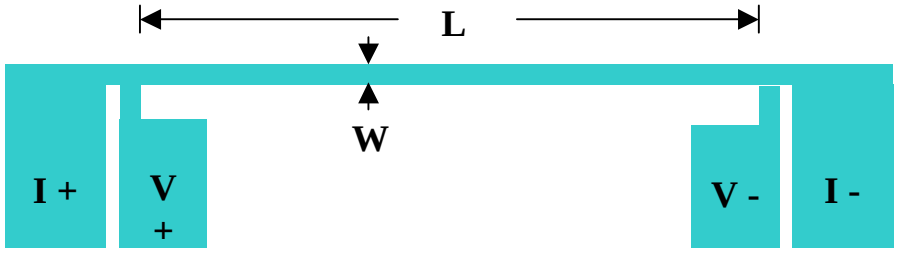
To get the quantitative thermal diffusivity, a longer delay time in the order of nano-seconds is needed in this pump-and-probe measurement. This requires the delay stage's travel length up to 1 meter. However, long travel length makes the measurement very challenging. One crucial requirement of the measurement is to keep good overlap between the pump beam and probe beam at the focusing spot on the surface of the sample. With the delay stage's travel length increasing, even a small misalignment of the optical before the

translation stage will cause the probe beam spot position change on the sample surface. In addition, the divergence of the laser beam may alter the size of the probe spot as the delay is changed. It has also very high requirements on the delay stage's straightness, flatness and the smoothness of its movement. One way to solve this problem is to use single mode fibers to send the probe beam to the sample [12]. It is based on the idea that if designed properly, the intensity distribution of the light transmitted through a fiber will solely depend on the modal properties of the fiber and thus independent of the characteristics of the light beam when it is launched into the fiber.

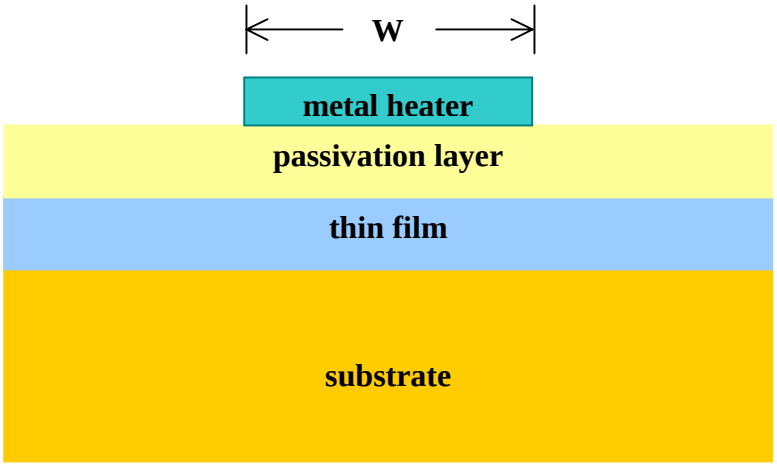
The pump-and-probe method measures thermal diffusivity. To get the thermal conductivity, the specific heat is needed also. For thin film materials, their specific heat is usually estimated because no measured values available. So, their bulk material values are often used to calculate thermal conductivity from thermal diffusivity.

4.4.3 3ω method

The cross-plane thermal conductivity of thin films can be measured by 3ω method developed by Cahill and coworkers [8-10]. In this method, as shown in Figure 4.8, a metal wire is deposited onto the film to function as a heater and a temperature sensor. When a current is sent into the heater, its temperature will



(a)



(b)

Figure 4.8 The heater/senor structure used in 3ω method for thermal conductivity measurement. (a) top view (b) cross-section view.

increase and the temperature increase amount depends on the materials' thermal conductivity and layer thickness, etc. This temperature increase can be measured from the metal wire's electrical resistance change since the electrical resistivity is a function of temperature. Thermal conductivity can be calculated

from the temperature change knowing the heat load. However, this temperature change is usually a very small signal. To measure the thermal conductivity more accurately, 3ω method is generally used: A sinusoidal current at the angular frequency ω is passed through the wire, which generates a 2ω heating source and a corresponding 2ω heater dependents linearly on temperature, there is also a 2ω variation in the resistance of a heater. Such a 2ω resistance variation, in combination with the 1ω heating current, induces a 3ω voltage component is detected by a lock-in amplifier. To reject the large 1ω heating voltage, a Wheatstone bridge is used to cancel the dc voltage before the signal is sent into a lock-in amplifier. The schematic diagram of the equipment set up is shown in Figure 4.9. This method can be used to measure the thermal conductivity of both bulk and thin film materials. For thin film materials with much lower thermal conductivity than that of the substrate, the thin film works as a extra thermal resistance in addition to the substrate, thus it will cause an temperature drop ΔT on thin film.

$$Q = \kappa_f \Delta T / d_f \tag{4.19}$$

$$\kappa_f = d_f Q / \Delta T \tag{4.20}$$

where Q is the heat load, κ_f is the thermal conductivity of the thin film and d_f is the thickness of the thin film.

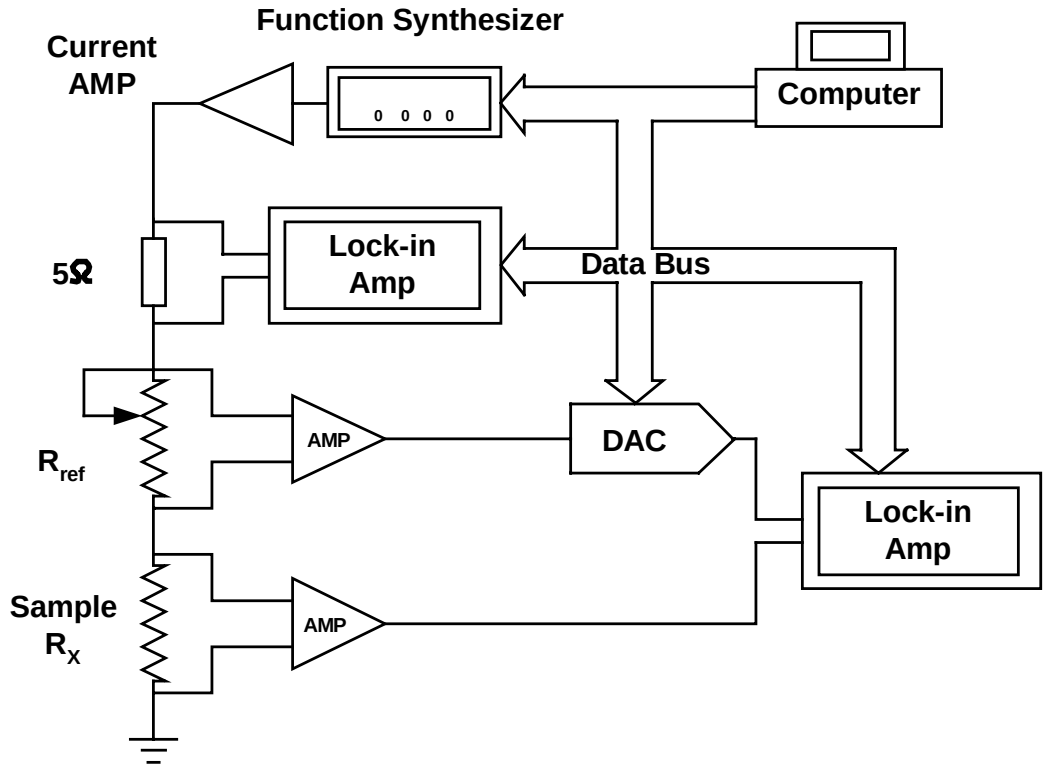


Figure 4.9 Schematic diagram of the equipment set up for the 3ω measurement. (From Lou [18])

To electrically isolate the heater and the sample, a passivation layer, such as SiO_2 or SiN_x can be deposited on the sample. The following are some of the procedures we used for the 3ω thermal conductivity measurement:

a. Cleave the sample to around 8×8 mm^2.
b. Deposit 100 nm SiO_2 or SiN_x on the sample with PECVD to electrically isolate the sample and the heater/sensor.
c. Pattern the heater/sensor patterns on to the sample with standard photolithography.
d. Deposit 20 nm Ti as the adhesion layer and 500 nm Au as the heater/sensor by e-beam evaporation or plasma sputtering.
e. Remove the photo resist and unwanted metal films by lift-off technique.
f. Package and wire bond the sample for testing.
g. Measure the resistance of the heater/censor at different temperatures to get its temperature coefficient of resistivity.
h. Perform the 3ω measurement for thermal conductivity.

In the 3ω method, the temperature rise of the metal wire is usually measured over a wide range of frequencies. Cahill showed that the temperature rise has a linear relation with the log of frequency and the substrate thermal conductivity can be obtained from the slope of the curve using [8]

$$K_{sub} = \frac{V^3 \ln(f_2 / f_1)}{4\pi L R^2 (V_{3\omega,1} - V_{3\omega,2})} \frac{dR}{dT} \tag{4.21}$$

where V is the voltage across the metal line at ω, L is the length of the metal line, R is the resistance of the metal line, $V_{3\omega,1}$ and $V_{3\omega,2}$ are the in-phase 3ω voltages at frequency f_1 and f_2 respectively, dR/dT is the resistance temperature coefficient of the metal line. Therefore, the 3ω method can measure the thermal conductivities of both the thin film material and the substrate or bulk material.

4.4.4 Experimental results of 3ω measurement

Unlike AC calorimetric method and optical pump-and-probe method which measure the thermal diffusivity, 3ω method measures the thermal conductivity directly both for thin film and bulk materials.

Our 3ω measurement were done with the 3ω setup, shown in Figure 4.9, in Prof. Clarke's group in UCSB. The metal wire pattern is shown in Figure 4.8 (a). Its length L is 760 nm or 670 nm, and its width W is 4 μm, 10 μm, 16 μm and 25 μm respectively for different patterns. The metal wires were made of 20 nm Ti and 500 nm Au. The measured resistant temperature coefficient $\frac{dR}{RdT}$ was in the range 0.026 to 0.031 K^{-1} for the metal wires deposited with e-beam evaporation. A passivation layer of 100 nm SiO_2 or SiN_x was used to prevent current leakage from the heater to the sample, as shown in Figure 4.8.

If the thermal conductivities of the substrate and the passivation layer is known, the thermal conductivity of the thin film layer can be obtained from measuring the temperature increase of the heater with a certain input power. For our SiGe samples, since the lattice constant of SiGe is larger than that of silicon, a buffer layer is grown before the SiGe layers. The thermal conductivity of the buffer layer is not known. Here, we used two samples, one original sample and one with the thin film layer etched off, to determine the temperature drop on the thin film. As an example, Figure 4.10 shows the 3ω measurement result on sample HA00.076. HA00.076 is 1 μm $Si_{0.8}Ge_{0.2}$ grown on 0.15 μm SiGe buffer layer on SOI substrate. Its thermal conductivity is calculated to be 5.9 W/mK form the measured $\Delta T_f/Q$. The substrate's thermal conductivity is calculated to be 144 W/mK from the lines' slope in Figure 4.10, close to the book value 150 W/mK [19].

Our measured thermal conductivities on SiGe and SiGeC thin film samples are listed in Table 4.2. They were grown with molecular beam epitaxy (MBE) in HRL Laboratory. The thermal conductivity was measured on 760×16 μm^2 heater pattern with 3ω method.

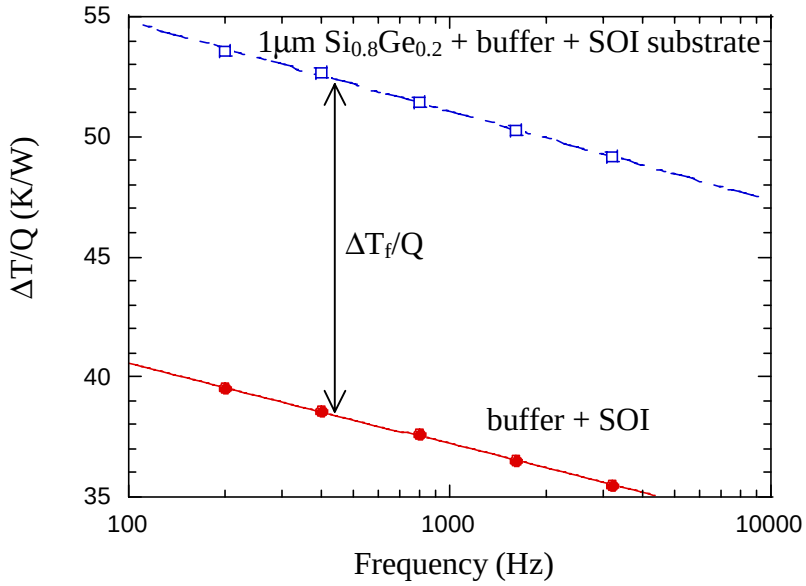


Figure 4.10 Measured temperature oscillation on sample HA00.76 (1 μm $Si_{0.8}Ge_{0.2}$) and its buffer sample. The metal heater size is 760 × 16 μm^2. The passivation layer is 10 nm SiO_2. ΔT_f is corresponding to the temperature drop on the 1 μm $Si_{0.8}Ge_{0.2}$.

4.4.5 Discussions

Low thermal conductivity is required for thermoelectric materials since their TE figure of merit is inversely proportional to the thermal conductivity. Si and Ge have relatively high thermal conductivities and their figures of merit are low. Phonon alloy scattering is an effective way to reduce thermal conductivity. Superlattice structure can be another way to reduce thermal conductivity.

Table 4.2 Measured thermal conductivity of MBE grown SiGe and SiGeC samples.

sample #	substrate	buffer	structure	doping (cm^{-3})	κ (W/mK)
HA99.089	n-type Si		2μm 100×(10nm Si/10nm $Si_{0.89}Ge_{0.1}C_{0.01}$)	$Nd=2\times10^{19}$	8.4
HA99.091	n-type Si		2μm $Si_{0.89}Ge_{0.1}C_{0.01}$	$Nd=6\times10^{19}$	6.0
HA00.007	p-type Si	2μm SiGe/SiGeC	3μm 400×(5nm Si/2.5nm $Si_{0.7}Ge_{0.3)}$	$Na=5\times10^{19}$	9.2
HA00.008	p-type Si	2μm SiGe/SiGeC	3μm 667×(3nm Si/1.5nm $Si_{0.7}Ge_{0.3)}$	$Na=5\times10^{19}$	10.8
HA00.016	p-type Si	2μm SiGe/SiGeC	3μm 100×(20nm Si/10 nm $Si_{0.7}Ge_{0.3)}$	$Na=5\times10^{19}$	13.5
HA00.037	p-type Si	2μm SiGe/SiGeC	3μm 200×(10nm Si/5nm $Si_{0.7}Ge_{0.3)}$	$Na=5\times10^{19}$	10.7
HA00.076	SOI	0.15μm SiGe	1μm $Si_{0.8}Ge_{0.2}$	$Nd=9.7\times10^{14}$	5.9

Figure 4.11 shows the measured the thermal conductivities of $Si/Si_{0.7}Ge_{0.3}$ superlattices with difference periods. The samples include HA00.016 100 × (20nm Si/10nm $Si_{0.7}Ge_{o.3}$) superlattice, HA00.37 200 × (10nm Si/5nm $Si_{0.7}Ge_{0.3}$) superlattice, HA00.107 400 × (5nm Si/2.5nm $Si_{0.7}Ge_{0.3}$) superlattice, HA00.108 667 × (3nm Si/1.5nm $Si_{0.7}Ge_{0.3}$) superlattice and HA00.043

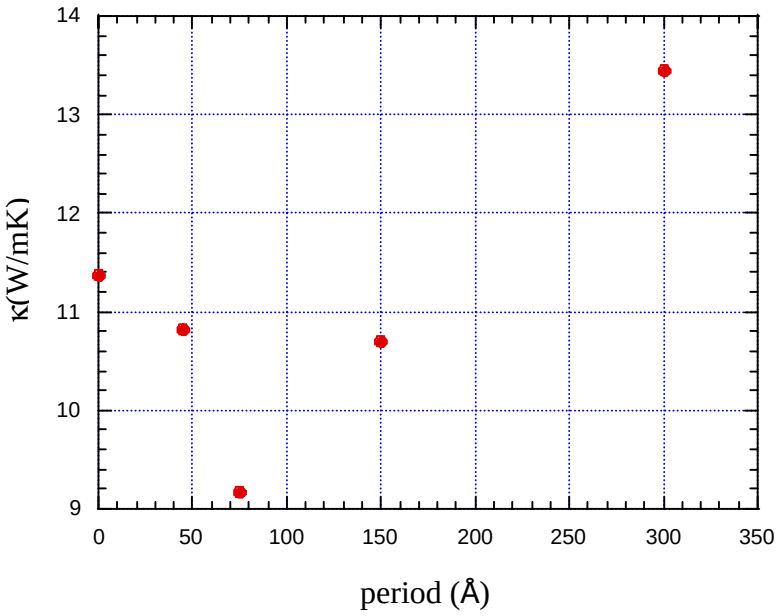


Figure 4.11 Measured thermal conductivity of Si/$Si_{0.7}Ge_{0.3}$ superlattices with different periods. The average composition of the samples are corresponding to $Si_{0.9}Ge_{0.1}$, and the data point of 0 period is for the $Si_{0.9}Ge_{0.1}$ alloy sample.

$Si_{0.9}Ge_{0.1}$ alloy. The superlattices here are composed of Si and $Si_{0.7}Ge_{0.3}$ layers whose thickness ratio is 2. Their average composition is corresponding to $Si_{0.9}Ge_{0.1}$, so $Si_{0.9}Ge_{0.1}$ alloy material is included in the figure for comparison.

For superlattice, if we ignore the interface effects, its thermal conductivity can be calculated with the average of the two materials that the superlattice is composed of. It can be easily shown that the average thermal conductivity has following relations with its individual layers:

For the in-plane direction,

$$\kappa_{ave} = \frac{d_1\kappa_1 + d_2\kappa_2}{d_1 + d_2} \tag{4.22}$$

For the cross-plane direction,

$$\kappa_{ave} = \frac{d_1 + d_2}{\frac{d_1}{\kappa_1} + \frac{d_2}{\kappa_2}} \tag{4.23}$$

where κ_{ave} is the overall thermal conductivity, κ_1 and κ_2 are the thermal conductivity of layer 1 and 2, d_1 and d_2 are the thickness of 1 and 2 respectively.

The heat transport in our 3ω measurement is mainly in the cross-plane direction. Assuming the thermal conductivity of $Si_{0.7}Ge_{0.3}$ 5.5 W/mK and the thermal conductivity of Si 150 W/mK, the average thermal conductivity can be calculated to be 15.4 W/mK for $Si/Si_{0.7}Ge_{0.3}$ (2:1) structures. As shown in Figure 4.11, the thermal conductivities of the superlattices are smaller than this average thermal conductivity showing the thermal conductivity reduction through interface scattering, etc. The thermal conductivity decreases with decreasing the superlattice period until about 75 Å, where it reached a minimum. Then, the thermal conductivity increase with decreasing the periods and it is approaching the value of alloys. (However, the differences are small for small period superlattice and SiGe alloy material and within experimental run-to-run variation. We tested samples twice and they show similar trend.)

This thermal conductivity increase may come from that phonon tunneling at very short superlattice periods. Generally, the interface scattering will lower the thermal conductivity and the more interfaces per unit length the lower thermal conductivity; however, when the layers become very thin and below the phonon's mean free path, phonon tunneling may occur, which may reduce interface scattering and increase the thermal conductivity. With further reducing the period, the superlattice will become an alloy and its thermal conductivity will be approaching to that of the alloy material too. Therefore, it is possible to have an optimal superlattice period for minimum thermal conductivity. This can also be observed on GaAs/AlAs and Si/Ge superlattices [11, 14, 20].

The $Si/Si_{0.89}Ge_{0.10}C_{0.01}$ sample also shows smaller thermal conductivity than the average of Si and $Si_{0.89}Ge_{0.10}C_{0.01}$, but still larger than that of $Si_{0.89}Ge_{0.10}C_{0.01}$. $Si_{0.89}Ge_{0.10}C_{0.01}$ shows smaller thermal conductivity than that $Si_{0.9}Ge_{0.1}$.

In summary, the thermal conductivity of SiGe and SiGeC samples tested here have over 1 order smaller thermal conductivity than that of bulk silicon; superlattices show smaller thermal conductivity than their layer average. However, the superlattices' thermal conductivities are still higher than or comparable with those of their corresponding alloy materials and the

superlattice thermal conductivity reduction in SiGe/Si and SiGeC/Si superlattice system is not as large as that in Si/Ge and GaAs/AlAs superlattice materials systems [11, 14, 21, 22]. One reason for this is the material difference between Si and SiGe (or SiGeC) is smaller than that between Si and Ge. Different materials have different phonon impedance. The larger phonon impedance mismatch, the stronger phonon scattering at the interface. To minimize thermal conductivity, superlattices with large phonon impedance mismatch are preferred.

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Chapter 5

SiGe/Si microcoolers

5.1 Introduction

SiGe is one of the best thermoelectric materials for high temperature applications [1, 2]. Figure 3.1 shows the temperature dependence of its figure of merit along with some other common thermoelectric materials. Its figure of merit increases with temperature until about 1100 K. Its maximum ZT is about 1 at 1000 K and 0.12 at room temperature. Its main thermoelectric application has been in power generation at high temperatures. SiGe radioisotope thermoelectric generators (RTGs) have been used in spacecrafts like Voyager and Galileo [3-6]. Recently, SiGe were also used to convert the waste heat in the exhaust gas of automobiles into electricity [7]. Both the SiGe RTGs and energy converters in automobiles generate electricity from large temperature difference either caused by nuclear reactors or gasoline engines, and they all work at high temperatures to maximize their efficiency.

However, there is not much work on SiGe thermoelectric coolers reported since most coolers are for room temperature or low temperature applications.

At those temperature ranges, Bi_2Te_3 and other telluride materials have much better dimensionless figure of merit ZT than SiGe, thus higher cooling performance than that of SiGe. There has been a lot of efforts to improve the ZT of SiGe, like small grain materials, SiGe:P, etc [8-10]. The idea of small grain materials is to reduce the thermal conductivity. The thermal conductivity κ can be express as [1]

$$\kappa = \frac{1}{3} vcl \qquad (5.1)$$

where v is the phonon velocity, c is the heat capacitance and l is the phonon mean free path. If we can reduce the phonon mean free pass, the thermal conductivity can be reduced accordingly. Small grain materials are used to reduce the thermal conductivity of SiGe materials. Experimentally, lower thermal conductivity was measured on the small grain SiGe materials. However, its electrical conductivity gets lower when the grain gets smaller because of more scattering at the grain boundaries. The overall figure of merit doesn't improve much.

With the rapid development of superlattice thermoelectrics, there has been renewed interest on thermoelectric materials. The use of quantum-well structures to increase ZT was proposed by Hicks and Dresselhaus in 1993 [11,

12]. Since then much work has been done in the study of superlattice thermoelectric properties. Both theoretical and experimental results show that signification ZT enhancement could be achieved with superlattice structures. The physical origins of the ZT increase in superlattices include thermal conductivity reduction from phonon interface scattering, enhanced density of electron states due to the reduced dimensionality, selectively removal of hot carriers through thermionic emission, etc. SiGe/Si and Si/Ge superlattices are good candidates to take advantage of these progresses in superlattice thermoelectrics [11-28]. Through carrier pocket engineering, ZT up to 0.96 and 1.25 was predicted on (111) oriented strain-symmetrized and strain-nonsymmetrized Si/Ge superlattices at 300 K [27].

The most attractive property of SiGe thermoelectric refrigeration is its potential for monolithic integration with silicon microelectronics. SiGe is an important microelectronic material. It has been used in heterostructure bipolar transistors. Its processing is comparable with standard integrated circuit (IC) technology. Among the common microelectronic materials, such as silicon, GaAs and InP, SiGe has the highest ZT even at room temperature.

In this chapter, we will present our experimental results on SiGe and SiGe/Si superlattice microcoolers. Here we use cross-plane electrical and thermal transport. Superlattice structures can enhance the cooler performance

by reducing the thermal conductivity between the hot and the cold junctions, and by selective emission of hot carriers above the barrier layers in the thermionic emission process.

5.2. Material and device structure

In order to make monolithically integrated SiGe/Si microcoolers, we used epitaxial SiGe and SiGe/Si superlattices grown on silicon, instead of bulk SiGe materials.

5.2.1 SiGe/Si superlattice structure

Like silicon and germanium, $Si_{1-x}Ge_x$ has a diamond crystal structure. Its lattice constant is larger than that of silicon, as shown in Figure 5.1 [29].

The lattice constant of SiGe can be expressed with Vegard's law:

$$a_{SiGe} = a_{Si} (1-x) + a_{Ge} x \qquad (5.2)$$

where a_{Si} = 0.5431 nm and a_{Ge} = 0.5658 nm are the lattice constants of Si and Ge respectively.

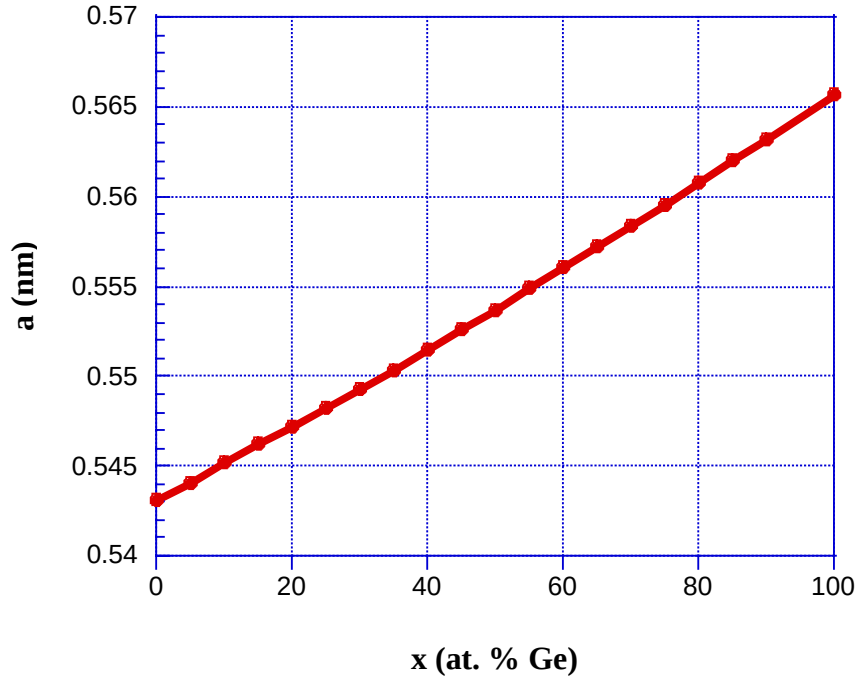


Figure 5.1 Lattice constant a(x) of $Si_{1-x}Ge_x$ alloys for x from 0 to 100 at.%[29].

When SiGe is grown on silicon, it will get strained due to their lattice mismatch. Dislocations will be generated if the thickness is larger than the critical thickness. To grow high quality thick SiGe or SiGe/Si superlattice on silicon, a buffer layer is required to gradually change the lattice constant from that of silicon to that of the SiGe or the average lattice constant of the SiGe/Si superlattice.

Figure 5.2 shows the sample structure of sample HA99.071 as an example for our cooler sample structures. It is a p-type SiGe/Si superlattice sample, its epitaxy layers include SiGe/SiGeC buffer layer, SiGe/Si superlattice and SiGe cap layer. Other microcooler samples have similar material structures.

cap layer	0.25 μm $Si_{0.9}Ge_{o.1}$ Na > 1×10^{20} cm^{-3}
	0.25 μm $Si_{0.9}Ge_{o.1}$ Na = 5×10^{19} cm^{-3}
superlattice	3 μm 200 × (10 nm Si / 5 nm $Si_{0.7}Ge_{0.3}$) superlattice Na = 5×10^{19} cm^{-3}
buffer layer	1 μm $Si_{0.9}Ge_{o.1}$ Na = 5×10^{19} cm^{-3}
	1 μm 5 × (150 nm $Si_{0.9}Ge_{0.1}$ / 5 nm $Si_{0.845}Ge_{0.150}C_{0.005}$) Na = 5×10^{19} cm^{-3}
substrate	p-type (001) silicon substrate ρ: 0.001~0.006 Ωcm

Figure 5.2 Material strucutre of p-type SiGe/Si superlattice sample HA99.071.

5.2.2 Basic SiGe/Si microcooler structure

There are two main methods to make integrated thin film microcoolers on silicon. One is to use in-plane current and heat transport, and the other is to use cross-plane transport. The in-plane cooler device structure is described in refrence [30-34]. For this kind of device, the thin film TE material is deposited on SiO_2 or SiN_x membrances and the substrate silicon is removed beneath the cooler in order to reduce the heat conduction between the cooler's cold and hot sides. A reported device structure with in-plane thermal and electrical transport is shown in Figure 5.3 [34]. The cooling power is small due to the small cross section area of the TE film.

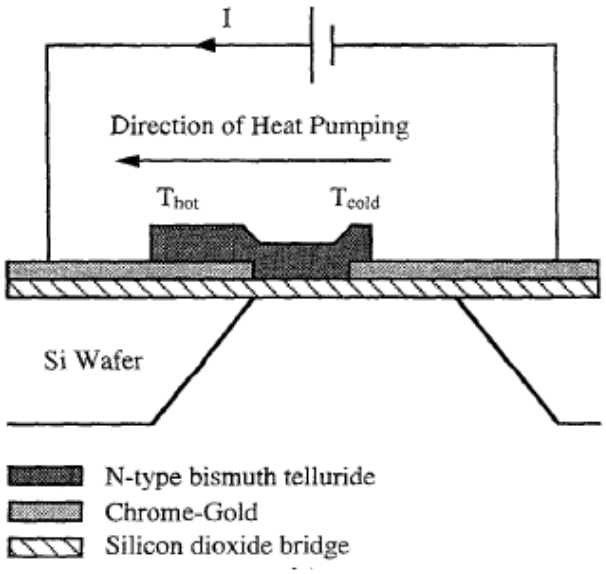


Figure 5.3 Reported microcooler structure with in-plane heat and electric transport. From Shafai [34].

The other microcooler structure is to use cross-plane thermal and electrical transport. One of the main advatages of this method is its large cooling power density as we discussed in Chapters 1 and 2. In this thesis, we use the cross-plane transport device structure. With across-plane electrical and thermal transport in superlattice structures, it is possible to ehance the thermoelectric cooling by selectively removing hot carriers through thermionic emission and by thermal conductivity reduction through phonon scattering at the superlattices interfaces. A basic single element SiGe/Si superlattice microcooler structure with cross-pane transport is shown in Figure 5.4. Its difference from conventional sigle element TE cooler is that the the bottom contact metal is on the buffer layer instead of directly at the bottom side of the SiGe/Si superlattice. This is to try to make the device processing simple and easy for integration with no need for substrate removal. In principle, the microcooler structure cam also be like those of conventional TE cooling using n- and p-type materials arries, which will be dissused in later section of this chapter.

5.2.3 Improved SiGe/Si microcooler structure

The basic SiGe/Si microcooler structure in Figure 5.4 is simple and so is this processing. It is good for the demo of the microcooler concept and quick

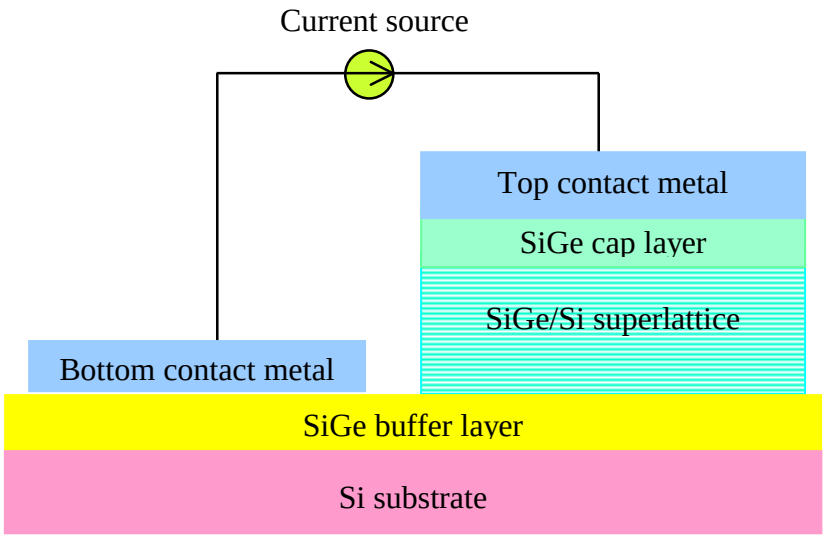


Figure 5.4 Schematic structure diagram of the basic SiGe/Si superlattice microcooler with cross-plane thermal and electrical transport.

check for both TE materials and devices. Our first SiGe/Si microcooler was fabricated with this basic structure and cooling by as much as 1.1 K at room temperature was measured [35].

The basic SiGe/Si microcooler structure also has limitations. Their metal contacts are isolated and they need some external electrical connections to send currents to them. This can be achieved by direct probing or wire bonding, which is usually no problem for large TE coolers. However, the sizes of the probes and bonding wires become relativity large for the small sizes of the microcoolers, which limits further reduction of the microcooler sizes. In

addition, the probes and bonding wires can be a large heat conduction source which degrades the cooling performance of the microcoolers. Another issue is device integration. Probe and bonding wires are not good for the integration of a large number of micro devices.

To solve these problems, the basic SiGe/Si microcooler structure can be improved by using integrated extended top metal contacts, as shown in Figure 5.5. This is similar to IC chips which use deposited metal wires for electrical connections and the wire bonding only at the I/O area for packaging. The extended top metal contact can be electrically isolated from other parts, such as the buffer layer, through a passivation layer of SiO_2 or SiN_x. Device current source can connected to the extended top metal contact without taking the small cooling area space.

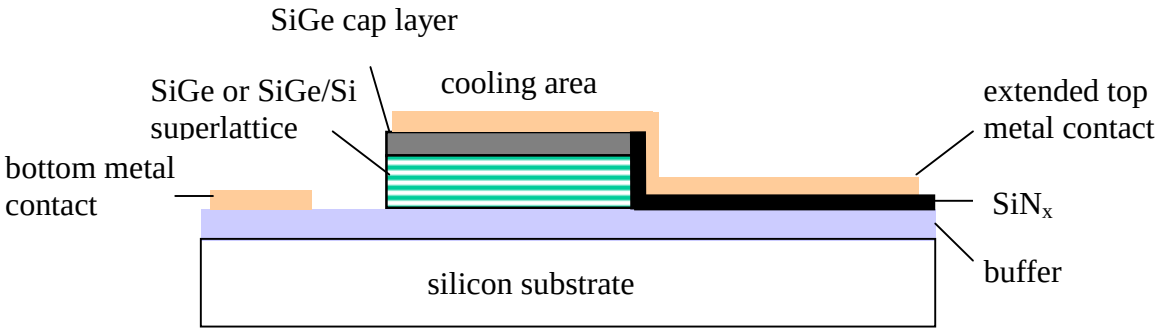


Figure 5.5 Schematic structure diagram of an improved SiGe/Si microcooler with integrated extended top metal contact.

5.2.4 SiGe/Si band structure

Band structure is an important property for semiconductor heterostructures and superlattices. By properly selecting the band offsets and doping levels in each layer, superlattices can be used to enhance thermoelectric cooling through thermionic emission.

SiGe has a smaller band gap than Si, and the band gap is strain dependent [36, 37]. Figure 5.6 shows the bandgap for $Si_{1-x}Ge_x$ measured at 90 K. It can be seen that the bandgap decreases with increasing Ge composition x and with increasing the compressive strain.

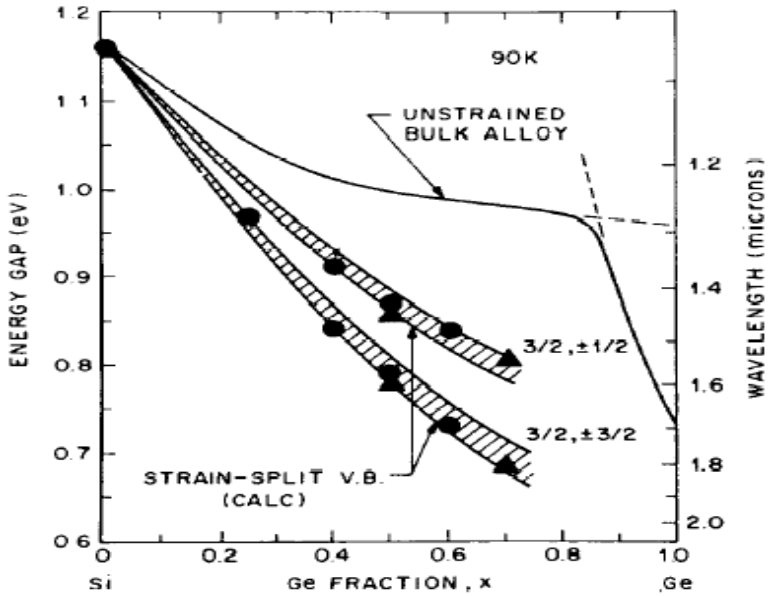
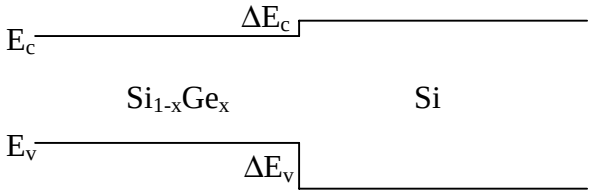
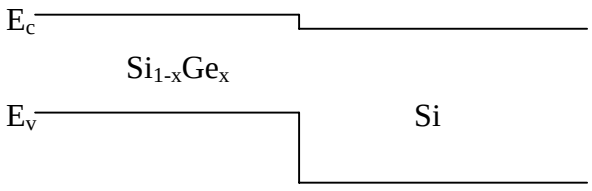


Figure 5.6 Bandgap for $Si_{1-x}Ge_x$ measured at 90 K. Top line for normal unstrained alloys. Bottom bands calculated for strained alloy layer grown on undistorted silicon. Difference between bands stems from strain splitting of the valence band energies. (From Bean [37])

The band offsets in SiGe/Si heterostructures mainly lie in the valance band and they depend on the strain level in the materials. Figure 5.7 shows the band alignment for (001) oriented SiGe/Si heterostructure. It is interesting to note that the band alignment can goes from type I to type II by the strain adjustment, and in both case the band offset is in the valence band.



(a) Strained $Si_{1-x}Ge_x$ on unstrained Si



(b) Strained $Si_{1-x}Ge_x$ on strained Si

Figure 5.7 Band alignments for (001) oriented $Si_{1-x}Ge_x$/Si heterostructures. (a) Type I alignment for $Si_{1-x}Ge_x$ layers strained to match unstrained Si; (b) Type II alignment achieved if $Si_{1-x}Ge_x$ and Si layers are grown on hypothetical $Si_{1-y}Ge_y$ of intermediate composition such that SiGe is under compressing and Si under tension.

As shown in Figure 5.8, the valance band offset $\Delta Ev(x, y)$ of $Si_{1-x}Ge_x/Si$ heterostructure grown on relaxed $Si_{1-y}Ge_y$ buffer layer can be expressed as [37],

$$\Delta Ev\ (x, y) = (90.84 - 0.53y\ )\ x \qquad (5.3)$$

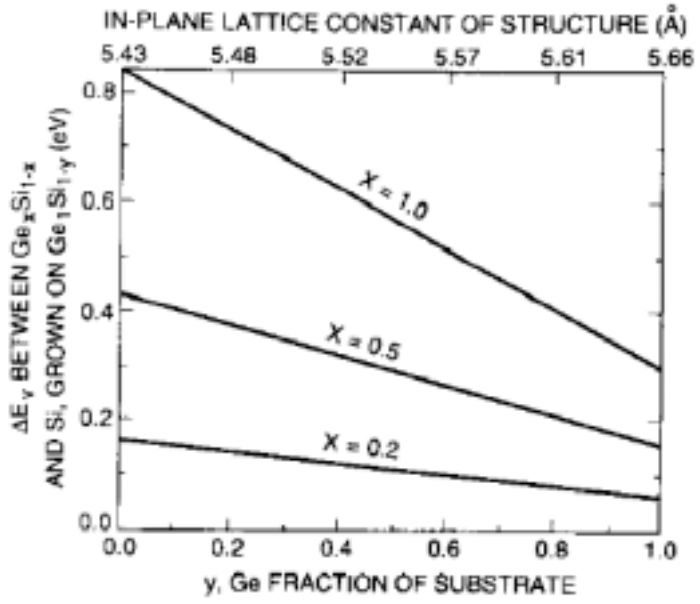


Figure 5.8 Valence band discontinuities between strained $Si_{1-x}Ge_x$ and Si layers grown on unstrained $Si_{1-y}Ge_y$ buffer layers (with in-plane lattice constant indicated at top). (From Bean [37])

The band structures of heterostructures and superlattices depend not only on band discontinuities but also on the doping in etch layer. Band banding will happen at the junctions. The valence band structure of sample HA99.071 (material structure in Figure 5.2) is simulated with SimWindows program and the result is shown in Figure 5.9. In this sample, the $Si_{0.7}G_{0.3}$/Si superlattice were grown on unstrained $Si_{0.9}Ge_{0.1}$ buffer layer, and they are uniformly doped with boron at 5×10^{19} cm^{-3}. It can be seen that the effective barrier in the valance band is greatly reduced by the doping and carrier tunneling will happen for the spike shape barriers. To better control, modulation doping is required.

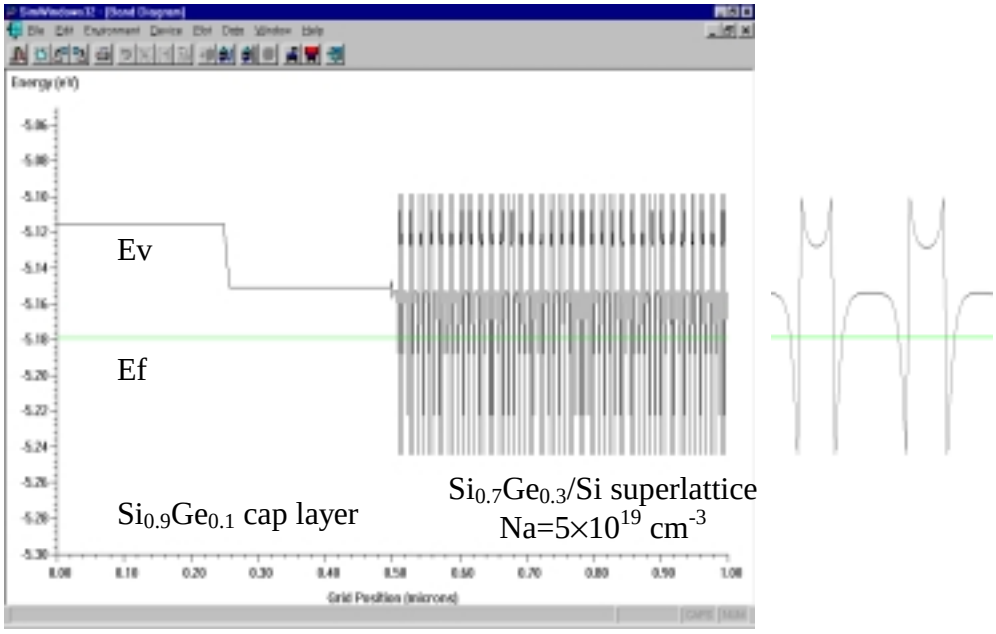


Figure 5.9 Simulated valance band structure of sample HA99.071 with SimWindows.

The $Si_{0.7}Ge_{0.3}$/Si superlattice has a valance band offset of about 0.2 eV [36], and hot holes over this barrier produce thermionic cooling. In addition, superlattice structure has many interfaces that increase phonon scattering, and therefore gets lower thermal conductivity.

5.3 Materials growth

Our SiGe/Si superlattice cooler samples are provided by Edward Croke from HRL Laboratories. They were grown in a Perkin-Elmer Si molecular beam expitaxy (MBE) on 125 mm diameter, (001)-oriented Si substrates. For n-type samples, the substrates were doped to < 0.020 Ωcm with Sb; for p-type samples, the substrates were doped to < 0.006 Ωcm with B.

To illustrate the superlattice growth, we take n-type SiGe/Si superlattice sample HA99.051 and p-type SiGe/Si superlattice sample HA99.071 as examples. Their cross sectional transmission electron microscopy images and structure are shown in Figure 5.10. The sample's main part is a 3 μm thick 200 × (5nm $Si_{0.7}Ge_{0.3}$/10nm Si) superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant was approximately

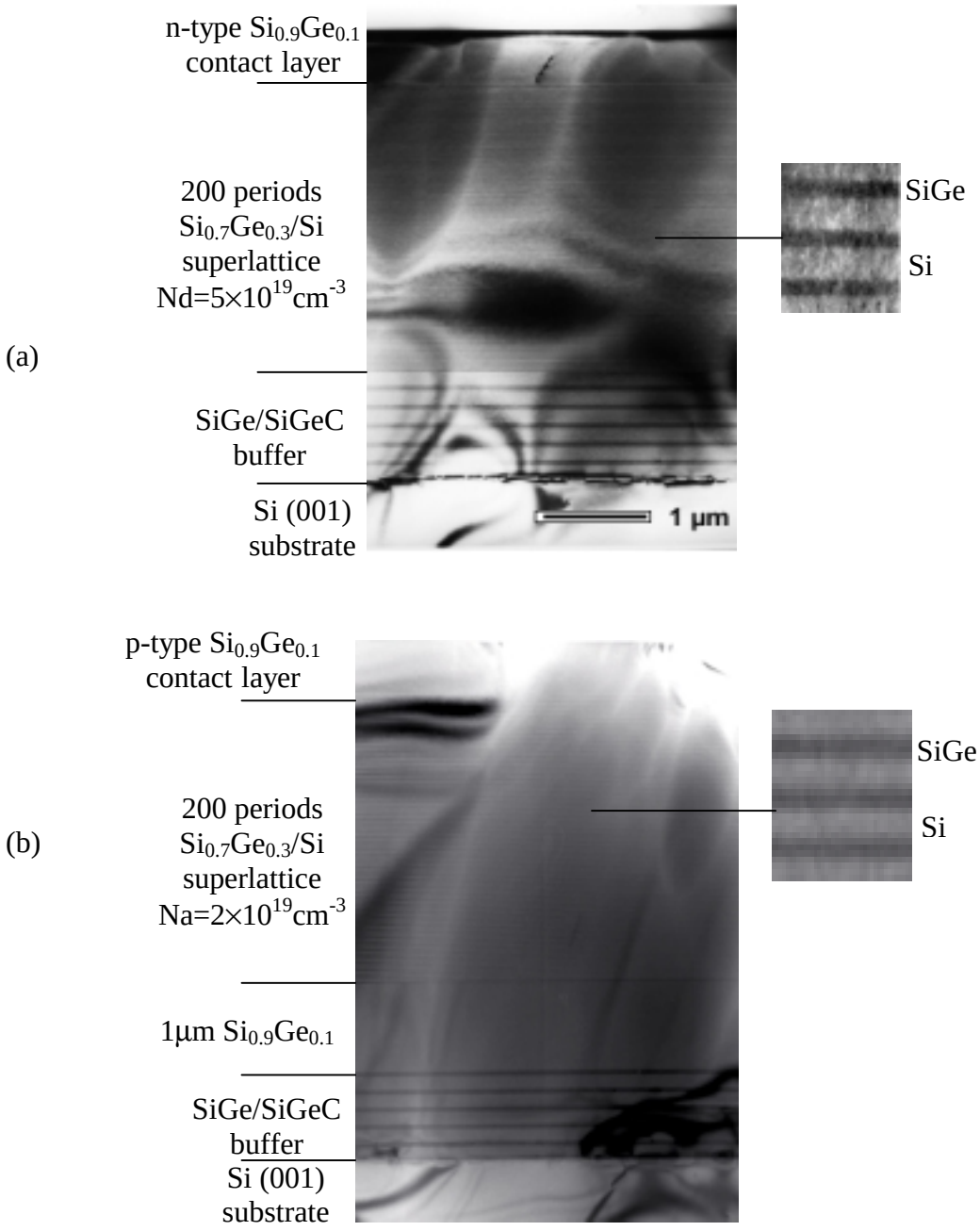


Figure 5.10 TEM pictures of MBE grown SiGe/Si superlattice coolers samples: (a) sample HA99.051 n-type (b) sample HA99.071 p-type [38].

that of relaxed $Si_{0.9}Ge_{0.1}$. The doping levels are 2×10^{19} cm^{-3} (Sb) and 5×10^{19} cm^{-3} (B) for n-type and p-type SiGe/Si superlattices, respectively.

The relaxed buffer layer has a 10-layer structure, alternating between 150 nm $Si_{0.9}Ge_{0.1}$ and 50 nm $Si_{0.845}Ge_{0.150}C_{0.005}$ [39]. For the n-type sample, the layers were grown at 390 °C and annealing was performed at 750 °C for 10 minutes after the growth of each $Si_{0.9}Ge_{0.1}$ layer. In the p-type case, the growth temperature was simply alternated between 700 °C for the $Si_{0.9}Ge_{0.1}$ layer and 500 °C for the $Si_{0.845}Ge_{0.150}C_{0.005}$ layer. After the relaxed buffer sequence, another 150 nm thick $Si_{0.9}Ge_{0.1}$ layer was grown at 390 °C for the n-type sample and a 1 μm thick Si0.9Ge0.1 layer was grown at 700 °C for the p-type case. Growth of a 200 period, 5 nm $Si_{0.7}Ge_{0.3}$/ 10 nm Si superlattice then followed at 390 °C (n-type case) and 500 °C (p-type case). Finally, the samples were capped with a heavily doped $Si_{0.9}Ge_{0.1}$ layer sequence to provide for a low-resistance ohmic contact.

5.4 SiGe/Si microcooler fabrication

Because of their thin film material structures and very small device sizes, microcoolers are very difficult to be processed with conventional bulk TE

cooler fabrication technology with mainly use mechanical machining and packaging. Integrated circuit (IC) processing is the preferred way to make microelectronic devices in a large scale. We will try to make SiGe/Si microcoolers with standard IC processing.

5.4.1 Processing of the basic SiGe/Si microcooler structure

Figure 5.11 shows the main process stages for the fabrication of the basic SiGe/Si microcooler structure in Figure 5.4.

The first step in SiGe/Si microcooler processing is sample cleaning, including HF wet etch for oxide removal and DI water rinse. Then the sample is patterned with photo resist for top metal contact. After hardening the resist at 120 °C for 2 minutes, the sample is cleaned with plasma cleaning for 20 seconds and then the second HF wet etch to make the sample ready for first metal contact.

The top metal contact is directly related to the contact resistance which is crucial to the microcooler performance, as discussed in Chapter 3. The contact resistance characterization will be described in Section 5.4.3. To have low contact resistance and facilitate later processing, Ti/Al/Ti/Au are deposited on to the sample in high vacuum (10^{-7} torr) e-beam system. The typical thickness

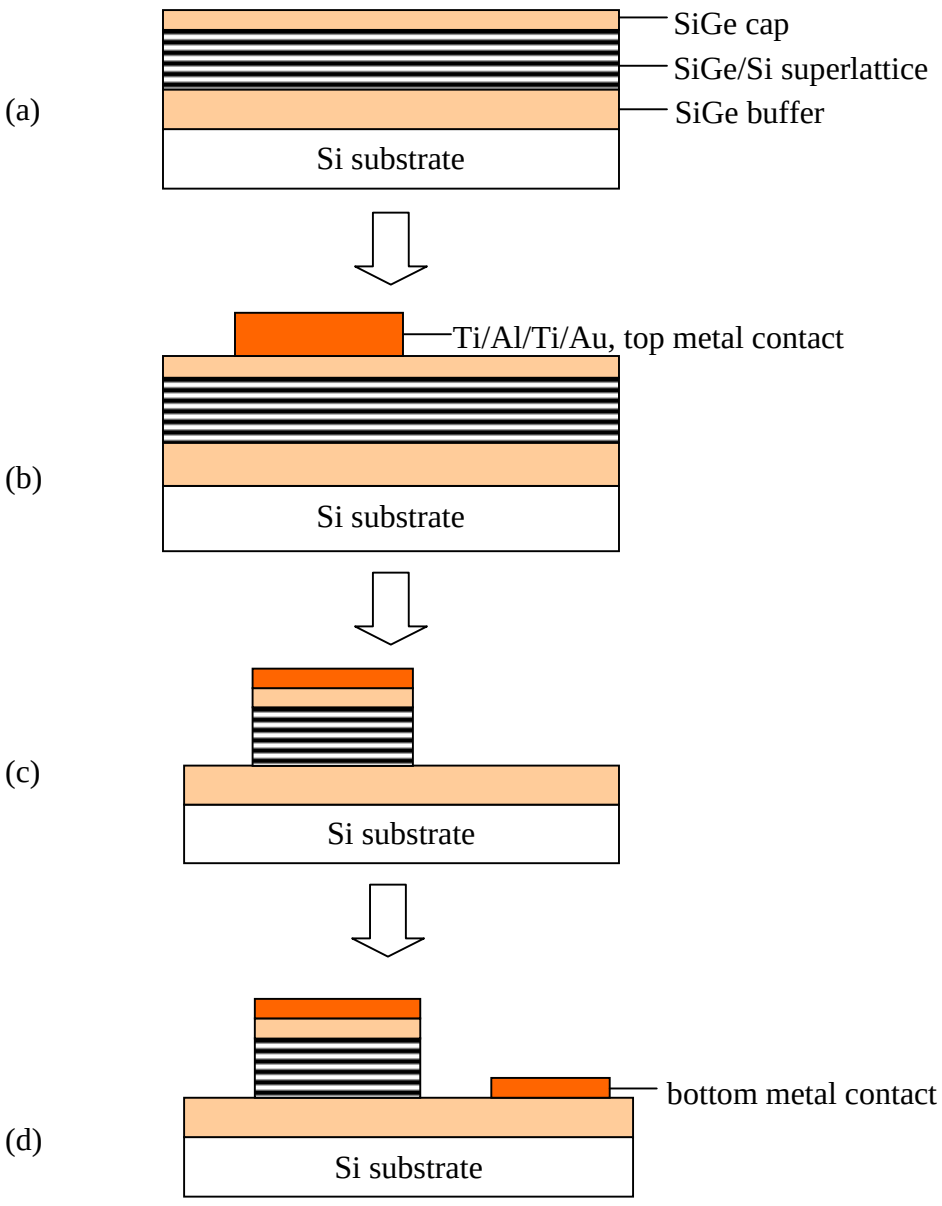


Figure 5.11 Main processing stages for the basic SiGe/Si microcooler structure.: (a) initial cooler sample; (b) top metal contact deposition; (c) mesa etch down to the buffer layer; (d) bottom metal contact deposition and annealing.

is 0.1μm/1μm/0.1μm/1μn respectively. The photo resist and unwanted metal are removed by liftoff technique after metal deposition.

To thermally isolate the microcooler, reactive ion etch is used to form the mesa structure in Figure 5.10 (c). Cl_2 is used at an etch rate of about 100 nm per minute and the etch time is selected to let the etch stop at the SiGe buffer layer. For deep mesa etch, a photolithograph step is needed to form a resist mask to protect the top metal contact. For shallow mesa etch (< 1 μm), the top contact metal can work as the mask and it can be a self-aligned mesa etch.

After the mesa etch, the bottom contacts are patterned on SiGe buffer layer with photolithography. Ti/Au e-beam deposition and liftoff processes are carried out to make to bottom metal contacts. Finally, the devices are annealed at 450 °C for 5 seconds in a strip annealer to reduce the contact resistance.

Since the SiGe/Si microcooler processing uses IC processing technology, thousands of microcoolers can be fabricated at the same time on a single wafer. Figure 5.12 shows the scanning electron microscope (SEM) images of the processed SiGe/Si microcoolers.

5.4.2 Processing of the SiGe/Si microcooler structure with integrated extended top metal contact

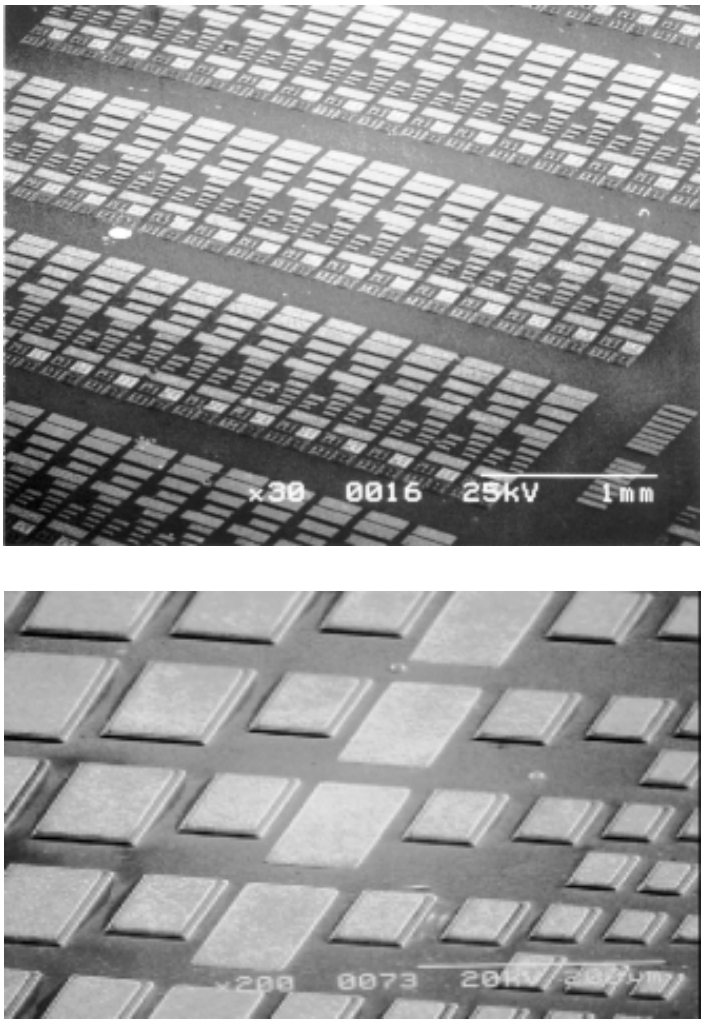


Figure 5.12 SEM images of the processed SiGe/Si superlattice microcoolers.

To send currents to the microcooler, the basic SiGe/Si microcooler structures in Figure 5.4 and 5.11 require addition contacts, such as probing or

wire bonding, to the limited area of the microcooler top contacts. This reduces microcooler performance and is not very good for integrating the microcooler with the microelectronic device to be cooled. The modified microcooler structure with integrated extended top metal contact, as shown in Figure 5.5, is a better way for microcooler testing and packaging. Its processing is similar to that of the basic SiGe/Si microcooler structure in the last section, but with a few more processing stages, as shown in Figure 5.13.

The device processing steps are the same as those of the basic SiGe/Si microcooler structures until the end of mesa etch. After the mesa etch, a passivation layer, such as 300 nm SiN_x, is deposited on the whole sample with PECVD. Then the sample is patterned with photo resist as a mask to etch off the SiN_x layer in the top and bottom metal contact region with CF_4 plasma etch. Another photolithography step is performed to pattern the sample for metal contacts, including the extended top metal contact pads. The Ti/Au deposited on the whole sample for the metal contact layer. After that, photo resist and unwanted metal are removed with liftoff process. Finally, the sample is annealed at 450 °C for 5 seconds in a strip annealer. A SEM image of the processed sample is shown in Figure 5.14.

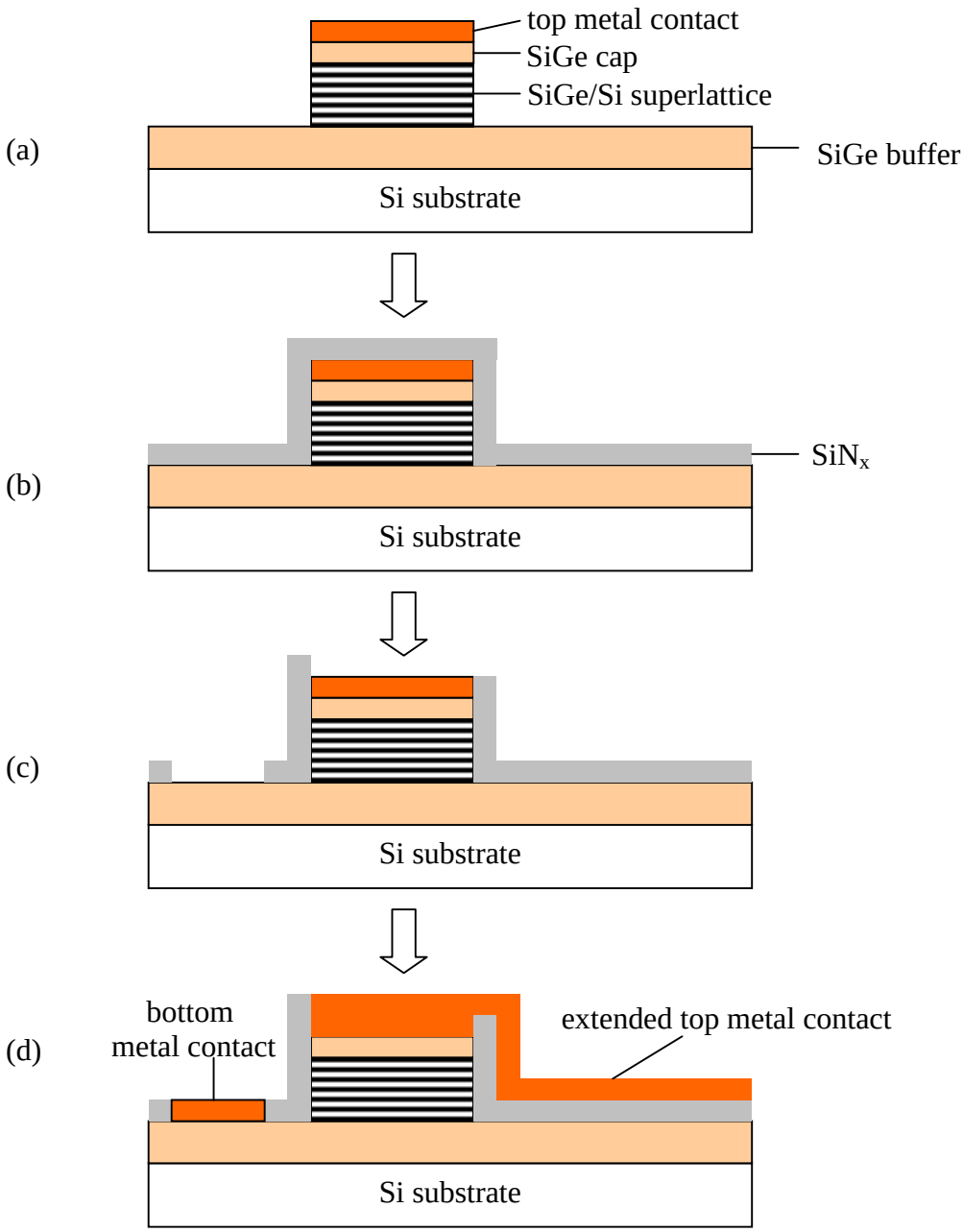


Figure 5.13 Some main processing stages for integrated SiGe/Si microcooler with extended top metal contact. (a) mesa etch; (b) SiN_x deposition; (c) SiN_x etch to open windows for top and bottom metal contact; (d) Ti/Al deposition and annealing.

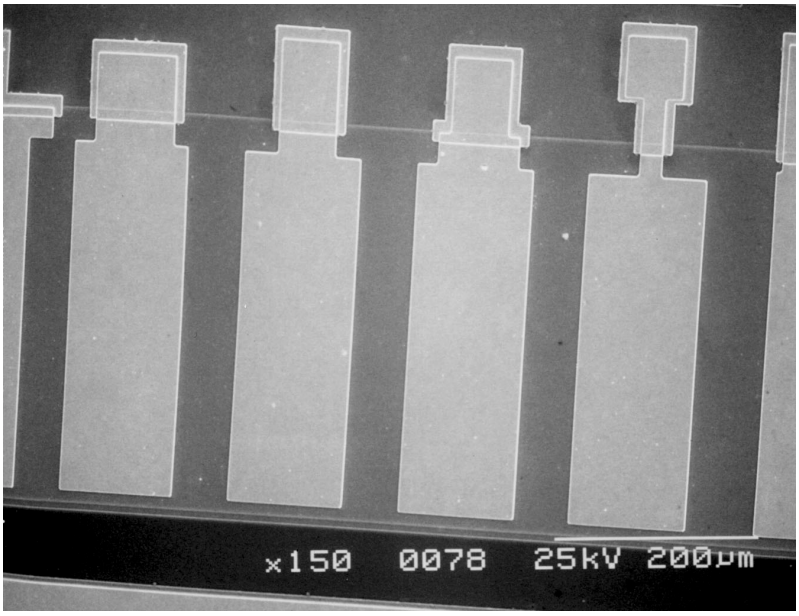


Figure 5.14 SEM image of the processed SiGe/Si microcooler with difference cooler shape.

5.5 Microcooler cooling temperature measurements

The sizes of the SiGe/Si microcooler ranged from 10×10 μm^2 to 500×500 μm^2. Device testing for microcoolers is still a challenging research area. It includes small area temperature and temperature distribution measurements, cooling power measurements and cooling response time measurements, etc. In

this section, we will discuss the cooling temperature measurements for microcoolers, including testing with micro thermocouples, IR camera, thermoreflectance method and integrated thermal sensors.

5.5.1 Test with micro thermocouples

A thermocouple is a commonly used thermoelectric device for temperature measurements. It is composed of two different metal wires and the junction temperature can be measured through Seebeck voltage measurement at the two terminals of the thermal couple. Depending on the metal materials they are composed of, thermocouples can be divided into many types, such as E, J, K, R, S, T, etc. Each type thermocouple has different working temperature range and sensitivity (or Seebeck coefficient). Table 5.1 shows the Seebeck coefficients for some commercial thermocouples at 20 °C [40]. Among them, E-type thermocouple has the highest Seebeck coefficient, thus the highest sensitivity at room temperature. Therefore, we selected E-type micro thermocouple to be used in our cooling temperature measurements.

The cooling temperature measurement setup with micro thermocouples is shown in Figure 5.15. The sample is tested on a temperature-controlled heat sink, which is kept a constant temperature during device testing. The cooling temperature is measured by two micro thermocouples: one is at the heat sink

Table 5.1 Seebeck coefficients for some commercial thermocouples at 20 °C.

thermocouple type	Seebeck coefficient (μV/°C) @ 20°C	thermocouple materials
E	62	Nickl-10%Chromium(+) vs. Constantan(-)
J	51	Iron (+) vs. Constantan (-)
K	40	Nickel-10%Chrominm (+) vs.Nickel-5%AlSi (-)
R	7	Platinum-13%Rhodium(+) vs. Platinum(-)
S	7	Platinum-10%Rhodium(+) vs. Platinum(-)
T	40	Copper (+) vs. Constantan (-)

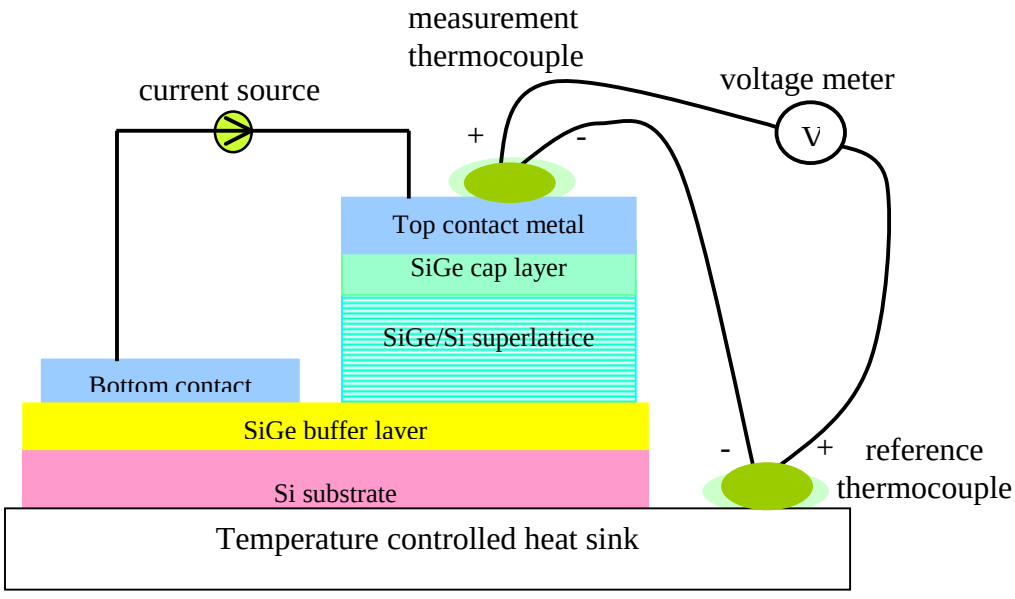


Figure 5.15 Cooling temperature measurement with micro thermocouples.

surface for reference temperate; the other is on the top metal contact of the microcooler for cooling temperature measurement. The thermocouples' negative polarity wires are connected together and the positive polarity wires are connected to a digital voltage meter. In this way, the measured temperature is the temperature difference between the microcooler and the heat sink. This differential temperature measurement has a lower signal noise level than measuring the microcooler and heat sink temperature separately. The measurement thermocouple has a wire diameter of 25 μm and the thermocouple junction bead size is around 50 μm.

Since the thermocouple head bead is in a ball shape, the contact area between the thermocouple and the object to be measured is very small, which makes poor thermal contacts. To improve the measurement accuracy, a small amount thermal paste with good thermal conductivity is used to improve the thermal contact. We used the thermal paste in the thermocouple-microcooler contact, thermocouple-heat sink contact and the cooler sample - heat sink contact, and this significantly improved signal to noise ratio in the microcooler cooling temperature measurements.

To test the cooling temperature of the microcoolers, we first need to send currents to drive the microcooler devices. As mentioned in Sections 5.2 and 5.3, there are two microcooler structures: the basic SiGe/Si microcooler

structure with isolated top and bottom contacts and the improved SiGe/Si microcooler structure with integrated extended top metal contact. Figure 5.16 shows three testing structures for these microcoolers with micro thermocouples: direct probe testing, wire bonding, and testing with the extended to metal contact pads. We will discuss these three structures respectively.

The direct probe testing structure in Figure 5.16 (a) is simple for both device fabrication and testing. It just directly put two micro probes on the top contact and bottom contact respectively and sends current to the microcooler. For p-type coolers, current goes from the top contact to the bottom contact for cooling; for n-type materials, current goes from the bottom contact to top contact for cooling. If the current is reversed from that of the cooling operation, the microcooler will work as a heater. This direct probing method has a lower microcooler testable size limit. Since the micro thermocouple we used for testing has a heat bead size of about 50 μm and micro probe takes an additional space of about 50 μm, smallest testable microcooler size is about 100 μm for the direct probe testing method. Another issue of the direct probing method is the contact resistance between the probe and the microcooler top contact metal. This probe contact is a point contact and the contact area is small, thus the contact resistance relatively large. The current density of thin film microcoolers

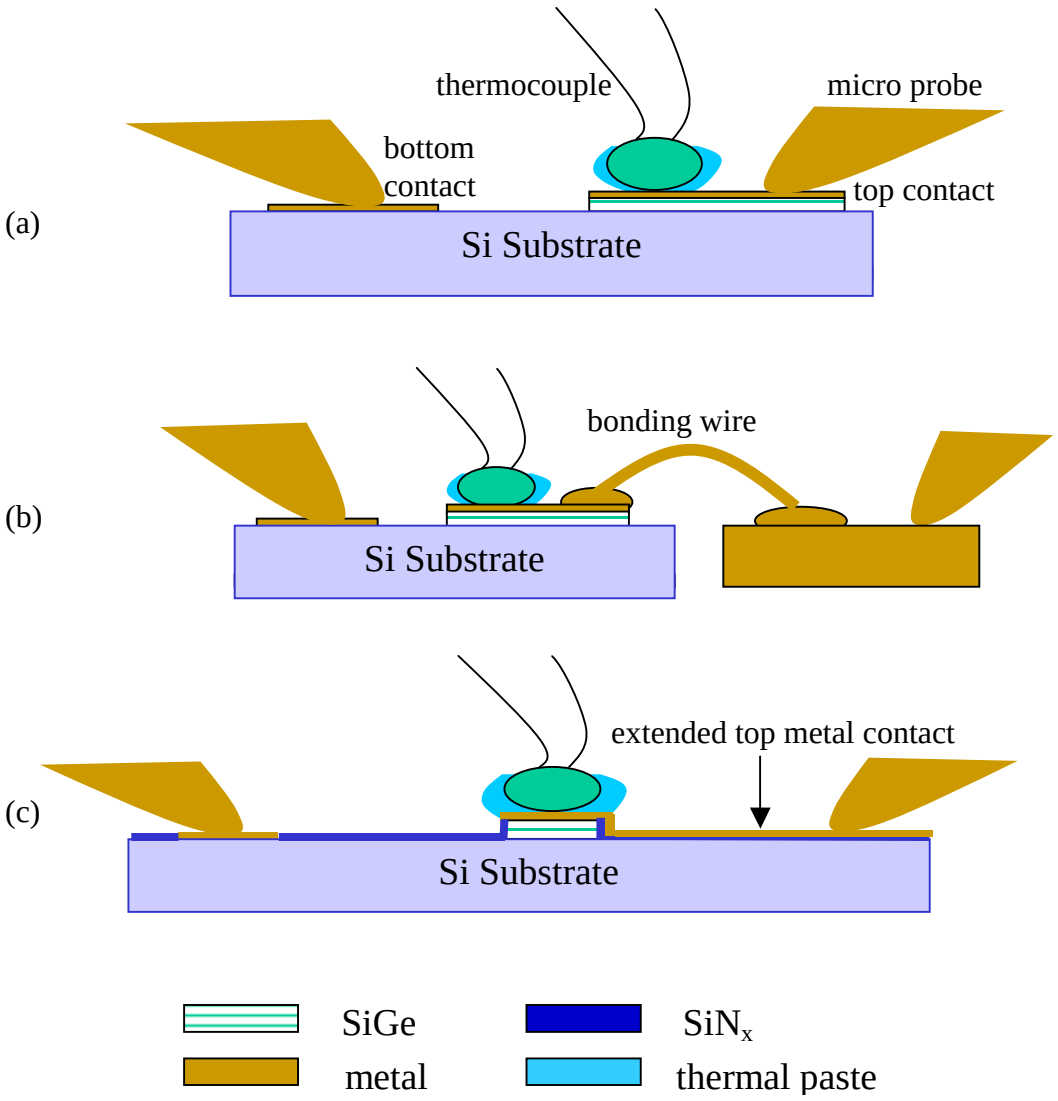


Figure 5.16 Microcooler testing structures: (a) direct probe testing; (b) wire bonding; (c) testing with integrated extended top metal contact pad.

is very large and joule heating will happen at the probe and microcooler contacts. This will reduce the cooling and make the temperature of the microcooler not uniform. Therefore, depending on the stress applied on the probe and the positions of the probe and the micro thermocouple, the measured cooling temperature will vary especially for small cooler sizes. This makes the testing repeatability not very good.

As shown in Figure 5.16 (b), wire bonding is another way for microcooler testing and packing. In this method, current is sent to the microcooler top metal contact through the bounding wire. An SEM image of the wire bonding contact of a 25 μm diameter Au wire is shown in Figure 5.17. The contact area of the wire bonding contact is larger than that of the probe point contact, thus it has a smaller contact resistance than micro probing. On the other hand, this larger contact area also limits the smallest microcooler size that wire bonding can be applied to. For 25 μm diameter Au wires, the minimum pad size foe bounding is about 50 μm. Considering the bead size of the micro thermocouple, the minimal microcooler size for testing with wire bonding and thermocouples is about 75 μm.

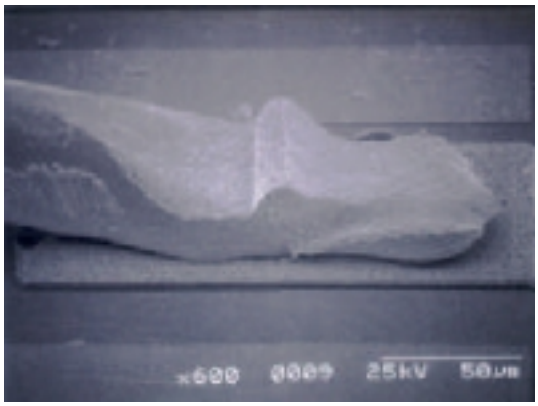


Figure 5.17 A SEM image of a wire bonding contact. The wire is a 25 μm diameter Au wire.

The bonding wire length is usually in the order of millimeter. When current is sent to the microcooler through this wire, there will be joule heating in it. About half of the heat generated in the bonding wire will go to the microcooler as a heat load and the other half will go to the other bonding end. This causes extra heat load to the microcooler and reduces the maximum cooling temperature. Figure 5.18 shows the measured cooling temperature on n-type $Si_{0.7}G_{0.3}$/Si superlattice microcooler tested with thermocouple and wire bounding. The cooler sample is HA99.051, its TEM cross-sectional image has been shown in Figure 5.10 (a). The tested device size is 150×150 μm^2. The bonding wire was 25 μm diameter Au wire. One wire bonding and two wire

bonding was tried. The maximum cooling increased from 0.9 K to 1.1 K by changing one wire bonding to two wire bonding.

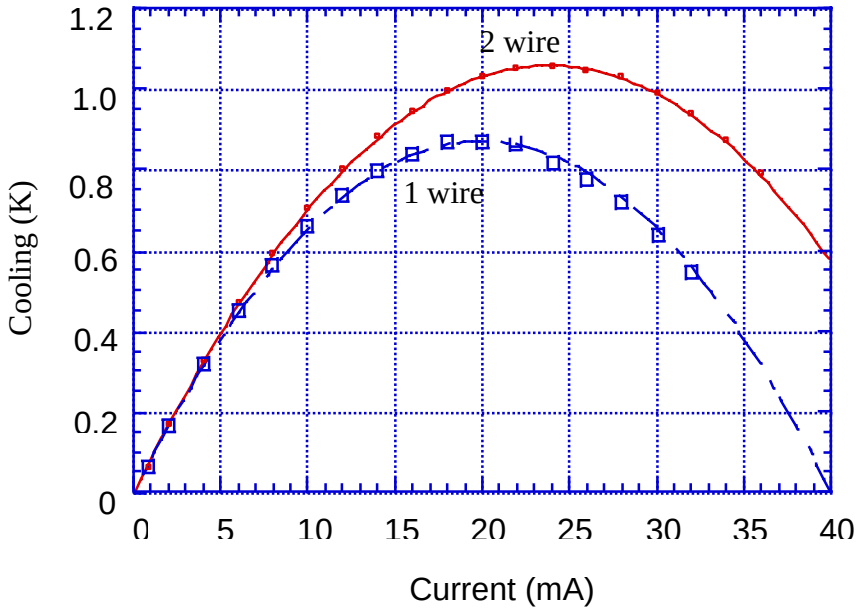


Figure 5.18 Thermocouple measured cooling n-type SiGe/Si superlattice (sample HA99.051) with the testing structure of one wire bonding and two wire bounding. The bonding wires are 25 μm diameter Au wires.

Considering the bonding wire resistance R_w, the cooling power Q_c and cooling temperature ΔT can be expressed as

$$Q_c = SIT_c - \frac{1}{2}(R+2R_c+R_w)I^2 - \frac{\Delta T}{R_{th}} \qquad (5.4)$$

$$\Delta T = R_{th}\left[SIT_c - \frac{1}{2}(R+2R_c+R_w)I^2 - Q_c\right] \qquad (5.5)$$

where S is the Seebeck coefficient, I is the current, T_c is the cold side temperature of the cooler, R is the electrical resistance of the TE leg, R_c is the contact resistance, R_{th} is the thermal resistance of the TE leg. When wire bonding changes from one wire bonding to two wire bonding, the wire resistance decreases which will cause the quadratic coefficient of the cooling vs. current curve decreasing while the linear coefficient unchanged, according to Equation 5.5. The experiment results in Figure 5.18 fits this prediction well.

Both the direct probing structure and the wire bonding structure use external contacts to the cold side of microcooler. This not only puts some limits on the measurable microcooler size, but also make the packaging or integration of the microcooler with the to be cooled microelectronic devices difficult. The testing structure with integrated extended top metal contact pad, as shown in Figure 5.16 (c), can be a better choice. This only needs a few more processing steps in the microcooler fabrication as described in Section 5.4.2, but it eliminates the external contacts directly on the cold surface of the microcooler. In this structure, the testing probe or wire bonding can be in the I/O area of the chip and the minimum measurable device size is not limited by the probe tip size and the wire bonding junction size anymore. For micro thermocouple testing, the measurable microcooler size is now limited by the thermocouple bead size. In our setup, the smallest measurable device size is $40 \times 40\ \mu m^2$.

More important, the integrated extended top contact structure can keep the microcooler top surface flat and easy for packing or integration with the microelectronic devices that need to be cooled.

Direct probe testing, wire bonding and integrated top metal contact are the developments sequence of our microcooler testing. With this development, testable device size decreased, the test receptivity improved and better results were measured. Figure 5.19 shows the measured cooling on p-type SiGe/Si microcooler sample HA99.071 (the material structure is shown in Figure 5.2). The cooling temperature was measured with micro thermocouples at room temperature and was relative to the device temperature at zero current. With the microcooler size went from 150×150 μm^2 down to 100×100 μm^2 and 50×50 μm^2, the measured maximum cooling temperature increased from 1.3 K to 1.9 K and 2.7 K respectively. This is partially due to the testing structure improvements and is partially due to the devices size effects. Unlike conventional bulk TE coolers whose maximum cooling temperature generally doesn't depend on the device size, our microcoolers showed that their cooling performance is device size dependent. The size effects will be discussed in later sections in this chapter.

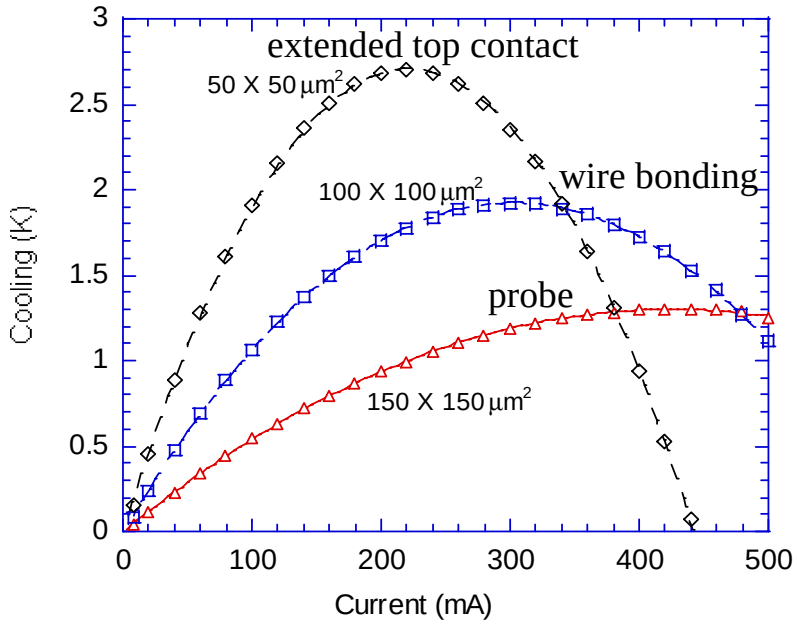


Figure 5.19 Measure cooling on p-type SiGe/Si superlattice microcoolers (sample HA99.071) with different testing structures: direct probe testing, wire bonding and integrated extended top metal contact structure. The device size are 150×150 μm^2, 100×100 μm^2 and 50×50 μm^2 respectively. This cooling is measured with micro thermocouples at room temperature.

5.5.2 Test with IR cameras

Microcooler cooling temperature measurement with thermocouples is a contact measurement method. Thermocouples along with some thermal paste need to contact the cooler surface and get thermal equilibrium with it. Due to the small size of the microcooler, the size of the thermocouple is relatively large, even for micro thermocouples. When the microcooler works at the

cooling mode, its top surface temperature will be below its environmental temperature and a temperature gradient will be established on the thermocouple. This will introduce heat flow to the microcooler through thermocouple heat conduction. The smaller the microcooler size and the larger cooling temperature, the larger adverse impact to the cooling performance will be from the contact temperature measurement. To solve this problem, non-contact temperature measurement is preferred.

Infrared (IR) cameras can be one of the non-contact temperature measurement methods. All materials have infrared radiation and this radiation increases with temperature increase. With proper calibration of relation between the IR radiation intensity and temperature, the temperature can be measured through the infrared radiation detection. IR cameras usually consist of an IR detector array, such as InSb IR detector array, which are located at the focal plane of the IR camera. Each detector can be a pixel in the thermal image. IR cameras have been widely used in military for night vision, etc. Recently, they are also developed for microscopic thermal imaging applications. Due to its smaller IR signal at room temperature, this is still a challenging research area.

We used a Radiance IR camera made by Raytheon Inc. to measure the thermal image of our SiGe/Si superlattice microcooler. Its pixel size is 30 μm

and the nominal temperature resolution is 0.02 K at room temperature. The IR image of the p-type SiGe/Si microcooler (sample HA99.071) is shown in Figure 5.20. The tested microcooler size is 90×170 μm^2. Figure 5.20 (a) and (b) show its thermal image at zero current and 400 mA current respectively. Form the thermal images, no cooling can be seen on the microcooler and only the bottom contact probe heating can be observed at 400 mA current. The thermocouple measured cooling on this sample is shown in Figure 5.20 (c) and 1.7 °C is measured at 400 mA current. This measurement difference between micro thermocouple and IR camera shows that this IR camera's sensitivity or signal to noise ratio is not high enough for our microcooler measurement. The IR radiation at room temperature is a very small signal, the nominal camera temperature resolution is at the ideal testing condition. When microscope lens are used to increase the IR camera's space resolution, the IR signal and temperature resolution may get lower. The IR radiation not only depends the temperature, but also heavily depends on the material's emissivity. Our microcoolers have gold deposited surface, which have high reflectivity but low

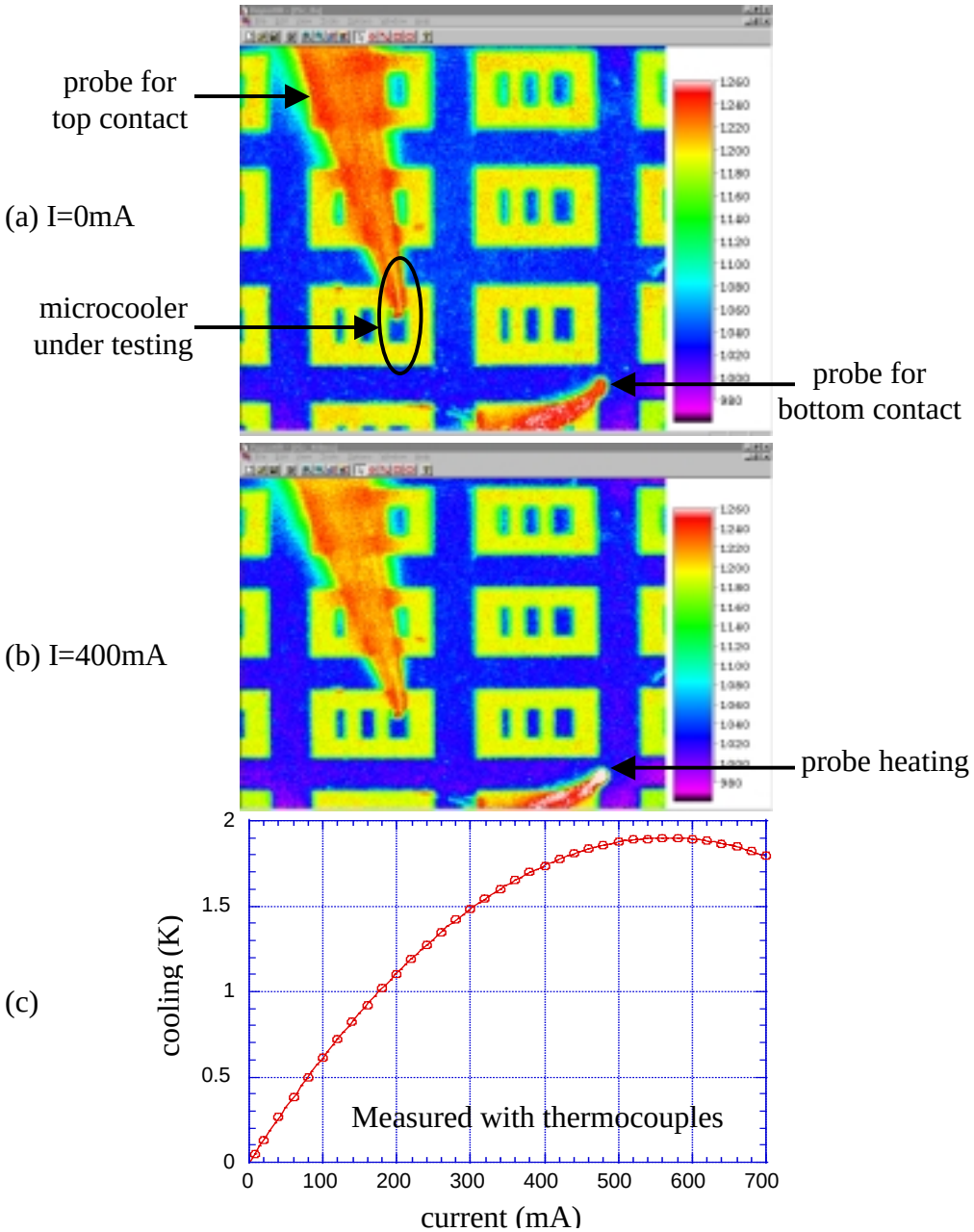


Figure 5.20 P-type SiGe/Si superlattice microcooler characterization. The size of the microcooler measured is $90 \times 170\ \mu m^2$. (a) thermal image measured with IR camera at 0 mA current; (b) thermal image measured with IR camera at 400 mA current; (c) cooling temperature measured with thermocouple.

resistivity. This further reduces the noise to signal ratio in the IR camera thermal image measurement for the microcooler.

To increase the signal to noise ratio, the microcooler can be coated with some high emissivity material. Another way to increase the signal to noise ratio of the IR detection is to modulating the current to drive the microcooler and testing the signal through lock-in technique.

5.5.3. Test with thermoreflectance method

Thermoreflectance imaging is another non-contact temperature measurement method [41-44]. Like IR camera, thermoreflectance imagine can also give the temperature distribution which is very important of the thermal management of microelectronics. The thermoreflectance method is based on that the material's optical reflectivity is a function of temperature. The temperature change ΔT can be obtained by measuring the reflectivity change ΔR.

$$\Delta T = \frac{\Delta R}{\frac{dR}{dT}} \tag{5.6}$$

The reflectivity change rate $\frac{dR}{dT}$ is in the order of 10^{-5} for metals. Therefore, the reflectivity change is a very small signal and lock-in technique is used for getting sufficient signal to noise ratio.

One advantage of thermoreflectance method over IR camera is its higher spatial resolution. The spatial resolution of the IR camera is limited by its long wavelength of infrared signal and 3~5 μm is the typical resolution for HgCdTe IR cameras. In thermoreflectance method, visible light can be used and submicron resolution can be achieved.

The SiGe/Si microcoolers were tested by James Christofferson for the thermoreflectance imaging in UC-Santa Cruz [41]. The experimental setup is shown in Figure 5.21. White light from an illuminator was used as the light source and the reflected thermal image is recorded by the Hamamtsu 16 × 16 PIN camera. The microcoolers are driven by current pulses and lock-in amplifiers are used for noise filtering. The measurement calibration is base on the temperature measured with micro thermocouple on large devices in which case the device temperature change due to the thermocouple contact is small.

Figure 5.22 shows the thermoreflectance image measured on the p-type SiGe/Si superlattice microcooler (sample HA99.071). The device size is 40 × 40 μm^2 and over 4 K cooling is measured at 40 °C with a current of 250 mA.

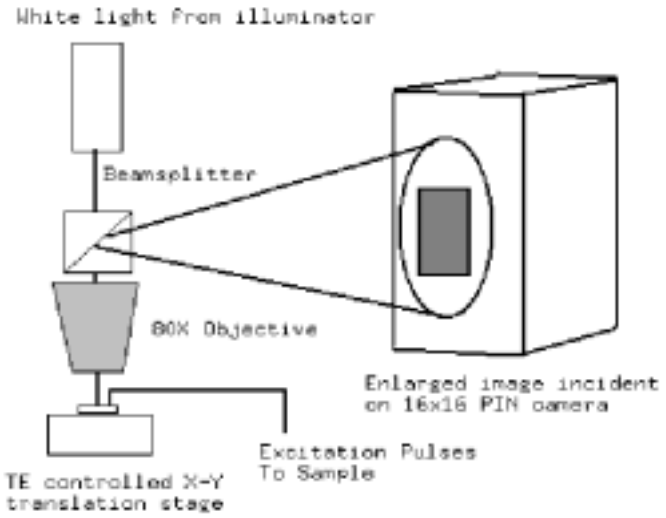


Figure 5.21 Experimental setup of the thermoreflectance imaging. From Christofferson [41].

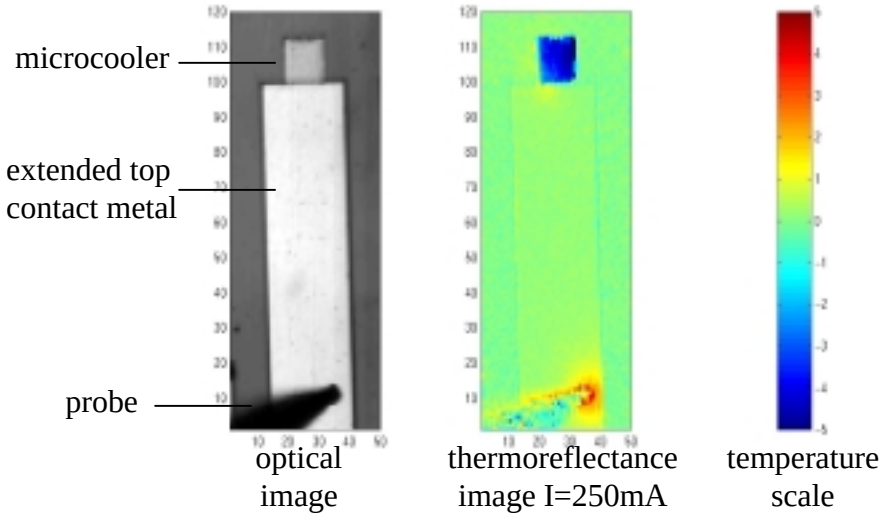


Figure 5.22 Measured thermoreflectance image of the p-type SiGe/Si superlattice microcooler (sample HA99.071) at 40 °C. The microcooler size is $40 \times 40\ \mu m^2$.

The temperature on the microcooler looks uniform. The joule heating at the contact between the test probe and the extended top metal contact can also be observed in the measured thermoreflectance image. This is consistent with our cooling measurements with thermocouples which show close distance between the thermocouple bead and the probe tip can reduce the measured cooling.

5.5.4. Integrated temperature sensor

Thermocouples, IR cameras and thermoreflectance method are all external measurement methods are cooling temperature characterization. Integrated temperature sensor would be a more convenient way in monitoring the temperature of the microcoolers and the micro devices to be cooled. One goal of our silicon microcooler research is to integrate the microcoolers, microelectronics and temperature sensors together on a single chip.

Microcoolers can be used for localized temperature control of temperature sensitive micro devices and some device characteristics of these micro devices can in turn be used for temperature characterization. For example, Dutta used monolithically integrated TE cooler to cool semiconductor lasers and the cooling temperatures were measured by the wavelength changes of the lasers [45-49]. In this case, the semiconductor laser can be regarded as an integrated temperature sensor.

Another commonly used temperature measurement method is resistive temperature device (RTD). It is based on that material's electrical resistance changes with temperature. The temperature is measured through resistance measurement. A typical RTD consists of a fine platinum wire wrapped around a mandrel and covered with a protective coating. For integrated thermal sensors, thin film metal wires can be made on the chip as RTDs to measure temperature. For the metal selection, platinum is commonly used because of it high resistance coefficient $\frac{dR}{RdT}$ (about 0.039/K at room temperature). Other metals should also work, but with less sensitivity. A SEM image of a processed integrated Au thin film resistor on the SiGe/Si microcooler is shown in Figure 5.23. Before the metal deposition of the thin film resistor, a SiN_x film was deposited for electrical isolation between the microcooler and the thin film sensor. The resistance of the thin film resistor can be measured with four-probe method to eliminate the contact resistance effect on the measurement.

The cooling measurement result on P-type $Si_{0.75}Ge_{0.25}$/Si microcooler (sample HA00.085) with the integrated thin film resistor method is shown in Figure 5.24 along with the thermocouple measurement results. It shows the cooling temperature can be measured with the integrated resistor method and the result is similar with that of the thermocouple method.

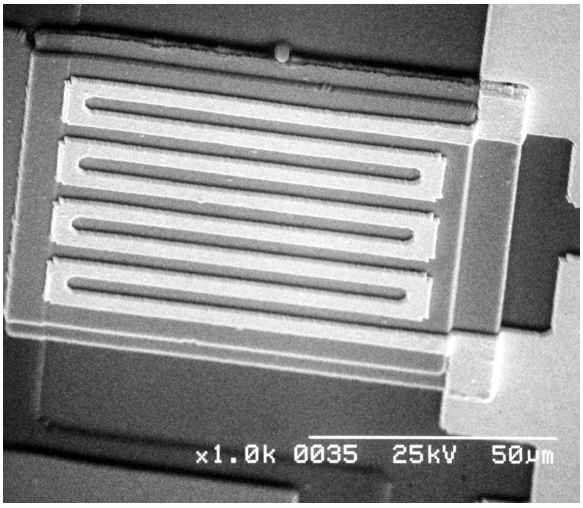


Figure 5.23 SEM image of the integrated thin film metal resistor on the SiGe/Si microcooler.

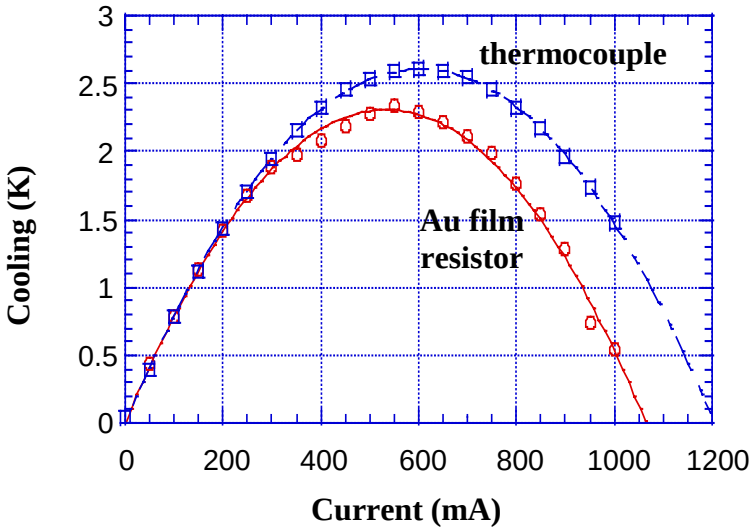


Figure 5.24 Measured cooling on 100 × 100 μm^2 p-type SiGe/Si microcooler with thermocouple and integrated thin film resistor at 25 °C. The cooler sample is HA00.085, 200 × (3 nm Si / 12 nm $Si_{0.75}Ge_{0.25}$) superlattice, Na = 5~7 × 10^{19} cm^{-3}.

5.6 Cooling power density measurement

Cooling power density is an important characterization parameter for TE coolers. Large cooling power density is preferred. This is especially true for microcoolers. First, the microcooler has a small cooling area, thus the total cooling power is low. For a certain heat load, small coolers require large cooling power density. Second, the heat generation on microelectronic chips is not uniform. Some devices are active ones, some are passive ones, and they consume different amount of energy. Hot spots may exist on the chip and threat the device performance and reliability. Integrated microcoolers are an attractive way to solve this problem. At these hot spots the power density is much higher than the average power density of the chip. Therefore, high cooling power density is required for the localized thermal managements. Theoretically, thin film microcoolers can have high cooling power densities due to its short TE leg structure. To check it out, experimental measurement of the cooling power density is necessary.

Microcooler cooling power density can be measured through measuring the relation between cooling temperature and the heat load. Several cooling temperature measurement methods have been discussed in the last section. In this section, we will emphasize on the heat load characterization.

For bulk TE coolers, the heat load can be applied and measured by putting an external heater in contact with the cooler. But for microcoolers, the external heater method doesn't work well. Due to the small size of the microcooler, micro heater is needed and it is difficult to separate how much heat of the heater goes to the microcooler and how much heat goes to elsewhere, such as the heater's connectors or supporters etc.

Another way to add heat load to the microcooler is to use non-contact method. Lasers can be used as a heat source to heat the microcooler. The incident laser power can be measured by laser power meters and it should be adjusted according to the microcoolers' surface states, reflectivity, etc. To measure the cooling power density, cooling temperature needs to be measured at the same time. Thermocouple and thermal paste will make the surface complicated for laser energy absorption measurement of the microcooler. The laser will increase the noise of IR camera. Therefore, the thermocouple and IR camera temperature measurements don't work well with the laser heating method. The cooling power density measurement may work for the combination of the laser heat load and the thermoreflectance temperature measurement. The laser noise may be filtered out by the lock-in amplifier in the thermoreflectance measurement.

Integrated thin film metal resistor/heater is the way we used for the cooling power density measurement. The same integrated thin film metal resister structure we used for temperature measurement in the last section can be used as a integrated micro heat to add and measure the heat load to the microcooler. The processing of the integrated metal resister has been described in Section 5.5.4. Figure 5.25 shows a SEM image of the device structures with the integrated microcoolers and thin film metal resistors. The microcoolers and thin wire resistors are electrically isolated by a layer of SiN_x film. The upper pads in the picture are for the probing of the metal resistors; the lower pads in the picture are for probing of the extended microcooler top metal contacts.

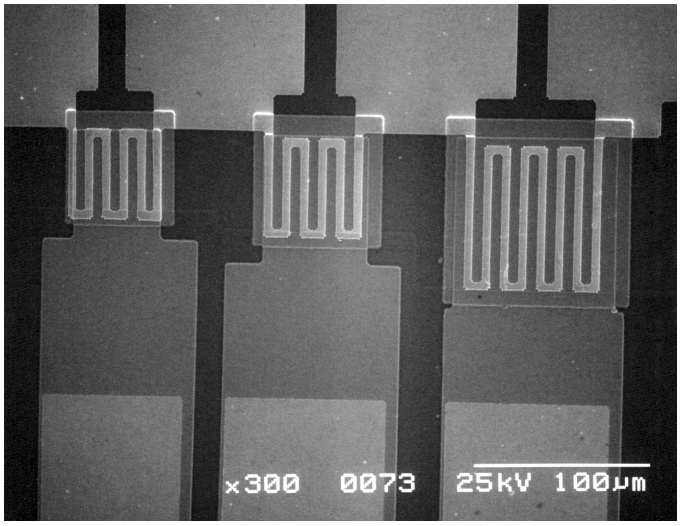
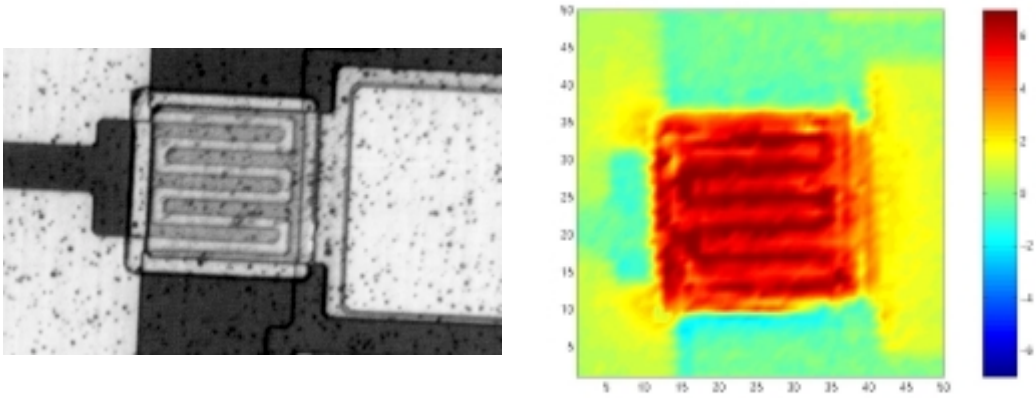


Figure 5.25 SEM image of the integrated microcoolers and thin film metal resistors. A SiN_x layer was deposited on the microcooler before the metal wire resistor deposition. The upper pads are for the probing contacts of the thin film resistors; the lower pads are for the probing contacts of the microcoolers.

The electrical resistance of the integrated thin film metal resistors can be measured by four-probe resistance measurement. By sending current to the metal resistors, the heat load to the microcooler can be easily calculated and controlled. Figure 5.26 shows the optical and thermoreflectance image with current in the integrated thin film metal resistor a 70 × 70 μm SiGe/Si microcooler. It shows the heat is mainly on the microcooler and it can be a suitable heat load to the microcooler.



Optical image Thermoreflectance image

Figure 5.26 The optical and thermoreflectance images of the integrated thin film metal resistor on a 70 × 70 μm^2 cooler with current in the resistor for heat load. Measured by Christofferson.

The cooling power density measurement result on 40×40 μm^2 microcooler of sample HA00.085 is shown in Figure 5.27. The sample is a p-type 3 μm 200 × (3 nm Si / 12 nm $Si_{0.75}Ge_{0.25}$), Na = 5~7 × 10^{19} cm^{-3}. The resistance of integrated metal resister is 0.371 Ω. The maximum cooling temperature decreases linearly with increasing the heat load. The maximum cooling power density can obtained from the x-axis interception in Figure 5.27 (b). The maximum cooling power density is 598 W/cm^2 for this microcooler, which is much higher than those of bulk TE coolers.

5.7 Transient response measurement

The transient response time of TE coolers is important for fast temperature control and fast cooling. Thermoelectric cooling and thermionic cooling happen at the junctions between different materials with electrical currents going through them. The energy is transfer through the current flow and the temperature change is achieved with phonon-electron interaction. This is a fast process and not the limiting factor for the cooler response time. The thermal diffusion time in the cooler is much larger.

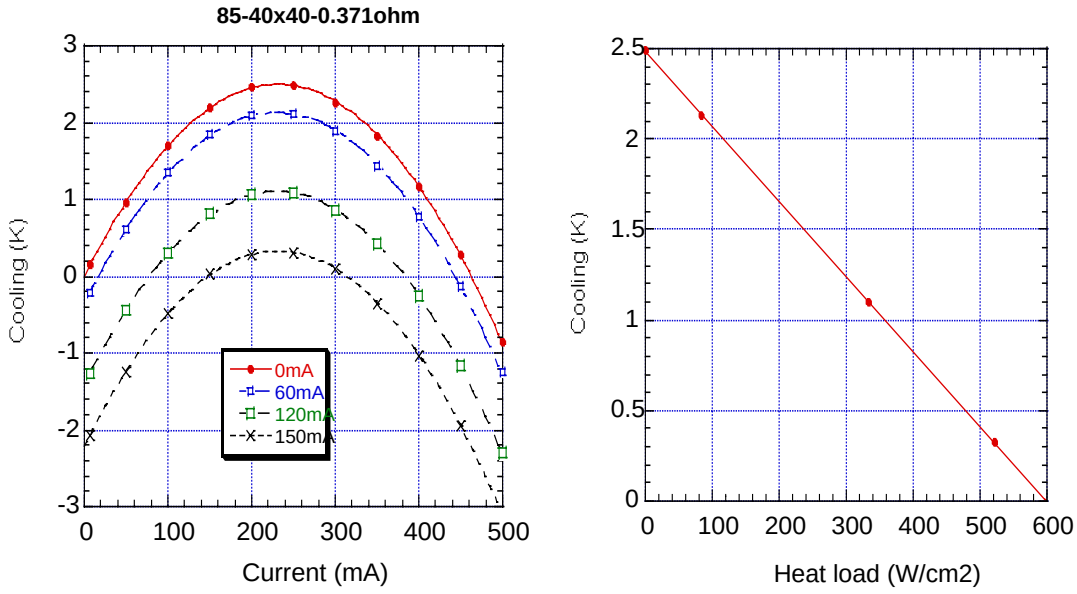


Figure 5.27 Cooling power density measurement results on 40 × 40 μm^2 p-type SiGe/Si microcooler (sample HA00.085) at 25 °C. (a) cooling temperature vs. current at different integrated wire resistor currents, the resistance of the resistor is 0.371 Ω. (b) Maximum cooling power vs. the heat load density.

The thermal diffusion time t_0 can be expressed as

$$t_0 = \frac{d^2}{D} \qquad (5.7)$$

where d is the distance between the cooler cold side and the heat sink and D is the thermal diffusivity of the TE leg. Due to the small d of thin film microcoolers, fast transient response can be expected.

The transient response time on SiGe/Si microcoolers was measured by Alberto Fitting with thermoreflectance method in UC-Santa Cruz. [50] The measurement setup is shown in Figure 5.28. A current pulse is sent to the microcooler and the temperature response is measured through the reflectivity change of the cooler.

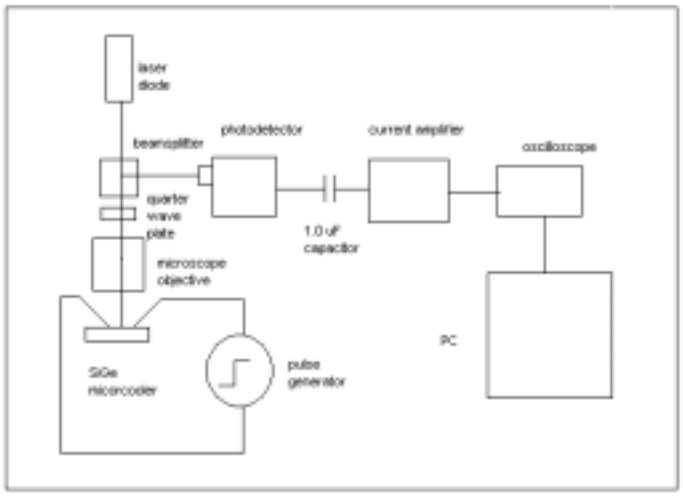


Figure 5.28 Experimental setup for the transient response measurement for SiGe/Si microcoolers. From Fitting [50].

Figure 5.29 shows the measured microcooler transient response on sample HA00.034 at room temperature. The sample is a p-type $Si_{0.8}Ge_{0.2}$ alloy samples, its structure consists of 4.3 μm $Si_{0.8}Ge_{0.2}$ and 1 μm SiGe/SiGeC buffer

grown on p-type Si substrate. Devices sizes of 80×80 μm^2 and 40×40 μm^2 were measured and the measured response time is 20 ~ 30 μs. This result is comparable with the reported 15 μs response time on Bi_2Te_3/Sb_2Te_3 superlattice microcoolers, and its much faster than bulk TE coolers whose response time is in the order of tenths of second.

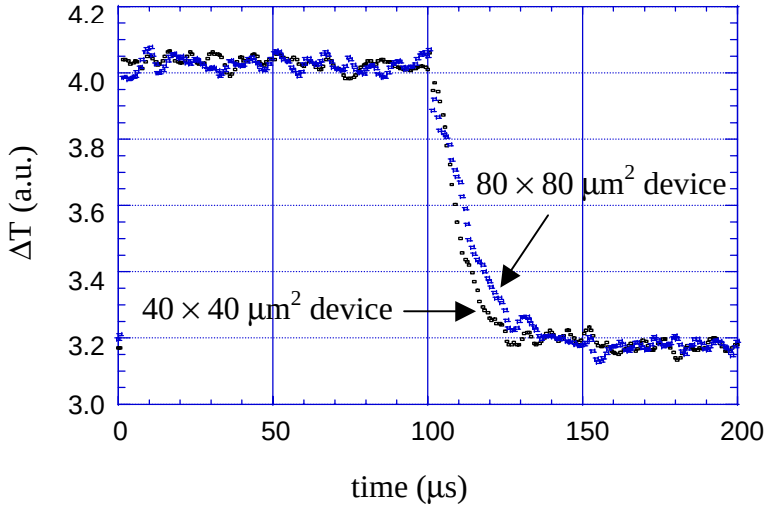


Figure 5.29 Measured transient response of $Si_{0.8}Ge_{0.2}$ microcoolers (sample HA00.034). The device sizes are 80×80 μm^2 and 40×40 μm^2. Measure by Fitting [50].

5.8 SiGe/Si microcooler optimization and results

The integrated SiGe/Si microcooler research started just about three years ago. There are a lot of room to improve the microcooler performance. The microcooler optimization includes the optimization of device structure, processing, packaging, materials, testing, etc. The testing methods have been discussed in Sections 5.5~5.7. In this section, we will discuss microcooler device and material issues.

5.8.1 Contact resistance minimization

As shown in Chapter 2, contact resistance is one of the main non-ideal effects that limit the performance of thin film microcoolers [51-53]. Contact resistance on the order of 10^{-7} Ωcm^2 or lower is required for micron thick microcoolers.

Contact resistance R_c can be expressed as

$$R_c = \frac{r_c}{A} \tag{5.8}$$

where r_c is the specific contact resistance and A is the contact area. Since the thermal resistance and electrical resistance of the TE leg are also scaled with the area A for usual cooler structures, specific contact resistance r_c is a better parameter to characterize the contact resistance.

Specific contact resistance between semiconductor and metal is related to the semiconductor material, its surface state and doping concentration, the metal used for contact, annealing temperature, etc. It can be measured with transmission line model (TLM) method [54].

We used 0.1 μm Ti / 1 μm Al as the contact metal. The specific contact resistance is measured by the TLM method on n-type and p-type Si samples with the doping of 1×10^{20} cm^{-3} and 2×10^{20} cm^{-3} respectively. They are annealed with strip annealer and rapid thermal annealer (RTA) for 5 seconds. The measured specific contact resistance is shown in Figure 5.15 with Ti/Al deposition with UCSB e-beam #1 at 2×10^{-6} torr. Although the annealing time at target temperature is 5 seconds here for both RTA and strip annealer, strip annealer actually has a longer annealing time than RTA due to its slow temperature rising and dropping time compared with those of RTA. Our experimental results shows the specific contact resistance is more repeatable for annealed with strip annealer than annealed with RTA.

Contact resistance is sensitive to the sample's surface state. Clean and oxide free surface is required for low contact resistance. Sample cleaning and oxide etch by HF are performed before metal deposition. During metal deposition, high vacuum is required for good ohmic contact. Figure 5.31 shows the measured specific contact resistance for Ti/Al or AlSi (1% Si) deposited

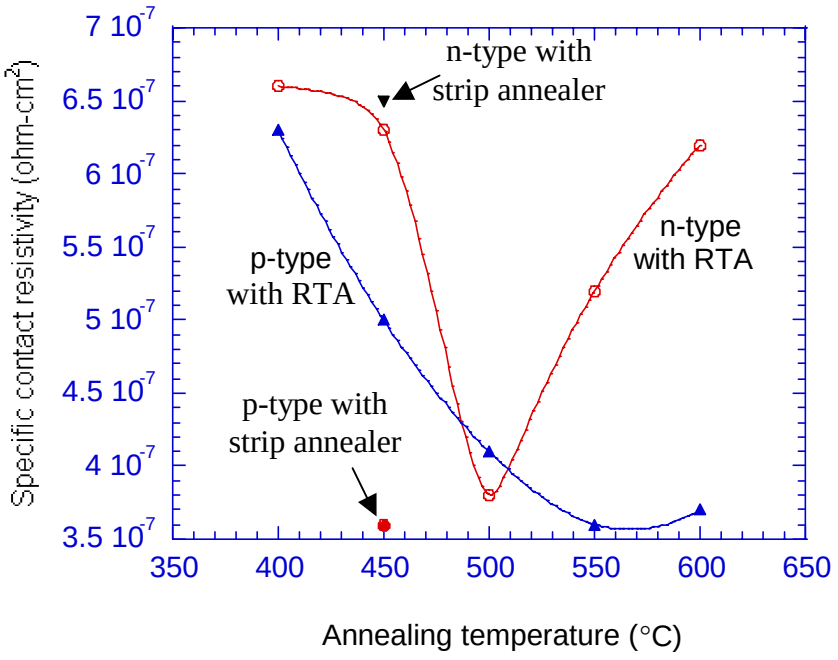


Figure 5.30 Measured specific contact resistance versus annealing temperature for Ti/Al contacts to n-type Si (1×10^{20} cm^{-3}) and p-type Si (2×10^{20} cm^{-3}). 0.1 μm Ti / 1 μm Al were deposited on the Si samples by UCSB e-beam #1 at about 2×10^{-6} torr. Samples were annealed for 5 seconds with RTA or strip annealer and measured by the TLM method.

with UCSB e-beam #3 at about 2×10^{-7} torr. Compared with Figure 5.12, it can be seen the specific contact resistivity decreased with increasing vacuum from 2×10^{-6} torr to 2×10^{-7} torr. For the contact metal, Ti/Al shows lower specific contact resistance than AlSi. Contact resistance as low as 7×10^{-8} Ωcm^2 was measured on the Ti/Al and p-type Si contact for 5 seconds annealing at 450 °

on the strip annealer. It can also be noticed that, for the samples we measured, p-type contact has a lower contact resistance than the n-type contact.

Regarding the doping in the semiconductor, generally the higher doping concentration the lower contact resistance due to the stronger band bending and carrier tunneling at the metal semiconductor junction. To minimize the contact resistance, the top layers of our microcooler samples are doped to the order of 10^{20} cm^{-3}.

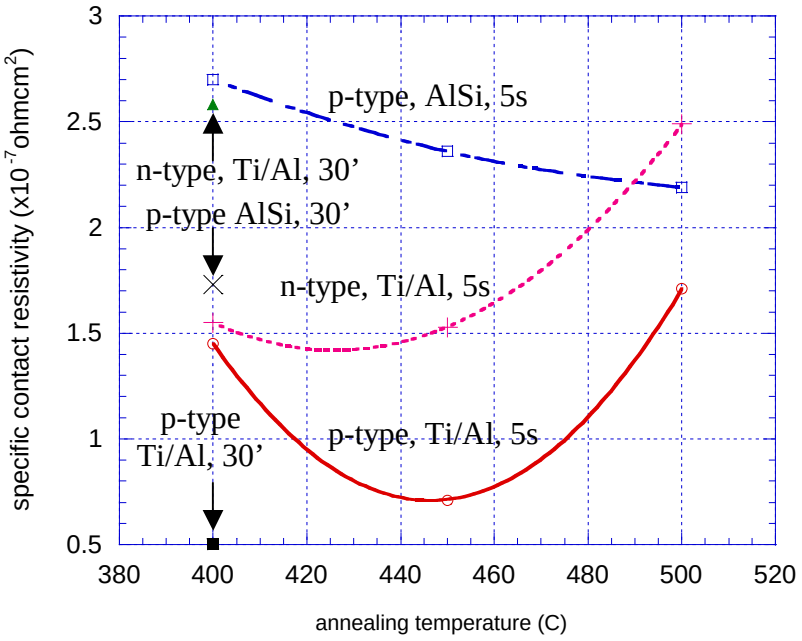


Figure 5.31 Measured specific contact resistance versus annealing temperature for Ti/Al and AlSi contacts to n-type Si (1×10^{20} cm^{-3}) and p-type Si (2×10^{20} cm^{-3}). 0.1 μm Ti / 1 μm Al or 1 μm AlSi (1% Si) were deposited on the Si samples by UCSB e-beam #3 at about 2×10^{-7} torr. Samples were annealed with the strip annealer.

In summary, low specific contact resistivity requires high doping concentration, clean sample surface, high vacuum metal deposition condition, suitable contact metal and good annealing condition. The typical metal contacts in our microcooler fabrication is Ti/Al contact annealed at 450 °C 5 seconds with strip annealer for both n- and p-type silicon-based microcooler samples. The specific contact resistivity is expected on the order of low 10^{-7} Ωcm^2.

To have low contact resistance, we used self-alignment method for mesa etch, in which the top contact metal was used as a mask for mesa etch so that the contact area is the same as the microcooler mesa area. To further reduce contact resistance, the "mushroom" structures similar to that in Figure 3.7 can be used to increase the contact area.

5.8.2 Microcooler metal contacts

We used two microcooler structures as described in section 5.2. One is the basic SiGe/Si microcooler, as shown in Figure 5.4, it uses direct probing or wire bonding to send current to the microcooler. Its limitations have been discussed in Section 5.5.1. In this structure, rectangular shape mesa is easier for thermocouple testing than square shape mesa with the same area.

The microcooler structure with integrated extended top metal contact (side contact), as shown in Figure 5.5, is a better choice for device minimization,

integration and testing. However, this microcooler structure is still a single element TE cooler structure, the joule heating and heat conduction from the side contact needs to be considered. Figure 5.32 shows three situations of the side metal contacts: smaller width than the cooler, same width as the cooler and larger width than the cooler. For smaller side contact width, there will be less heat conduction to the cooler but there will be more joule heating in the side contact; for larger side contact with, there will be more heat conduction to the cooler but there will be less joule heating in the side contact. The side contact width modeling has been discussed in reference [55]. The measured cooling of 60×60 μm^2 p-type SiGe/Si microcoolers (sample HA99.071) with different side contact pad widths is shown in Figure 5.33. The cooling ranges from 2.2 K to 2.5 K with side contact width of 100 μm, 75 μm, 60 μm, 50 μm and 40 μm. The best cooling is for side contact width 75 μm, but the differences are small.

5.8.3 N- and p-type cooler array

As an electrical device, TE coolers need electrical connections to send current to them. The cooler structure discussed in this chapter so far are single element cooler structures. In this case, the wire connection to the cold side of

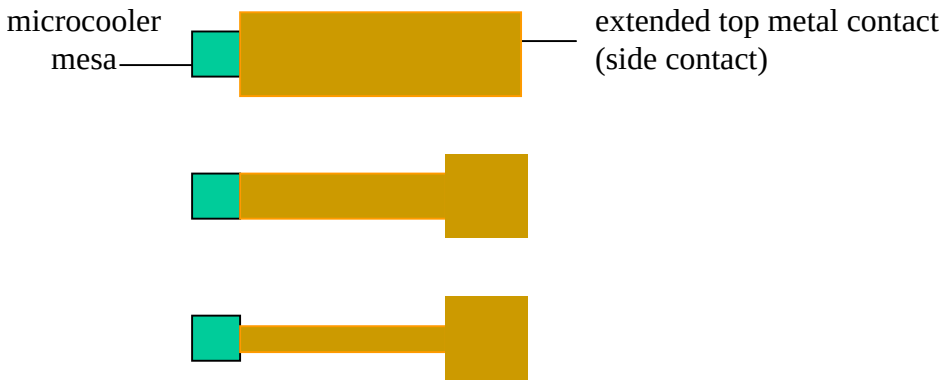


Figure 5.32 Microcooler top view with different extended top metal contact (side contact) width.

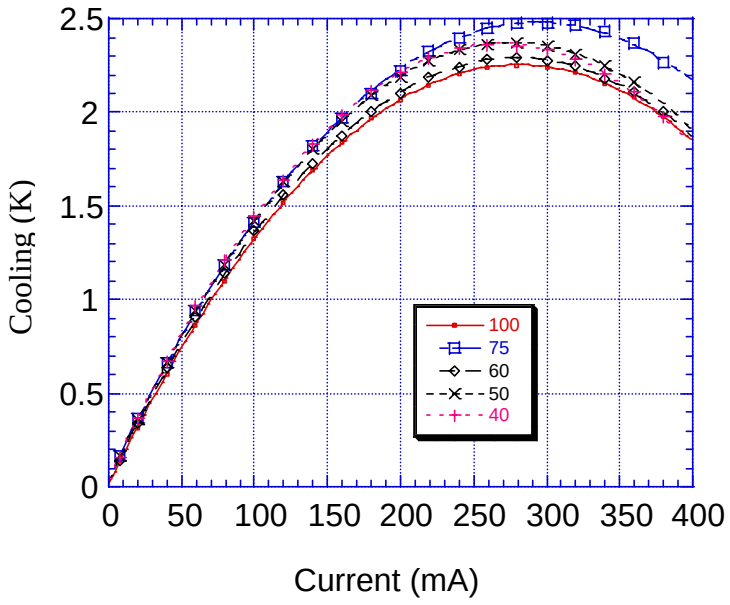


Figure 5.33 Measured cooling of 60 × 60 μm^2 p-type SiGe/Si microcoolers (sample HA99.071) with different side contact pad widths: 100 μm, 75 μm, 60 μm, 50 μm and 40 μm.

the cooler will work as a heat conduction and joule-heating source which will reduce the cooling performance. As mentioned in last section, with connection geometry changes, the joule-heating and heat conduction move at opposite direction and they can't be minimized at the same time.

The way to solve this problem is used n- and p-type cooler pair or array structure, like the commercial bulk TE coolers. Figure 5.34 shows a schematic diagram of a n- and p-type cooler pair. In this structure, n- and p-type coolers are connected electrically in series and thermally in parallel and the wire connections to the cooler are at the bottom metal contacts. The top contact metal is at the cold sides of the n- and p-type coolers, instead of one end at cold side and one end at the hot side in single element TE cooler structures, thus eliminating the heat conduction from the hot side of the cooler to the cold side. The joule heating in the top metal contacts can be minimized by reducing the n- and p-type cooler spacing and increase the contact metal thickness. To further expend this structure n- and p-type cooler arrays can be made to cool large areas and large heat load with relatively small currents.

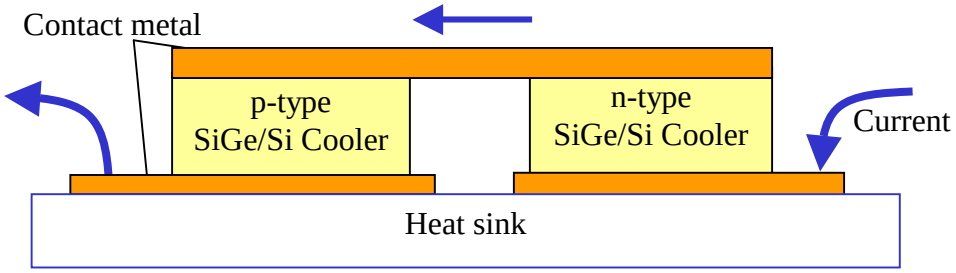


Figure 5.34 Schematic diagram of a n- and p- type cooler pair.

To make n- and p-type SiGe/Si microcooler pairs or arrays, it first requires that both n- and p-type coolers can work well individually. We have demonstrated both n-type and p-type SiGe/Si superlattice microcoolers. Figure 5.35 shows the measured cooling on n- and p-type SiGe/Si microcoolers at room temperature. The sample used are HA99.051 and HA99.071, they are 3 μm 200 × (5 nm $Si_{0.7}Ge_{0.3}$ / 10 nm Si) superlattices with doping of 2×10^{19} cm^{-3} (Sb) and 5×10^{19} cm^{-3} (B) respectively. Cooling of 2.3 K and 2.7 K are measured on 60×60 μm^2 device (n-type) and 50×50 μm^2 device (p-type) at 220 mA. For the cooler array, it is preferable to have n- and p-type devices working at the same optimal current. This can be done by selecting suitable device sizes for the cooler pair, as in Figure 3.35.

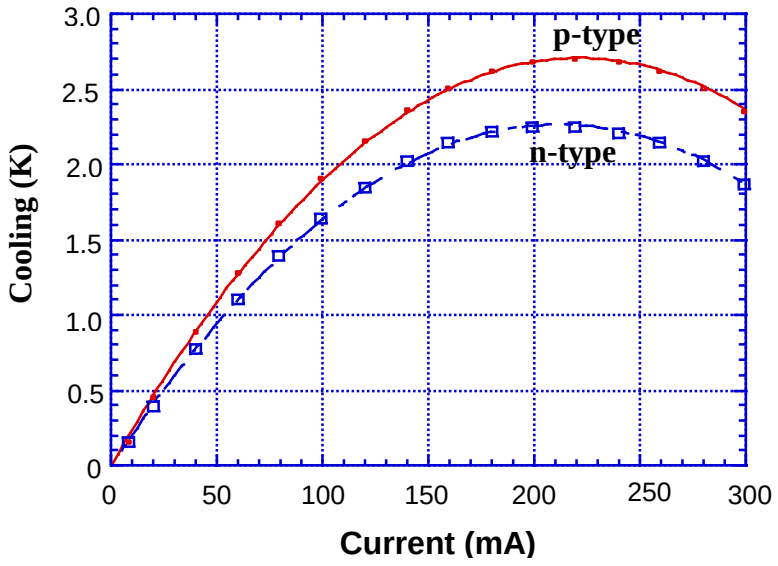


Figure 5.35 Measured cooling on n-type (60×60 μm^2, sample HA99.051) and p-type (50×50 μm^2, sample HA99.071) $Si_{0.7}Ge_{0.3}$/Si superlattice microcoolers at room temperature.

N- and p-type cooler pair was made in a structure similar to that in Figure 5.34. We put two individual n-type and p-type SiGe/Si superlattice microcoolers close to etch other on a heat sink and connected their top metal contacts together with wire bonding. Electrical current was sent to the microcoolers from the bottom contact of the n-type cooler to the bottom contact of the p-type cooler. The devices were tested with micro thermocouples at room temperature. However, we didn't get much cooling improvements from this configuration. One reason is the bonding wire was in the order of

millimeters and the joule heating in the wire is still a large heat source. The assembling of n- and p-type microcoolers will also greatly increase the microcooler packaging cost. Integrated n- and p-type cooler array is the preferred solution.

One possible monolithic integrated n- and p-type microcooler array structure is shown in Figure 5.36. SiGe or SiGe/Si superlattices are grown on silicon substrate. Using masking and ion implantations, n-type and p-type regions can be formed. Using proper etching and moralization, the monolithic integrated n- and p-type cooler array may be achieved.

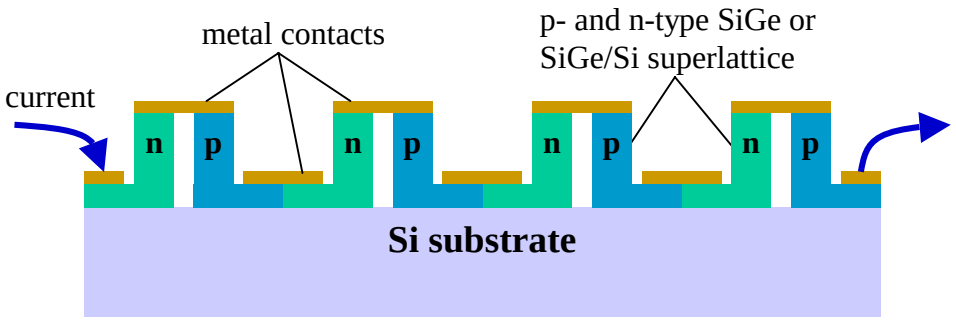


Figure 5.36 A possible structure for monolithically integrated n- and p-type SiGe/Si microcooler array. SiGe or SiGe/Si superlattices are grown on Si, n- and p-type regions are formed by ion implantation, mesas are form by etching.

5.8.4 Size effects

SiGe/Si microcoolers with different sizes were fabricated and tested. The device performance's size dependence was found. Figure 5.37 shows the thermocouple measured cooling on p-type $Si_{0.8}Ge_{0.2}$ microcooler (sample HA00.034) with size from 40×40 μm^2 to 150×150 μm^2 at room temperature. It can be observed that the maximum cooling is device size dependent. For the microcooler sample, at large device size, the maximum cooling temperature increases with decreasing the cooler size until about 60×60 μm^2, then it

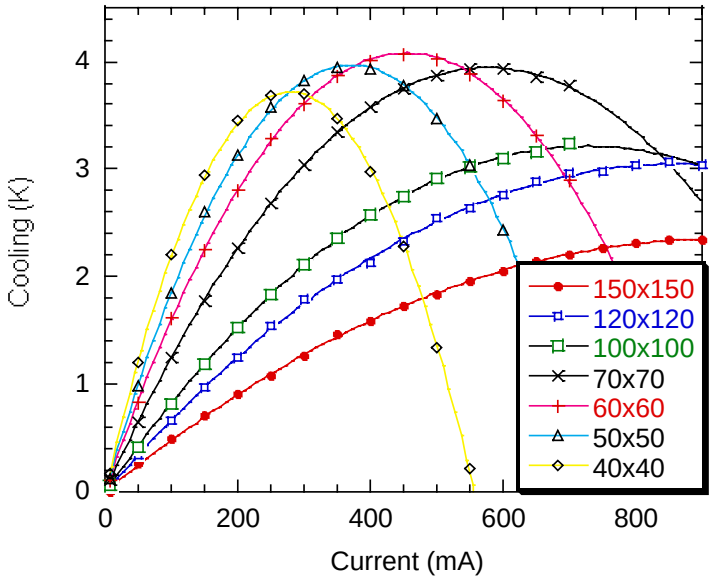


Figure 5.37 Measured cooling on p-type $Si_{0.8}Ge_{0.2}$ microcoolers (sample HA00.034) with various device sizes at room temperature. The mesa sizes of the coolers are: 40×40 μm^2, 50×50 μm^2, 60×60 μm^2, 70×70 μm^2, 100×100 μm^2, 120×120 μm^2 and 150×150 μm^2. The maximum cooling temperature varies with microcooler size.

begins to decrease with further dreading the device size. In this case, the optimal device size for maximum cooling is 60 × 60 μm^2, and maximum cooling over 4 K is measure at room temperature.

As shown in Figure 5.38, similar relation between maximum cooling and device size is measured on p-type SiGe/Si superlattice microcoolers (sample HA00.055). The superlattice structure is 200 × (12 nm $Si_{0.75}Ge_{0.25}$ / 3 nm Si). A

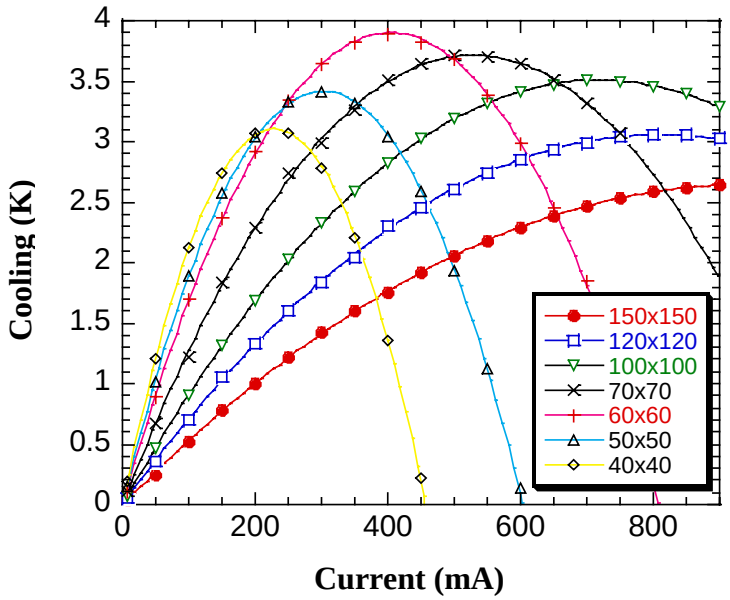


Figure 5.38 Measured cooling on p-type $Si_{0.75}Ge_{0.25}$/Si superlattice microcoolers (sample HA00.055) with various device sizes at room temperature. The mesa sizes of the coolers are: 40 × 40 μm^2, 50 × 50 μm^2, 60 × 60 μm^2, 70 × 70 μm^2, 100 × 100 μm^2, 120 × 120 μm^2 and 150 × 150 μm^2. The superlattice structure is 200 × (12 nm $Si_{0.75}Ge_{0.25}$ / 3 nm Si).

maximum cooling of 3.9 K is measured on 60 × 60 μm^2 device at room temperature. Depending the microcooler samples and device processing, the best device size for maximal cooling temperature varies from 40 × 40 μm^2 to100 × 100 μm^2 for thermocouple measurement. For devices smaller than 40 × 40 μm^2, other testing method such as thermoreflectance method should be used.

This device size dependence of maximum cooling can't be explained with conventional bulk TE cooler models. Without non-ideal effects, the TE cooler can be modeled as that in Chapter 2 and the maximum cooling can be expressed as $\Delta T_{max0} = \frac{1}{2} Z T_c^2$ (Equation 2.16), which is device size independent. If we add the non-ideal effect of electrical contact resistance into the device modeling, as in Chapter 3, the maximum cooling can be expressed as $\Delta T_{max} = \Delta T_{max0} \frac{1}{1 + 2\frac{r_c}{\rho d}}$ (Equation 3.12). Here r_c is the specific contact resistivity, ρ is the electrical resistivity of the TE leg and d the thickness of the TE leg. It can be seen that the maximum cooling decreases with increase contact resistance and reducing the cooler thickness, but it is still independent of the cooling area. The reason for this size independence of the cooling temperature is that the contact resistance, the thermal resistance of the TE leg

and the electrical resistance of the TE leg are all inversely proportional to the area of the cooler, the cooler area term is cancelled out in the maximum cooling temperature calculation. Other non-ideal effects are need to considered to explain the measured size effects on maximum cooling.

As discussed in Chapter 3, heat sink thermal resistance is an important non-ideal effect for microcoolers. Silicon substrate has good thermal conductivity (150 W/mK) compared with other common semiconductor materials, such as GaAs (46 W/mK) and InP (68 W/mK) [56]. However, due to the small thermal resistance of the thin SiGe or SiGe/Si superlattice film, the substrate thermal resistance can still be relatively large. For microcoolers, there is strong thermal spreading in the substrate and the substrate thermal resistance R_{th_sub} can be expressed as

$$R_{th\_sub} = \alpha \frac{\sqrt{\pi}}{4\kappa_{sub}\sqrt{A}} \tag{5.9}$$

where κ_{sub} is the thermal conductivity of the substrate, A is the device area; α is a modification factor for the finite thickness for the substrate and it depends on the thickness and thermal conductivity of the substrate, α=0.761 was reported on 125 μm thick InP substrate [52, 57]. It can be seen that the

substrate thermal resistance is inversely proportional to the square root of the area. This is different from the size dependence of the thermal resistance of the TE leg:

$$R_{th} = \frac{d}{\kappa A} \tag{5.10}$$

where R_{th} and κ is the thermal resistance and thermal conductivity of the TE leg, and d is the length of the TE leg. The ratio between the substrate thermal resistance and the TE leg thermal resistance can be expressed as:

$$\frac{R_{th\_sub}}{R_{th}} = \frac{\alpha\sqrt{\pi\kappa}}{4d\kappa_{sub}}\sqrt{A} \tag{5.11}$$

Its size dependence is shown in Figure 5.39 for α=0.8, κ=7 W/mK, κ_{sub}=150 W/cmK and d=3 μm. It can be seen that relative thermal resistance of the substrate is smaller for small devices, thus small devices should cool better.

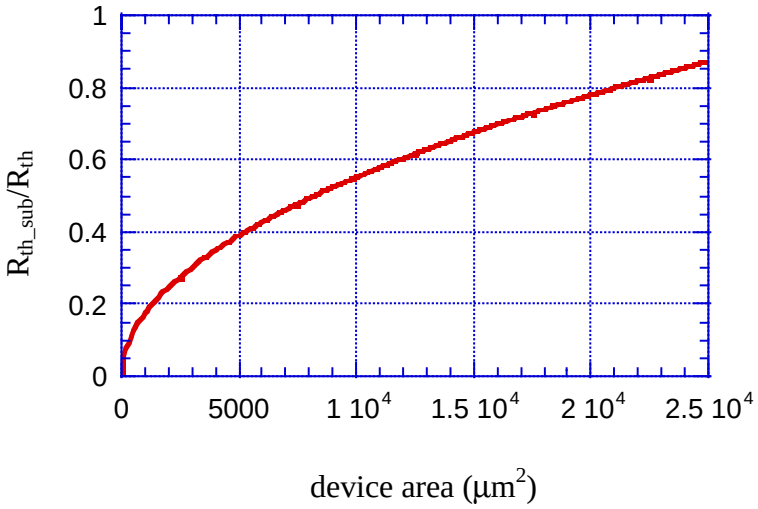


Figure 5.39 The ratio between the thermal resistance of the substrate and that of TE leg vs. device sizes. Assuming α=0.8, κ=7 W/mK, κ_{sub}=150 W/cmK and d=3 μm.

Another difference from conventional bulk TE coolers is that the microcoolers here are single element devices instead of the p- and n-type array structures. Heat conduction from the side contact to the cold junction of the cooler should also be considered. For the microcoolers in this work, the side contacts scale with the linear dimension of the cooler. Therefore the heat conduction is proportional to the square root of cooler area, with the cooling power in microcooler is proportional to the cooler area. This different size dependence in the cooler and the side contact makes larger devices tend to be

less affected by the conduction from the side. This can make larger devices cool better.

Thermocouple can also be a heat load to the microcooler. For the same size thermocouple, larger coolers should be less affected from the heat conduction from thermocouple. To eliminate the heat conduction from thermocouple, thermoreflectance method can be used. Figure 5.40 shows the thermoreflectance measurement result on p-type $Si_{0.75}Ge_{0.25}$/Si superlattice microcoolers (sample HA00.055). It also shows the cooling temperature decrease with very small devices, such as 10×10 μm^2 and 20×20 μm^2.

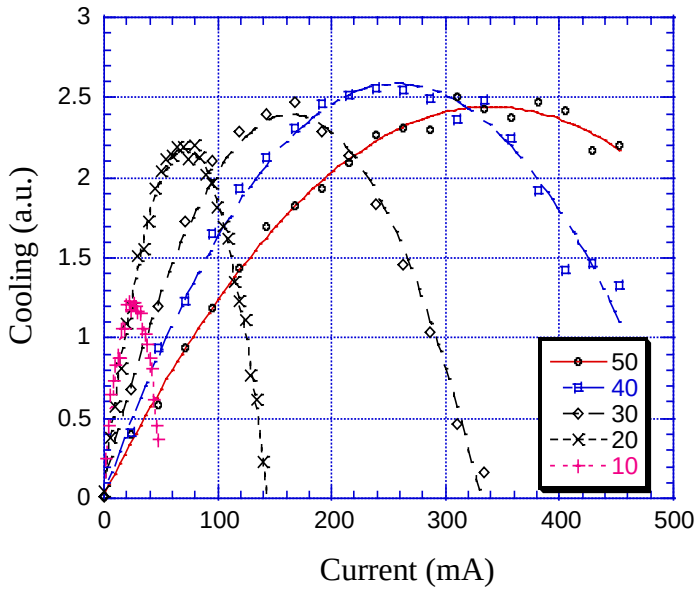


Figure 5.40 Measured relative cooling on p-type $Si_{0.75}Ge_{0.25}$/Si superlattice microcoolers (sample HA00.055) with thermoreflectance method at room temperature. The mesa sizes of the coolers are: 10×10 μm^2, 20×20 μm^2, 30×30 μm^2, 40×40 μm^2 and 50×50 μm^2. Measured by J. Christofferson.

Therefore, the size effects on maximum cooling of microcoolers come from the interplay of the non-ideal effects: non-ideal substrate heat sink, side contacts and heat conduction from thermocouples, etc. Taking these factors and contact resistance into account, Figure 5.41 shows the simulated cooling for $Si_{0.8}Ge_{0.2}$ microcooler by Daryoosh Vashaee. It fits the experimental results very well.

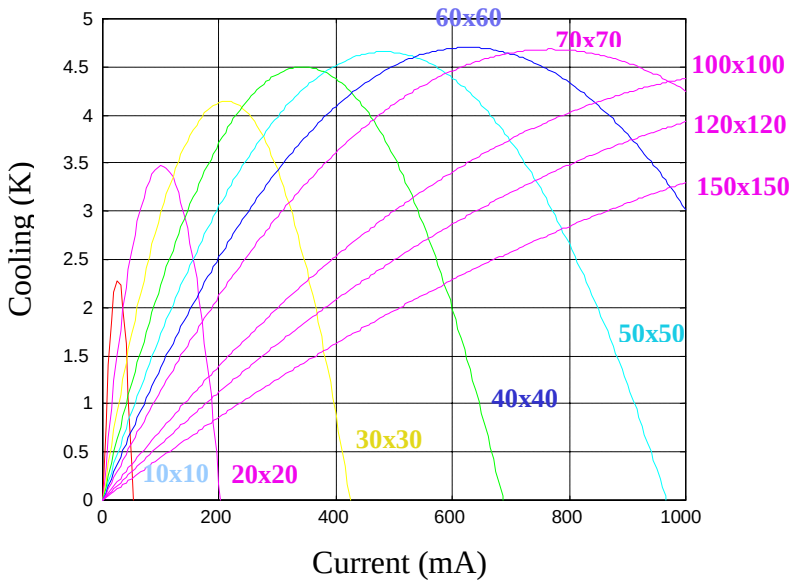


Figure 5.41 Simulated cooling on $Si_{0.8}Ge_{0.2}$ microcooler (sample HA00.034) with non-ideal effects taken into account. Calculated by D. Vashaee.

Size effects not only exist in the maximum cooling of microcoolers, but also exist in the maximum cooling power density. Figure 5.42 shows the measured maximum cooling power density on p-type $Si_{0.75}Ge_{0.25}$/Si superlattice microcooler (sample HA00.085) with various device sizes. Microcoolers were tested with micro thermocouple at heat sink temperature of 25 °C. The maximum cooling power is measured with the integrated metal wire as the heat load and is got from cooling vs. heat load curve at zero cooling temperature, as described in section 5.6. Strong device size dependence of the maximum cooling power density can be seen from Figure 5.42, smaller devices has larger maximum cooling power density. Similar size effects on cooling power is seen on other SiGe and SiGe/Si microcooler samples.

At $\Delta T = 0$, the maximum cooling power density q_{max} can be expressed as:

$$q_{max} = \frac{\Delta T_{max}}{AR_{th\_total}} \tag{5.12}$$

where R_{th_total} is an overall thermal resistance of the cooler, including TE leg thermal resistance R_{th}, substrate thermal resistance R_{th_sub} and side contact thermal resistance R_{th_side}. In the microcooler structures here, $R_{th}=\beta\sqrt{A}$, where β is a coefficient.

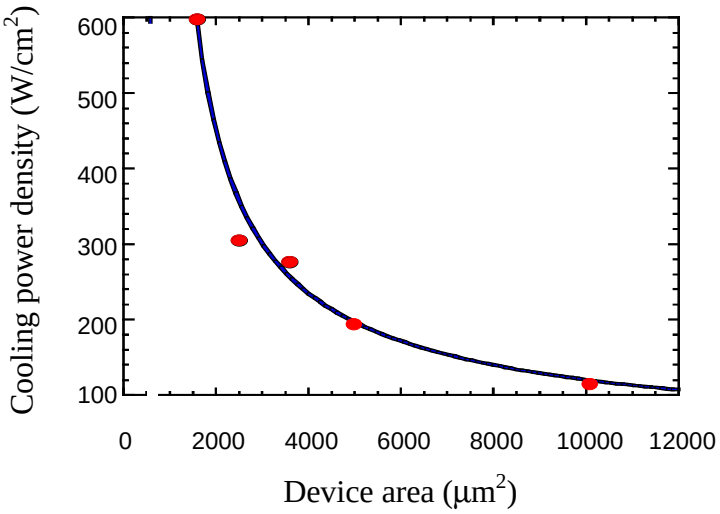


Figure 5.42 Measured maximum cooling power density on p-type $Si_{0.75}Ge_{0.25}$/Si superlattice microcooler (sample HA00.085) with various device sizes. Microcoolers were tested with micro thermocouples at heat sink temperature of 25 °C. The tested device sizes are: 40×40 μm^2, 50×50 μm^2, 60×60 μm^2, 70×70 μm^2 and 100×100 μm^2.

Substitute R_{th_side} and Equations 5.9 and 5.10 into Equation 5.12,

$$q_{max} = \frac{\Delta T_{max}}{\frac{d}{\kappa} + \alpha \frac{\sqrt{\pi}}{4\kappa_{sub}}\sqrt{A} + \beta\sqrt{A}}$$

$$= \frac{\Delta T_{max}}{a\sqrt{A} + b} \qquad (5.13)$$

where a = $\alpha \frac{\sqrt{\pi}}{4\kappa_{sub}} + \beta$, b = $\frac{d}{\kappa}$. For the same maximum cooling temperature, smaller device has larger cooling power density. Cooling power density may have stronger size dependence than cooling temperature.

5.8.5 Material optimization

Figure of merit of the TE material is the determining factor for the microcooler device performance. It sets the up limits for the largest possible cooling temperature, cooling efficiency, etc. Improving ZT is the most effective and fundamental way to get better cooling. The ZT of TE materials depends on the material composition, doping and quality etc. For superlattice materials, ZT also depends on the superlattice periods and band structures.

Figure 5.43 shows the measured maximum cooling temperature for different doping in p-type 3 μm 200 × (5 nm $Si_{0.7}Ge_{0.3}$ / 10 nm Si) superlattice microcoolers. They were measured with micro thermocouples at the heat sink temperature of 25 °C. With increasing the doping concentration, electrical conductivity increases, while Seebeck coefficient decreases. Therefore, there is an optimal doping. For microcoolers, the contact resistance has larger adverse impact on smaller cooler resistance and this may make the optimal doping

smaller than that of bulk TE coolers. From Figure 5.43, the optimal doping is in between 5×10^{19} cm^{-3} and 1×10^{20} cm^{-3}.

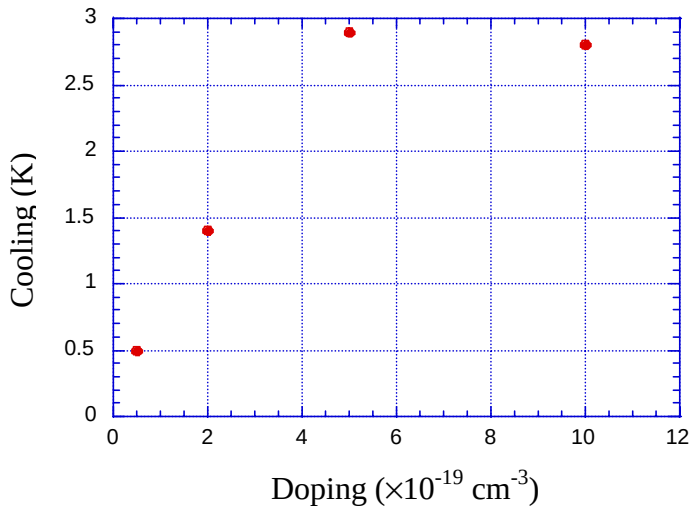


Figure 5.43 Measured maximum cooling temperature for different doping in p-type 3 μm 200 × (5 nm $Si_{0.7}Ge_{0.3}$ / 10 nm Si) superlattice microcoolers at the heat sink temperature of 25 °C.

The room temperature cooling vs. SiGe/Si superlattice periods is shown in Figure 5.44. The samples are 3 μm p-type $Si_{0.7}Ge_{0.3}$/Si superlattices with a layer thickness ratio of 1:2, their average lattice constant is that of $Si_{0.9}Ge_{0.1}$ alloy. The superlattice periods are 4.5 nm, 7.5 nm, 12 nm, 15 nm and 30 nm with the same doping 5×10^{19} cm^{-3}. Maximum cooling from 2.5 K and 3.2 K were measured on these samples, and period from 7.5 nm to 15 nm has relatively good cooling.

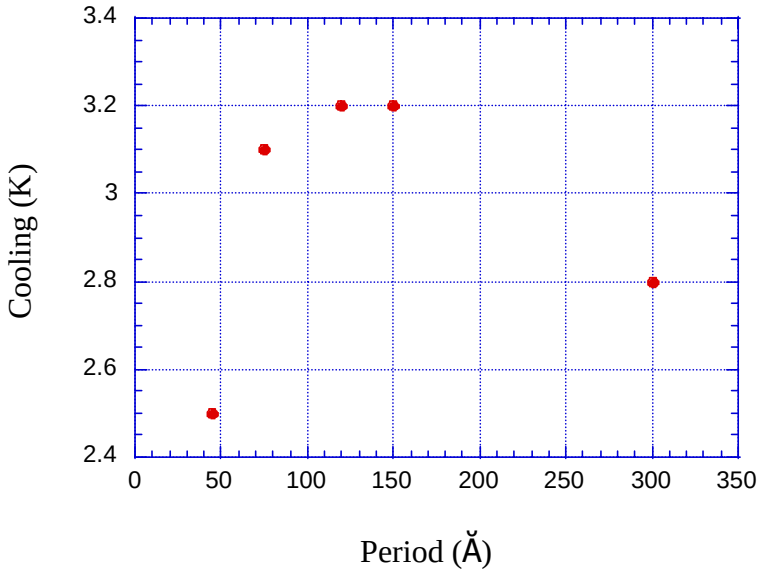


Figure 5.44 Measured cooling vs. $Si_{0.7}Ge_{0.3}$/Si superlattice periods at room temperature. The layer thickness ratio between $Si_{0.7}Ge_{0.3}$ and Si is 1:2 for the superlattices, they grown on $Si_{0.9}Ge_{0.1}$ buffer layers.

Material composition is one of the main factors in controlling the ZT of the material. Figure 5.45 shows the measured cooling on p-type SiGe/Si microcoolers with three different compositions: (a) sample HA99.095: p+ Si substrate; (b) sample HA00.037: 3 μm 200 × (12 nm $Si_{0.75}Ge_{0.25}$ / 3 nm Si) superlattice, its average composition is corresponding to $Si_{0.9}Ge_{0.1}$; (c) sample HA00.055 3 μm 200 × (12 nm $Si_{0.75}Ge_{0.25}$ / 3 nm Si) superlattice, its average composition is corresponding to $Si_{0.8}Ge_{0.2}$. The devices are tested with micro thermocouple at a heat sink temperature of 25 °C. Cooling of 3.2 K and 4.2 K

was measure on SiGe/Si sample HA00.037 and HA00.055, while only 1 K cooling is measured on the bare silicon sample. Silicon is a poor thermal electric material because of it large thermal conductivity. With SiGe and SiGe/Si superlattice, the thermal conductivity is reduce by alloy scattering and phonon interface scattering, thus better TE performance. The results also show higher Ge amount has better cooling, like $Si_{1-x}Ge_x$ alloys with $x \leq 0.3$.

Unlike conventional bulk TE coolers, the maximum cooling of microcoolers depends not only on the ZT of the material, but also on the geometry of the microcooler. The cooling area's size effects have been discussed in the last section. Figure 5.46 shows the measured cooling on p-type 4nm $Si_{0.7}Ge_{0.3}$ / 8nm Si superlattice microcoolers with different superlattice thickness at the heat sink temperature of 25 °C. The superlattices are doped at 5×10^{19} cm^{-3}, the zero thickness data point is for p+ Si substrate. Generally, the maximum cooling is less by non-ideal effects such as contact resistance and non-ideal heat sink for thicker microcoolers. This can seen in the cooling increase form 1 μm thickness to 3 μm thickness. We expected the cooling would further increase for 6 μm superlattice sample, but it didn't. This may come from the material growth difficulties in the thick superlattice grown, the superlattice quality may degraded during the several days long growth period

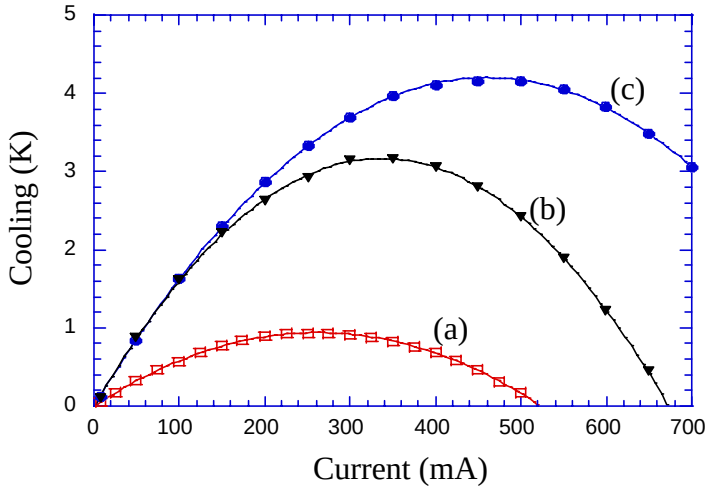


Figure 5.45 Measured cooling on p-type 60 × 60 μm SiGe/Si microcoolers with three different compositions: (a) sample HA99.095: p+ Si substrate; (b) sample HA00.037: 3 μm 200 × (12 nm $Si_{0.75}Ge_{0.25}$ / 3 nm Si) superlattice, Na = 5×10^{19} cm^{-3}; (c) sample HA00.055 3 μm 200 × (12 nm $Si_{0.75}Ge_{0.25}$ / 3 nm Si) superlattice, Na =$5\sim7\times10^{19}$ cm^{-3}.

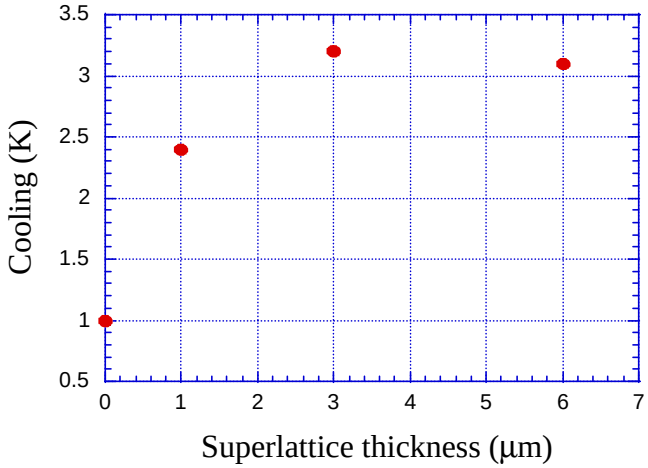


Figure 5.46 Measured cooling on p-type 4nm $Si_{0.7}Ge_{0.3}$ / 8nm Si superlattice microcoolers with different thickness at the heat sink temperature of 25 °C. The superlattices are doped at 5×10^{19} cm^{-3}, the zero thickness data point is for p+ Si substrate.

and reduce it cooling performance. Based on this result, 3 μm superlattices were used for most of our microcooler samples.

5.8.6 Cooling vs. temperature

SiGe is a good thermoelectric material for high temperature applications [4]. Its ZT increases with temperature until about 900 °C. Better cooling performance can be expected for SiGe and SiGe/Si superlattice microcooler at increased temperature.

Figure 5.47 shows the measured cooling on 60 × 60 μm^2 p-type 200 × (12 nm $Si_{0.75}Ge_{0.25}$ / 3 nm Si) microcoolers (sample HA00.055) at various heat sink temperatures. The maximum cooling increased from 4.2 K at 25 °C to over 12 K at 200 °C. Similar temperature dependence of the cooling temperature was measured on other samples also. Figure 5.48 shows the measured cooling on 50 × 50 μm^2 p-type $Si_{0.8}Ge_{0.2}$ microcoolers (sample HA00.034). It maximum cooling temperature increased from 4.3 K at heat sink temperature 25 °C to 13.8 K at heat sink temperature 250 °C. This increased cooling is related to the TE property improvements in SiGe and SiGe/Si superlattice with increasing the temperature.

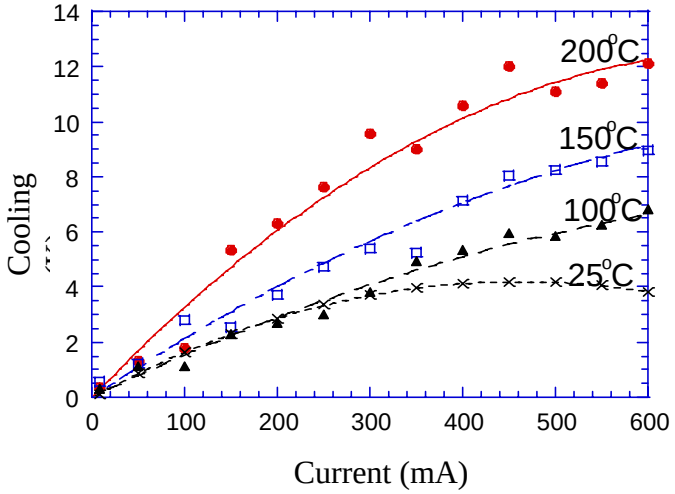


Figure 5.47 Measured cooling on 60 × 60 μm^2 p-type $Si_{0.75}Ge_{0.25}$/Si microcoolers (sample HA00.055) at various heat sink temperatures.

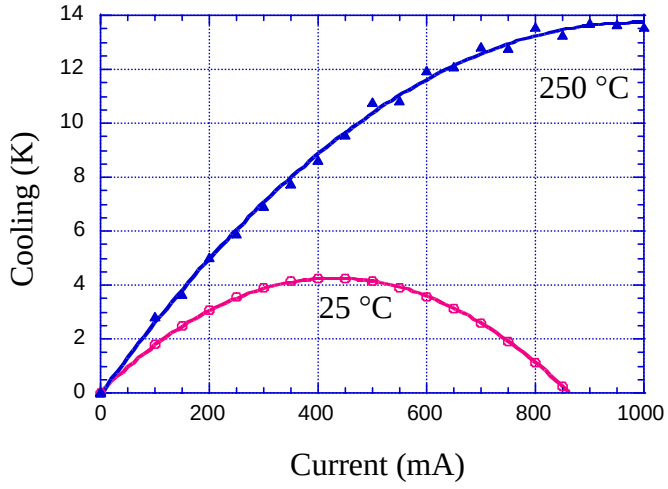


Figure 5.48 Measured cooling on 50 × 50 μm^2 $Si_{0.8}Ge_{0.2}$ microcoolers (sample HA00.034) at heat sink temperature of 25 °C and 250 °C.

5.9 Discussion

It can be seen from Figures 5.47 and 5.48 that over 4 K cooling is measured on both SiGe and SiGe/Si superlattice samples. This is over four-fold improvement over silicon microcooler that are fabricated with similar processing. (See Figure 5.45) However, it still not high enough for practical applications. In this section, we will discuss its limiting factors.

First, the maximum cooling depends on the material's TE figure of merit ZT. For sample HA00.034 $Si_{0.8}Ge_{0.2}$, its ZT can be estimated to about 0.08 at 25 °C from the TE properties measured in Chapter 4. In the ideal cooler model, its maximum cooling will be $\frac{1}{2}ZT^2$ = 12 K at room temperature, which is much larger than the measured 4.3 K cooling on 50×50 μm^2 microcoolers. This cooling reduction comes from the non-ideal effects, such as the contact resistance, non-ideal heat sink and the heat conduction from the connecting wire, etc.

Since the devices here are single element microcoolers, heat conduction to the cooling side from the bonding wires, probes or side contact is unavoidable. This can work as a heat load to the microcooler in two folds: Joule heating in the wire and heat conduction. Reducing the wire cross-section area and increasing the wire length can reduce the heat conduction, but that will increase

the joule heating in the wire. For a certain wire material, reducing the joule heating will increase the heat conduction and reducing the heat conduction will increase the joule heating. So the heat conduction from the wire can put a limitation to the cooler performance. As shown in Figure 5.49, this can be modeled with the two-leg TE cooler model, one leg is the TE material and the other is the metal wire.

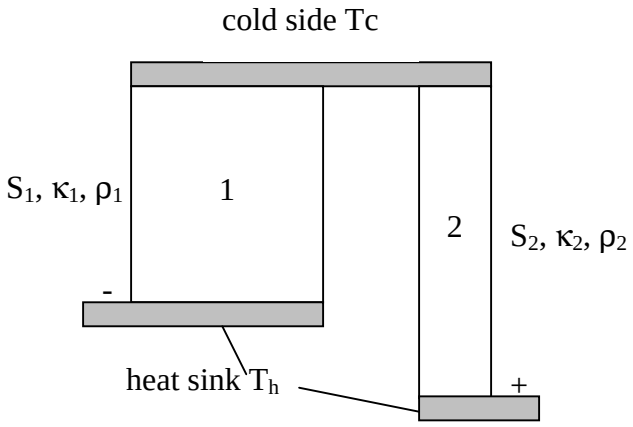


Figure 5.49 Two-leg TE cooler. In the single element cooler structure, the TE material can be regarded as leg 1 and the metal wire as leg 2.

It can be shown that under optimized geometry of the TE legs, the effective figure of merit can be expressed as [58]:

$$Z = \frac{(S_1 - S_2)^2}{(\sqrt{\kappa_1 \rho_1} + \sqrt{\kappa_2 \rho_2})^2} \tag{5.14}$$

For the metal connection wire, $S_2 = 0$. The effective Z can be rewritten as,

$$Z = \frac{S_1^2}{(\sqrt{\kappa_1 \rho_1} + \sqrt{\kappa_2 \rho_2})^2} = \frac{Z_1}{(1 + \sqrt{\frac{\kappa_2 \rho_2}{\kappa_1 \rho_1}})^2} \tag{5.15}$$

where $Z_1 = \frac{S_1^2}{\kappa_1 \rho_1}$ is the figure of merit of the TE leg, SiGe or SiGe/Si superlattice in our case. It can be seen that its effective Z is reduce by the metal wire connection, and small $\kappa_2\rho_2$ is preferred for efficient cooling. Table 5.2 shows the Z/Z_1 for two conditions: (a) κ_1=7 W/mK and ρ_1=0.003 Ω-cm and (b) κ_1=5W/mK and ρ_1=0.001 Ω-cm

Table 5.2 Effective figure of merit of single element TE cooler structure: (a) taking κ_1=7 W/mK and ρ_1=0.003 Ω-cm and (b) taking κ_1=5W/mK and ρ_1=0.001 Ω-cm.

metal	κ (W/cm•K)	ρ (Ω•cm)	ρ•k(WΩ/K)	Z/Z_1 (a)	Z/Z_1 (b)
Ag	4.27	1.629×10^{-6}	6.96×10^{-6}	0.716	0.530
Al	2.37	2.828×10^{-6}	6.70×10^{-6}	0.720	0.536
Au	3.18	2.44×10^{-6}	7.76×10^{-6}	0.704	0.515
Cu	4.01	1.742×10^{-6}	6.91×10^{-6}	0.716	0.531

The calculation results shat that depends on the thermoelectric properties of the TE material of the single element cooler, the side contact will cause about 30% to 50% figure of merit reduction. As discussed in Chapter 3, contact resistance can another 20% to 40% reduction in maximum cooling, plus the non-ideal heat sink, the measured cooling is much less than the ideal case.

The microcooler performance can be improve by using materials with higher ZT, using n- and p-type cooler array structure, further reducing contact resistance and improving the heat sink, etc.

5.10 Summary

A thorough experimental investigation of SiGe/Si microcoolers has been presented. Integrated SiGe/Si microcoolers as small as 10×10 μm^2 were fabricated with standard IC processing technology on five-inch diameter silicon wafers. Several testing methods have been explored for the microcooler characterization. Both n- and p-type SiGe/Si microcoolers were demonstrated, which paves the road to make n- and p-type microcooler arrays. Cooling up to 4.3 K and 13.8 K was measured on 50×50 μm^2 SiGe microcoolers. Thin film metal resistors were integrated the microcoolers for cooling power density and

cooling temperature characterization. Cooling power density up to 600 W/cm^2 was measured at room temperature, which is over one order larger than that of conventional bulk TE coolers. The microcooler transient response time as small as 20~30 μs was measured, this is over 10000 times faster than bulk TE coolers [13].

The device size effects on cooling temperature and cooling power density were found and discussed. The microcooler performance is limited by some non-ideal effects such as contact resistance, heat conduction from the metal wire contacts, non-ideal heat sink etc. With further device optimization, such as using integrated n- and p-type microcoolers in an array format electrically in series and thermally parallel, larger cooling can be achieved.

SiGe/Si superlattices with various doping, periods, composition and thickness were studied for spot cooling. Although over four-fold cooling temperature improvement over silicon was measured, the device performance difference between superlattice and SiGe alloy is small. We had hoped to improve the microcooler performance with thermionic emission and thermal conductivity reduction in superlattices. However, this is not fully realized for two reasons. First, with material growth limitations, our samples are either uniformly doped or in a doped/undoped format. This makes the effective barrier either too small or too big for optimal thermionic emission. Second, due

to the composition closeness between SiGe and Si, the interface phonon scattering between SiGe and Si is not as strong as that between Ge and Si. Thermal conductivity smaller than the SiGe/Si average was measured, but there was no significant reduction from that of SiGe alloy. These can be improved by modulation doping and using Si/Ge superlattice, etc.

With further material and device optimization, it is possible to monolithically integrate SiGe/Si microcoolers with Si microelectronics for localized cooling and temperature control.

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Chapter 6

SiGeC/Si microcoolers

6.1 Introduction

SiGe and SiGe/Si superlattices are promising materials for integrated localized cooling. Their microcoolers with large cooling power density and fast response speed have been presented in Chapter 5. However, SiGe has a larger lattice constant than that of Si and strain is present in SiGe/Si systems [1, 2]. This strain limits the thickness of strained layers. If the thickness of strained layers exceeds the critical thickness, dislocations and other extended defects will be generated and the material quality will be degraded, which will lower the carrier mobility and produce more Joule heating in the cooler devices. The critical thickness for strained $Si_{1-x}Ge_x$ on unstrained silicon substrate at (001) direction is on the order of one to one hundred nm depending on the Ge concentration. To avoid material quality degradation, the strained layer thickness should be below the critical thickness. For cross-plane transport microcoolers, as discussed in Chapter 3, the device performance is more affected by the non-ideal effects, such as contact resistance, for thinner TE

material thickness. This critical thickness is too thin to make high performance SiGe microcoolers directly on silicon substrates. One way to solve this problem is to use buffer layers, such as SiGe/SiGeC or graded SiGe, for unstrained SiGe or strain compensated SiGe/Si superlattice growth. This is the approach we used for the SiGe/Si microcooler materials in Chapter 5. SiGe and SiGe/Si superlattices on the order of several microns thick were grown on buffer structures and microcoolers were demonstrated with them. However, the buffer structures also increase the cost of material growth and the complexity of integration with silicon microelectronics. By adding a small amount of carbon into the SiGe material system, strain can be adjusted due to the small lattice constant of carbon. By properly selecting the Ge and C ratio, SiGeC can be lattice matched to silicon, and thick SiGeC or SiGeC/Si superlattice can be directly grown on Si without buffer layers.

SiGeC and SiGeC/Si superlattices are important semiconductor materials recently developed for high performance microelectronics compatible with Si technology [3-7]. We are the first to apply this material system to integrated microcooler study. This chapter describes the fabrication and characterization of SiGeC and SiGeC/Si superlattice microcoolers, their potential for practical applications are discussed at the end.

6.2 SiGeC and SiGeC/Si superlattice materials

6.2.1 Lattice constant and band structure

The covalent radius of carbon (0.77 Å) are much smaller than those of silicon (1.17 Å) and Ge (1.22 Å) [8]. Adding Ge into Si lattice can cause compressive stress, while adding C into Si lattice can cause tensile stress. By adjusting the Ge and C ratio, it is possible to form strain-compensated $Si_{1-x-y}Ge_xC_y$ with lattice constant matching that of unstrained silicon.

According to Vegard's law, the lattice constant of $Si_{1-x-y}Ge_xC_y$ can be expressed as

$$a(x,y) = (1-x-y)a_{Si} + xa_{Ge} + ya_C \tag{6.1}$$

where a_{Si} = 5.442 Å, a_{Ge} = 5.672 Å and a_C = 3.571 Å, they are the lattice constants for silicon, germanium and diamond respectively at 300 K. This results in a Ge:C ratio of 8.2 for complete strain compensation. However, experimental results and more comprehensive modeling show some deviation from Vegard's law on $Si_{1-x-y}Ge_xC_y$ materials [9, 10]. A Ge:C ratio of 12 is

reported in reference [9] for matching the lattice constant of silicon. $Si_{0.89}Ge_{0.10}C_{0.01}$ was used in this work for SiGeC/Si microcooler study.

Adding C into SiGe changes not only the strain and lattice constant, but also the band structure [8, 11-17]. Experimental measurements of the band gap for $Si_{1-x-y}Ge_xC_y$ compressively strained to Si (001) indicate that incorporation of C into $Si_{1-x-y}Ge_xC_y$ increase the band gap by 21~26 meV/%C. Additional measurements have shown a reduction in $Si_{1-x-y}Ge_xC_y$/Si valence-band offset and an increase in conduction-band offset with C incorporation into $Si_{1-x-y}Ge_xC_y$ alloys under compressive strain. One reported measurement result of $Si_{1-x-y}Ge_xC_y$ and $Si_{1-x}Ge_x$ band-edge energies is shown in Figure 6.1. SiGeC/Si heterostructure compared with SiGe/Si structure has a larger conduction band offset. The main band offset still lies in the valence band. This makes it possible to use thermionic emission to enhance the TE cooling for both n- and p-type SiGeC/Si materials.

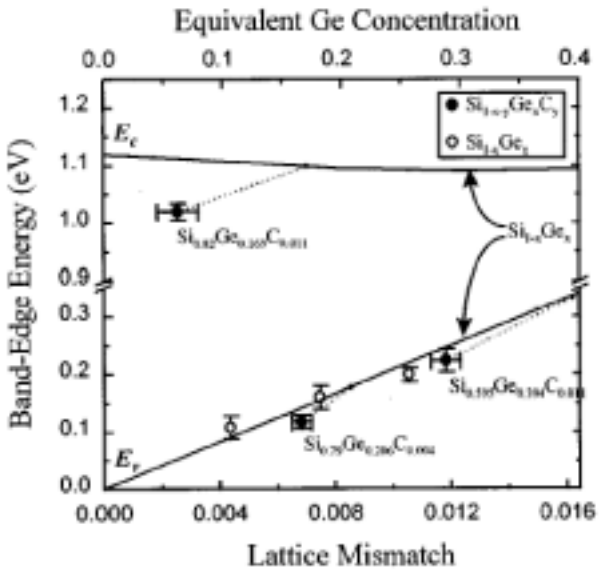


Figure 6.1 Valence- and conduction-band-edge energies as a function of lattice mismatch and equivalent Ge concentration for $Si_{1-x}Ge_x$ (open circles) and $Si_{1-x-y}Ge_xC_y$ (closed circles). The solid lines represent interpolated band-edge energies for $Si_{1-x}Ge_x$, and the dotted lines indicated the effect of C incorporation into a $Si_{1-x-y}Ge_xC_y$ alloy with fixed Ge concentration. From Stein [8].

6.2.2 Material growth

The SiGeC and SiGeC/Si superlattice were grown by Dr. Edward Croke in HRL Laboratory. The samples were grown in a Perkin-Elmer Si molecular beam epitaxy system capable of codepositing Si, Ge and C onto 5-inch Si substrates. Solid Si, Ge and C were evaporated through the use of e-beam

sources controlled by electron impact emission sensors (Si, Ge) and by monitoring atomic mass unit 36 (C_3) with a quadrupole mass spectrometer (C). Prior to loading into the MBE system, 125 mm diameter, (001)-oriented Si substrate, doped to <0.005 Ω cm with As, was striped using 5% hydrogen fluoride. After rinsing with deionized water, the wafer was loaded in the MBE chamber. In order to remove any remaining oxide and to prepare the sample for epitaxial growth, the substrate was heated to 850 °C and exposed to a 0.2 Å/s Si flux for 30 s.

A cross-sectional transmission electron microscopy image of a grown SiGeC/Si superlattice cooler sample (HA99.089) is shown in Fig. 6.2. The structure consisted of a 2 μm thick $Si_{0.89}Ge_{0.10}C_{0.01}$/Si superlattice (100 periods, each sub-layer 10 nm in thickness) grown at 500 °C, lattice-matched to the Si substrate. The superlattice was doped with Sb to approximately 2×10^{19} cm^{-3}. To reduce the device electrical contact resistance, the sample was capped with 100 nm Si: Sb, grown at 460 °C and doped to approximately 1×10^{20} cm^{-3}.

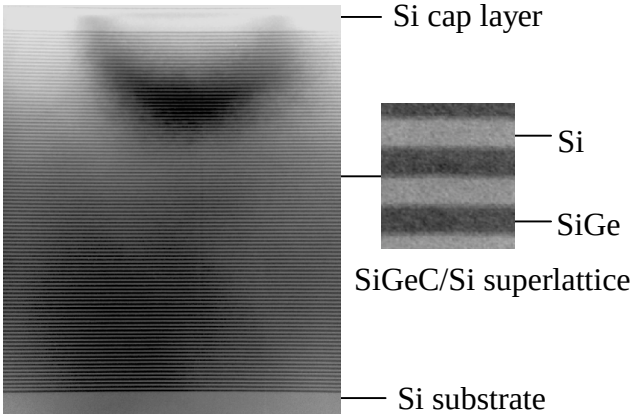


Figure 6.2 Cross-sectional TEM image of a MBE grown SiGeC/Si superlattice microcooler sample (HA99.089). The top is 100 nm Si cap layer; the middle is 2 μm superlattice of 100 × (10 nm $Si_{0.89}Ge_{0.10}C_{0.01}$ / 10 nm Si); the bottom is the Si substrate. An enlarged superlattice image is shown on the right-hand side.

6.3 Device structure and processing

The SiGeC/Si microcooler structure is about the same as that of SiGe/Si microcooler described in chapter 5, except it has no buffer layers. The schematic diagram of the cooler device structure is shown in Figure 6.3. This is a single element TE cooler structure with cross-plane transport. For n-type

microcooler, the current goes from the bottom metal contact to top metal contact for device cooling. For wire connection, the extended top metal contact (side contact) structure, as shown in Figure 6.4, can also be used in the SiGeC/Si microcooler structure to facilitate device integration and testing.

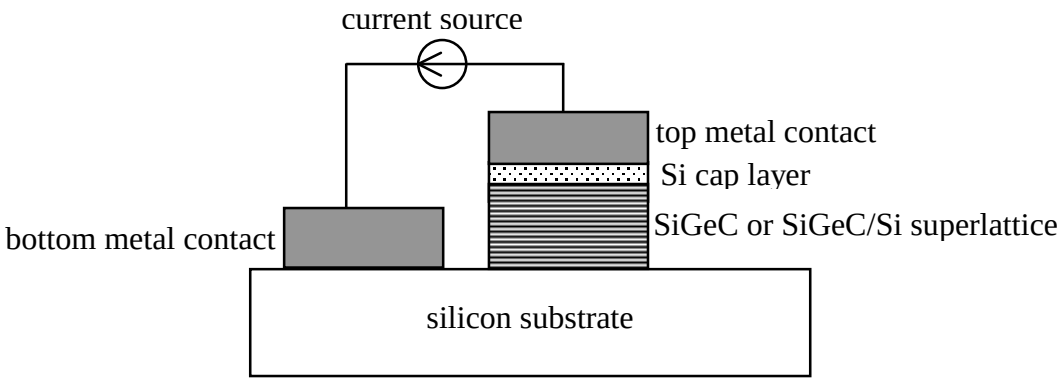


Figure 6.3 Schematic diagram of SiGeC/Si microcoolers (not to scale).

The processing of SiGeC/Si microcoolers is compatible with silicon integrated circuit fabrication process. Microcoolers were thermally isolated by dry etching mesa structures down to the n^+ Si substrate. Metallization was made on the mesa and the Si substrate for top and bottom contacts respectively. The main part of the cooler structure is the SiGeC or SiGeC/Si superlattice

layer. Its low cross-plane electrical resistance requires low contact resistance for optimum device performance [18]. Ti/Al metallization was used for ohmic contact. This was followed by annealing at 450 °C for 5 seconds. Specific contact resistivity of 1.5×10^{-7} Ω-cm^2 was measured by translation line model (TLM) method. To facilitate sending current to the cooler and device testing, Ti/Au was deposited for the extended top metal contact after a PECVD SiN_x passivation step, as shown in Figure 6.4.

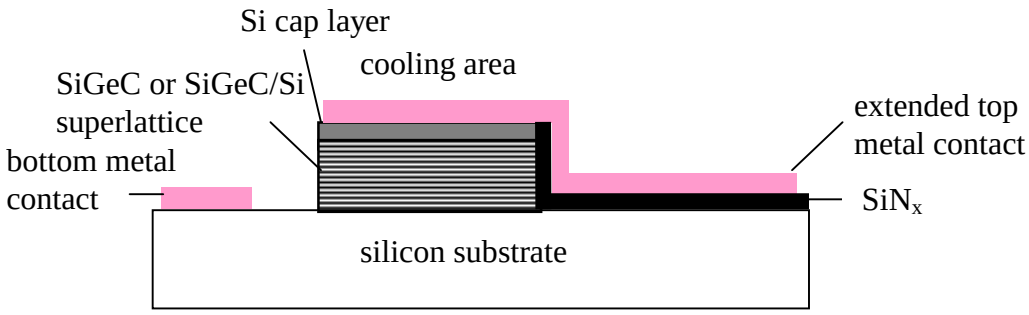


Figure 6.4 SiGeC/Si microcooler with extended top metal contact (side contact).

6.4 Device testing and results

N-type $Si_{0.89}Ge_{0.10}C_{0.01}$ and $Si_{0.89}Ge_{0.10}C_{0.01}$/Si superlattice microcoolers with various device sizes were fabricated. Since their device structures are similar to those of SiGe/Si microcoolers, the device characterization methods in chapter 4 can also be applied to SiGeC/Si microcoolers. Cooling temperature and cooling power were measured on SiGeC/Si microcoolers with micro thermocouples and integrated metal resistor method respectively.

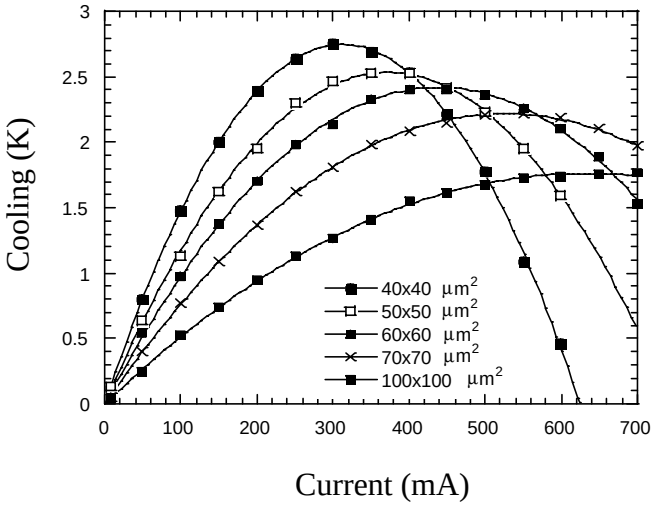
6.4.1 Cooling temperature

SiGeC and SiGeC/Si superlattice microcoolers were tested on a temperature-controlled heat sink, which was set at a constant temperature during device testing. Device cooling was measured with micro thermocouples on top of the device and was relative to the values at zero current. The tested device sizes are from 40×40 μm^2 to 100×100 μm^2.

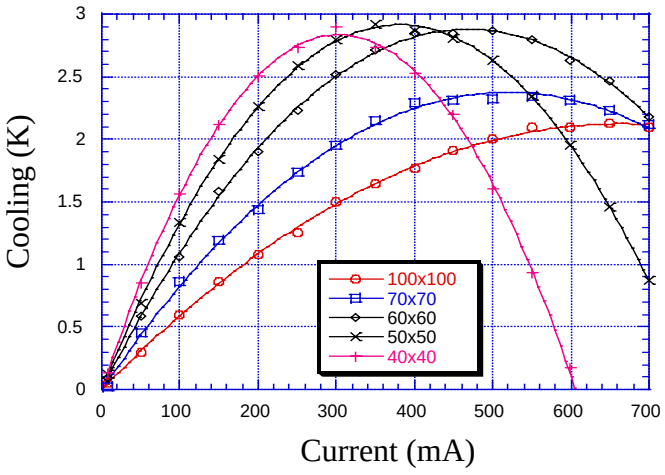
Figure 6.5 displays the measured cooling on top of the devices as a function of current for 2 μm $Si_{0.89}Ge_{0.10}C_{0.01}$/Si superlattice (HA99.089) microcoolers and 2 μm $Si_{0.89}Ge_{0.10}C_{0.01}$ alloy (sample HA99.091) microcoolers with the heat sink at 25 °C. The two samples are n-type and doped with Sb at 2×10^{19} cm^{-3}

and 6×10^{19} cm^{-3} respectively. 2.8 K cooling was obtained for the 40×40 μm^2 devices on both samples. 2.9 K cooling was measured for the 50×50 μm^2 SiGeC alloy microcoolers. It can be observed that the maximum cooling temperatures of the microcoolers are device size dependent. For the tested sizes (40×40 μm^2 to 100×100 μm^2), the smaller the device size, the higher maximum cooling for sample HA99.089 SiGeC/Si superlattice cooler; while the best device size for sample HA99.091 SiGeC alloy cooler was around 50×50 μm^2.

The size dependence of the maximum cooling in the microcoolers can't be explained with ideal thermoelectric or thermionic models which predict the maximum cooling is independent of the cooler size. As discussed in Chapter 5, this is due to the heat conduction from the side metal contact and the three-dimensional nature of current and heat spreading in the substrate. The silicon substrates of our samples are about 530 μm thick and its thermal resistance for the micro devices is about inversely proportional to the square root of the device area. On the other hand, the thermal resistance of the SiGeC or SiGeC/Si superlattice layer is inversely proportional to the device area. This different size dependence makes the effect of the non-ideal heat sink smaller for smaller size devices.



(a) $Si_{0.89}Ge_{0.10}C_{0.01}$/Si superlattice



(b) $Si_{0.89}Ge_{0.10}C_{0.01}$ alloy

Figure 6.5 Measured cooling for various SiGeC/Si microcooler sizes at 25 °C heat sink temperature. (a) Sample HA99.089: 2 μm 100 × (10 nm Si $Si_{0.89}Ge_{0.10}C_{0.01}$ / 10 nm Si) superlattice; (b) sample HA99.091: 2 μm $Si_{0.89}Ge_{0.10}C_{0.01}$ alloy. The cooler sizes are 40 × 40 μm^2, 50 × 50 μm^2, 60 × 60 μm^2, 70 × 70 μm^2, and 100 × 100 μm^2.

One possible way to reduce the substrate effects on the cooler performance is substrate thinning or removal. Figure 6.6 shows the measured cooling for 60 × 60 μm^2 SiGeC microcoolers (sample HA99.091) with various substrate thickness at 25 °C heat sink temperature.

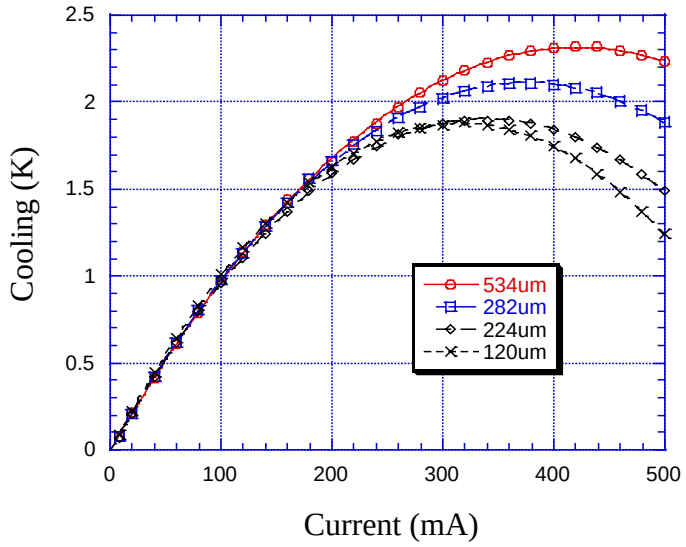


Figure 6.6 Measured cooling for 60 × 60 μm^2 SiGeC microcoolers (sample HA99.091) with various substrate thickness at 25 °C heat sink temperature. The thickness of the tested microcooler chips is 120 μm, 224 μm, 282 μm and 534 μm.

Contrary to what we had hoped, the measured maximum cooling decreased for thinner substrate. The reasons for this can be: silicon substrate is already a good heat sink itself especially with thermal spreading for small device sizes,

with substrate thinning, its thermal resistance reduction is very limited for substrate thickness larger than 100 μm [18, 19]; the removed silicon substrate part is replaced with thermal paste and copper heat sink in our microcooler testing, the thermal conductivity of copper (4.0 W/cmK) is just over 2 times that of silicon (1.5 W/cmK), but the thermal conductivity of thermal paste is about 1 order lower than that of silicon, plus the interface thermal resistance, the overall thermal resistance may not be reduced with reducing the substrate thickness.

For device comparison, Si microcoolers were fabricated on n^+ Si substrates with similar device structure and processing. The results of the 40×40 μm^2 Si devices are shown in Figure 6.7 along with those of the SiGeC/Si superlattice and SiGeC alloy coolers of the same size. Over three-fold improvement in maximum cooling is observed for SiGeC/Si superlattice and SiGeC alloy coolers over Si ones. This improvement mainly comes from the thermal conductivity reduction in SiGeC and SiGeC/Si superlattice with phonon alloy scattering and interface scattering. The measured thermal conductivity for $Si_{0.89}Ge_{0.10}C_{0.01}$ alloy and $Si_{0.89}Ge_{0.10}C_{0.01}$/Si superlattice are 6.0 W/mK and 8.4 W/mK respectively, which is over one order lower than that of Si (150 W/mK).

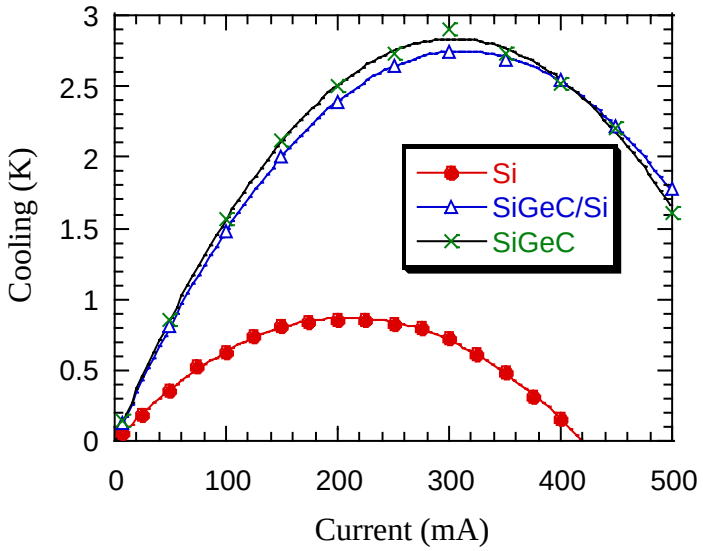


Figure 6.7 Measured cooling for 40×40 μm^2 μm^2 SiGeC (sample HA99.091), SiGeC/Si superlattice (sample HA99.089) and Si (sample HA99.097) coolers at 25 °C heat sink temperature.

SiGe is a good TE material for high temperature applications. [20, 21] The SiGeC/Si microcoolers also show better performance at higher temperatures. Figure 6.8 shows the measured cooling for 50×50 μm^2 SiGeC/Si microcoolers at various heat sink temperatures. The maximum cooling increases from 2.5 K at 25 °C to 6.9 K at 100 °C. Many high power microelectronic devices' operating temperature is 70 °C or higher due to insufficient heat sink. This improved cooling with increasing temperature in the microcoolers is beneficial to the thermal management of microelectronics working at elevated temperatures.

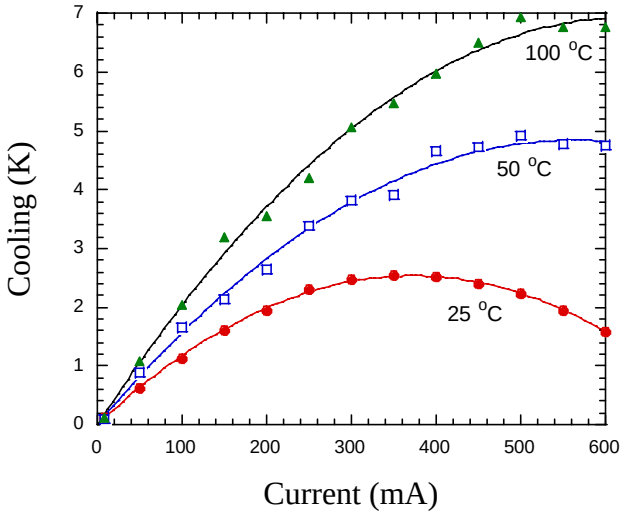


Figure 6.8 Measured cooling for 50 × 50 μm^2 SiGeC/Si superlattice coolers (sample HA99.089) at various heat sink temperatures.

6.4.2 Cooling power density

To send and control heat to the microcoolers, integrated thin film metal wire resistor structures were used for cooling power density measurement, as shown in Figure 5.25. The metal resistors are electrically isolated with the cooler layers by a SiN_x passivation layer. By measuring the resistance of the metal resistors, they can work as integrated temperature sensors for cooling temperature measurement; by sending electrical current into them, the metal resistors can work as integrated heaters for cooling power density measurement.

The cooling power densities of SiGeC/Si microcooler were characterized with integrated Au metal resistors.

The cooling power density measurement results on 40 × 40 μm^2 n-type SiGeC/Si superlattice microcooler (sample HA99.089) and SiGeC alloy microcooler (sample HA99.091) at 25 °C heat sink temperature are shown Figure 6.9 and 6.10 respectively. The heat load was controlled by the electrical in the integrated metal resistor. It can be seen that the cooling power decreases linearly with increasing the heat load and the cooler current of maximum cooling doesn't change with heat load. For a certain cooler current, the cooling temperature ΔT can be expressed as

$$\Delta T = \Delta T_0 - QR_{th\_total} \tag{6.2}$$

where ΔT_0 is the cooling temperature at zero heat load, Q is the heat load applied to the cooler from the integrated metal resistor and R_{th_total} is the overall thermal resistance of the cooler from the cold side to the hot side (heat sink). As shown in Figure 6.9 (b) and 6.10 (b), the maximum cooling power density can be obtained from the heat load axis junction (at zero cooling temperature) of the cooling temperature vs heat load density line. The measured maximum

cooling power density on the 40 × 40 μm^2 SiGeC/Si superlattice microcooler and SiGeC alloy microcooler are 540 W/cm^2 and 730 W/cm^2 respectively.

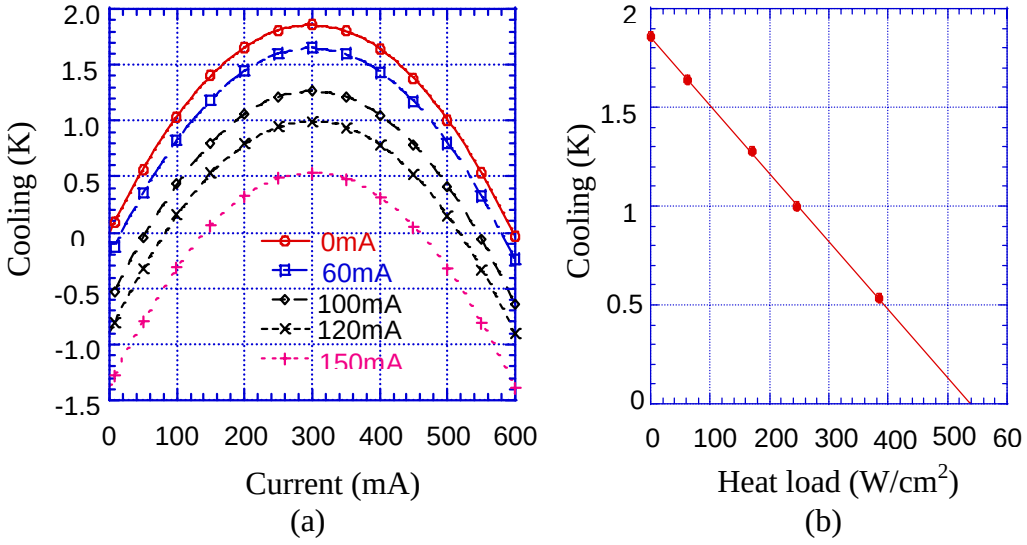


Figure 6.9 Cooling power density measurement results on 40 × 40 μm^2 n-type SiGeC/Si superlattice microcooler (sample HA99.089) at 25 °C heat sink temperature. (a) Cooling temperature vs. current at different integrated wire resistor currents, the resistance of the resistor is 0.273 Ω. (b) Maximum cooling vs. the heat load density.

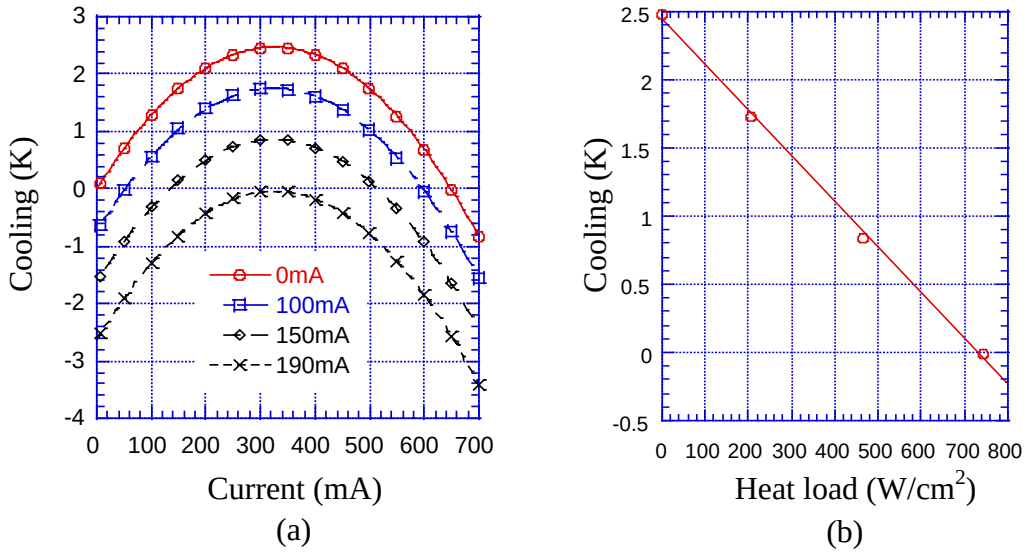


Figure 6.10 Cooling power density measurement results on 40 × 40 μm^2 n-type SiGeC alloy microcooler (sample HA99.091) at 25 °C heat sink temperature. (a) Cooling temperature vs. current at different integrated wire resistor currents, the resistance of the resistor is 0.33 Ω. (b) Maximum cooling vs. the heat load density.

The large cooling power density of SiGeC/Si microcoolers comes from their thin film structures. According to ideal TE cooler model in Chapter 2, the maximum cooling power density is inversely proportional to the TE leg thickness. For comparison, the cooling of a 40 × 40 μm^2 Bi_2Te_3 cooler with TE leg length of 1mm was calculated with the ideal TE cooler model and the result is shown in Figure 6.11 for various heat loads. It can be seen although Bi_2Te_3 bulk coolers can cool up to 70 K at 300 K heat sink temperature, there

maximum cooling power density is less than 20 W/cm^2 for TE leg thickness 1 mm and above. At larger heat loads larger than the maximum cooling power, the TE coolers actually work as heater, as can be seen in Figure 6.11. Therefore, bulk TE coolers are not suitable for cooling high power microelectronics. High cooling power density is one of the main advantages of our SiGeC/S and SiGe/Si microcoolers.

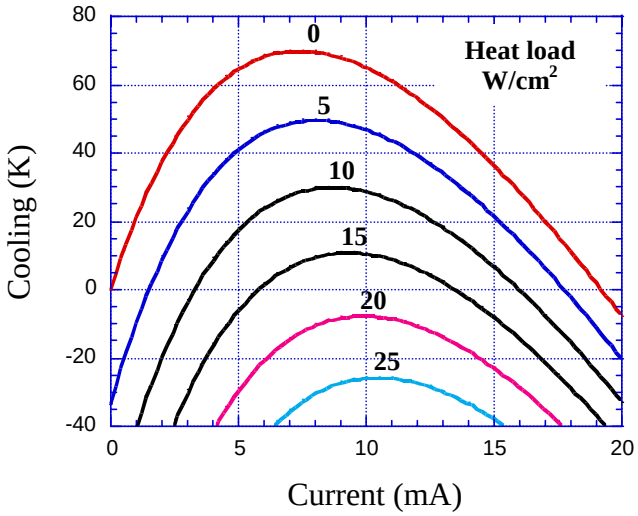


Figure 6.11 Calculated cooling for 40 × 40 μm^2 Bi_2Te_3 cooler with TE leg length of 1mm at 300 K heat sink temperature. The numbers in the graph are the heat load applied to the cooler. TE parameters used: Seebeck coefficient 200 μV/K, electrical resistivity 0.001 Ωcm and thermal conductivity 0.015 W/cmK.

Like SiGe/Si microcoolers, the maximum cooling power densities of SiGeC/Si microcoolers also have strong device size dependence as shown in Figure 6.12. The maximum cooling power density increases with decreasing the cooler size. One reason for this is that the substrate is closer to the ideal heat sink for smaller devices due to the heat spreading effects. With further device and material optimization, maximum cooling power density larger than 1000 W/cm^2 should be achievable.

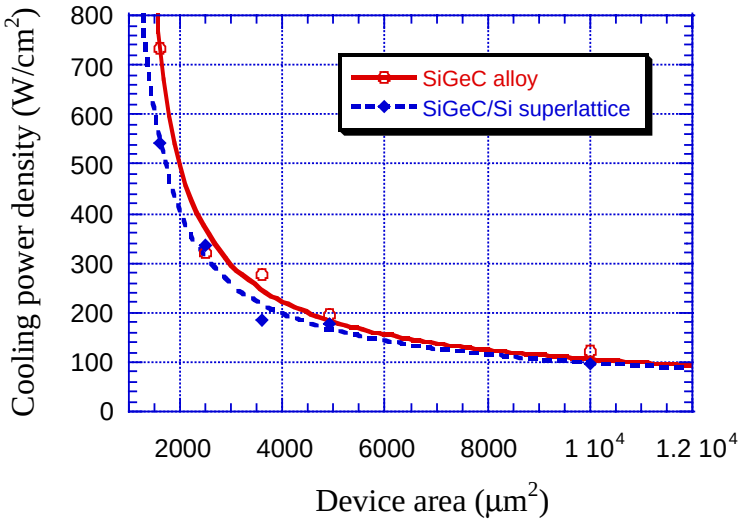


Figure 6.12 The measured maximum cooling power densities vs. cooler area for SiGeC (sample HA99.091) and SiGeC/Si superlattice (sample HA99.089) microcoolers at 25 °C heat sink temperature.

6.5 Application considerations for Si-based microcoolers

We have presented the fabrication and characterization of SiGeC/Si microcoolers in previous sections of this chapter and SiGe/Si microcoolers in Chapter 5. In this section, we will discuss some application considerations for Si-based microcoolers, including SiGeC/Si, SiGe/Si and other possible material systems such as Si/Ge superlattice etc.

First, as we have shown on SiGeC/Si and SiGe/Si microcoolers, one distinct advantage of Si-based microcoolers is their processing compatibility with silicon VLSI technology. This enables fabrication thousands of microcoolers on one silicon substrate at the same time with low cost per microcooler. More important, it is possible to monolithically integrate the microcoolers with other silicon based microelectronic or optoelectronic devices. This device integration has two aspects: one is to integrate the microcoolers with thermal sensitive devices, which can greatly reduce thermal contact resistance and reduce the packaging cost; the other is to integrated the microcoolers with its control circuits and other devices on the same chip. Lattice matched SiGeC/Si materials can make this integration easier by solving the lattice mismatch issues in SiGe/Si or Ge/Si material systems. To monolithically integrate the microcoolers with the devices to be cooled, the

cooler surface can't be covered with all of metal contacts and some space is needed for the devices to be cooled. To test the feasibility of surrounding cooling, we made microcoolers with metal contacts only covering part of cooler mesa surfaces. Figure 6.13 shows the measured cooling on a SiGe/Si superlattice cooler (sample HA00.085) with a ring shape metal contact on the cooler mesa. The mesa size is 150×80 μm^2, and it is covered with cooler top metal contacts except a 60×60 μm^2 region in the middle of the mesa. Maximum cooling of 3.6 K and 2.5 K were measured on the metal contact and off the metal contact at the mesa respectively at 25 °C cooling temperature. Large integrated cooling is possible if larger cooling can be obtained on individual microcoolers.

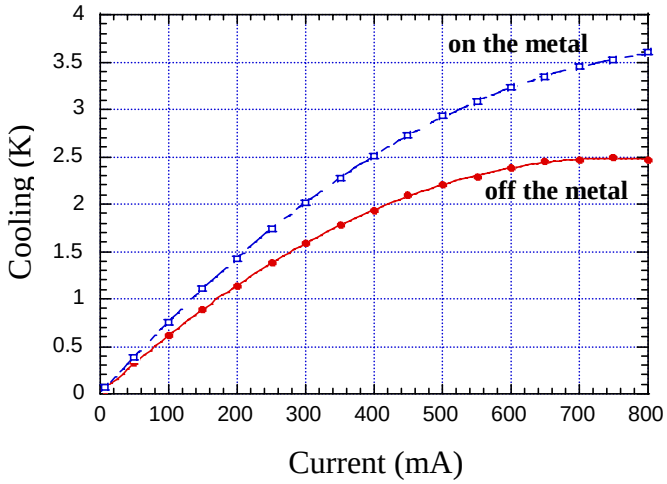
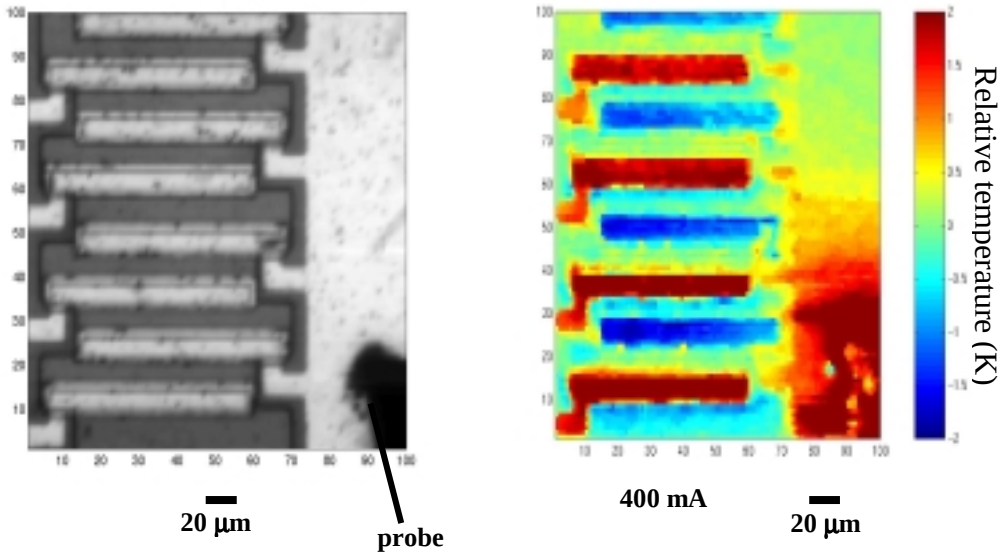


Figure 6.13 Measured cooling on p-type SiGe/Si microcooler (sample HA00.085) with ring shape top metal contact at 25 °C heat sink temperature. The mesa size is 150×80 μm^2, and it is covered with cooler top metal contacts except a 60×60 μm^2 region in the middle of the mesa. Cooling was measured with micro thermocouple for both on the metal position and off the metal position on the mesa.

Second, Si-based thermoelectric or thermionic (TI) microcoolers are solid state, robust and compatible with other cooling techniques. Their device structures are simple and still keep the silicon chip format. Almost all other cooling technologies for microelectronics, such as air-cooling, liquid cooling and diamond substrates etc, can be combined with the microcooler cooling. Even the recent other silicon integrated cooling methods, such as microchannel cooling, can also work with the TE and TI microcoolers [22-24]. This cooling

method compatibility is important in that the microcoolers need good heat sink and the heat sink is usually supported by other cooling methods.

Third, integrated Si-based microcooler can be used for localized temperature control. In this way, microcoolers can selectively cool thermal sensitive key devices instead of the whole chip, thus can have a better overall cooling efficiency. If the current direction is reversed from the its cooling condition, the TE or TI microcooler will work as a microheater, in which there will be TE or TI heating in addition to joule heating. This can provide wider latitude in temperature control. With the integrated microcooler, it is possible to have multi-place temperature controls on a single chip. Figure 6.14 shows the measured thermal image of a p-type $Si_{0.8}Ge_{0.2}$ (sample HA00.034) microcooler/microheater cross-finger structure. Localized cooling and heating is demonstrated at a spacing of 20 μm. Here the cooler and heater were controlled with the same current. It is also possible to control them individually.



(a) optical image (b) thermoreflectance image

Figure 6.14 Localized temperature control on p-type $Si_{0.8}Ge_{0.2}$ (sample HA00.034) with cross-finger microcooler/microheater. The current goes from the right contact pad to the right contact pad. (a) optical image (b) thermoreflectance image at a total current of 400 mA. Measured by J. Christofferson.

It can be noted that the current for the SiGe/Si and SiGeC/Si microcooler is in the order of hundreds of mA for devices as small as 50×50 μm^2. Although it is smaller than conventional bulk coolers whose current can be in the order of amperes, it can be a very large current for microelectronics. The reason for the large current in microcoolers is that the current density for maximum cooling temperature is inversely proportional to the TE leg thickness under the ideal TE

cooler model. Using n- and p-type microcooler array structure electrically in series and thermally in parallel is one way to achieve large cooling capacities with relatively small currents. The cooler array structure can also improve the cooler performance by eliminating the heat conduction to cold side of the cooler from the wire connections to the cooler top contacts.

The most important application consideration of Si-based microcoolers is cost and performance. The use of SiGe, SiGeC etc will increase material growth cost. In our work, the materials were mainly grown by MBE. Other lower cost growth method, such as liquid phase epitaxy (LPE) and chemical vapor deposition (CVD) may also be used. Some of the graded SiGe buffer layers of our SiGe/Si microcoolers samples, such as HA00.055, were grown by CVD and comparable cooler performance was measured with MBE grown buffer layers [25]. Integration between microelectronics and microcooler may increase the processing cost, but it can reduce the packaging cost. For practical applications of the microcoolers, a minimum cooling of 10 K is required to justify the additional costs. At room temperature, cooling up to 4.3 K and 2.9 K was measured on SiGe and SiGeC microcoolers respectively. However, they are still too small for practical applications. Further device and material optimizations are necessary. Based on the room temperature TE properties of bulk SiGe, the maximum cooling is about 10 K considering the unavoidable

non-ideal effects for microcoolers, such as contact resistance. To get larger cooling, breakthroughs in superlattice materials to have larger ZT are needed.

6.6 Summary

SiGe has a larger lattice constant than that of Si, and buffer layers are needed for integrated SiGe/Si microcoolers. This increases the material growth cost and the complexity of integration with other microelectronic devices. By adding small atom C into SiGe, the strain can be adjusted and lattice matched SiGeC/Si structures can be obtained with proper selection of Ge and C ratio. Lattice matched $Si_{0.89}Ge_{0.10}C_{0.01}$/Si superlattice and $Si_{0.89}Ge_{0.10}C_{0.01}$ alloy samples were grown directly on Si by MBE without buffer layers.

SiGeC/Si superlattice and SiGeC alloy microcoolers were fabricated with IC processing. Cooling by as much as 2.8 K and 6.9 K was measured with micro thermocouples on the SiGeC/Si superlattice microcooler at heat sink temperatures of 25 °C and 6.9 °C respectively. Cooling by up to 2.9 K and cooling power density of 730 W/cm^2 were measured on SiGeC microcoolers at 25 °C heat sink temperature.

Some application considerations for Si-based microcoolers, including SiGe/Si and SiGeC/Si microcoolers, are discussed. Si-based microcoolers are attractive for compatibility with VLSI processing and with other cooling techniques, localized temperature control, high cooling power density, etc. However, current cooling is not high enough for practical applications. Further device and material optimization is needed. Although the microcooler performance of superlattice materials is comparable with or less than that of alloy materials, superlattices can have more potential in using latest developments in ZT improvements, such as thermionic emission, carrier pocket engineering and phonon engineering.

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Chapter 7

Summary and future work

7.1 Summary

With the development of VLSI and ULSI technology, device power density increased, which puts higher requirements on the thermal management. Thermal management has become one of the barriers to further increase the clock speed and device performance of integrated circuits (ICs). Conventional Bi_2Te_3-based thermoelectric (TE) coolers have been used widely for optoelectronic device cooling. However, they are limited by efficiency and power density, and their processing is not compatible with IC processing. Silicon microcooler is an attractive approach for monolithically integrated cooling for silicon devices.

Chapter 1 gave the motivation and an overview of current research on solid-state active cooling, including thermoelectric cooling and thermionic cooling. Various ways to enhance the TE figure of merit were discussed. Current research on silicon microcoolers was overviewed. Chapter 2 introduced the basic thermoelectric and thermionic theory for cooling. They are

the fundamental operation theory of the coolers in this thesis. The thermoelectric figure of merit is the key material parameter for the cooler performance. The cooling power density is inversely proportional to the thickness of the TE leg. Thin film microcoolers are advantageous for both high cooling power density and their potential for integrated cooling. Thin film microcoolers can also increase the overall cooling efficiency by selectively cooling the key devices instead of the whole chip. The design of thin film microcoolers is different from bulk coolers in both device processing and non-ideal effects. The design of microcoolers was presented in Chapter 3. With reducing the TE leg thickness, the thermal and electrical resistance of the TE leg becomes very small and the non-ideal effects, such as contact resistance, heat sink thermal resistance, packaging thermal resistance, can't be ignored anymore.

Fundamentally, the microcooler cooling performance is determined by the TE material's figure of merit which is related to three TE properties: Seebeck coefficient, electrical conductivity and thermal conductivity. The TE property characterization of SiGe, SiGe/Si superlattice, SiGeC and SiGeC/Si superlattice were described in Chapter 4. Cross-plane thermal conductivity of SiGe/Si superlattices with different periods was measured with 3ω method. The thermal conductivity of superlattice is smaller than that of the average of

that of the silicon and SiGe layers, showing the phonon scattering effects at the superlattice interfaces. However, the thermal conductivity reduction in SiGe/Si superlattices is less than that reported in Si/Ge superlattice systems, which is related to the smaller phonon impedance mismatch in SiG/Si systems. [1]

SiGe is a good thermoelectric material for high temperature applications. At room temperature, its maximum cooling can be over 10 K under ideal conditions. Although this it is much less than that of Bi_2Te_3-based TE coolers, it is attractive for its process compatibility with silicon IC technology. The experimental work on SiGe/Si microcooler is presented in Chapter 5. SiGe and SiGe/Si superlattices were grown on silicon substrates with MBE. SiGe alloy and SiGe/Si superlattice microcooler with size from 10×10 μm^2 to 150×150 μm^2 were fabricated with standard silicon IC processing. Various microcooler characterization methods were developed and used to measure the cooling temperature and cooling power density. For quick and direct measurement of cooling temperature, micro thermocouples were used. For 25 μm diameter thermocouples, the minimum measurable cooler size is about 40×40 μm^2. To measure smaller device sizes, smaller thermocouple sizes are needed. To measure the temperature distribution of the microcooler, thermal reflectance method was used for thermal image measurement of the microcoolers. Cooling up to 4.3 K and 13.8 K was measure on $Si_{0.8}Ge_{0.2}$ microcoolers at heat sink

temperature 25 °C and 250 °C respectively. The better cooling at higher temperatures is related to the higher ZT of SiGe alloys. Unlike bulk TE coolers, the maximum cooling temperatures of the microcooler show size dependence. This is because of the non-ideal effects. Due to the heat spreading in the substrates for the microcoolers, the thermal resistance ratio between the heat sink and the TE leg decreases with decreasing the cooler size, which makes smaller devices cool better. As the first stage for demo of the Si-based microcoolers, the microcoolers used single element TE cooler structure, in which the heat conduction from the connecting metal wires to the cold side of the coolers is unavoidable. This will reduce the maximum cooling. For the device structure we used, the thermal resistance of the connection wire is proportional to the square root of cooler area while the thermal resistance of the TE leg is proportional to the area of the microcooler. This different size dependence makes better cooling for larger devices. Combined the effects from non-ideal heat sink and the heat conduction from the connecting wires, optimal device sizes were observed for maximum cooling.

One advantage of thin film microcoolers is their high cooling power density. To measure cooling power, integrated metal resistors were made on top of the microcooler working as both temperature sensor and microheater to

apply heat load to the microcooler. Cooling power density of 598 W/cm^2 were measured on 40×40 μm^2 microcoolers.

The lattice constant of SiGe is larger than that of silicon substrate and buffer layers are needed before the growth of thick SiGe or SiGe/Si superlattices to avoid strain induced dislocations. The buffer layers increase the material growth cost and the complexity of device integration. To solve this problem, small atom C was added to the SiGe. With proper selection of the ratio between C and Ge, the lattice constant of SiGeC can be adjusted to match that of Si. Lattice matched SiGeC/Si superlattice and SiGeC alloy were grown directly on silicon substrate with MBE by Edward Croke in HRL Laboratory. The fabrication and characterization of SiGeC/Si microcoolers were described in Chapter 6. Cooling up to 2.9 K and 6.9 K were measured at heat sink temperature 25 °C and 100 °C respectively. Cooling power density up to 700 W/cm^2 were measured at room temperature.

7.2. Future work

The research on integrated silicon microcoolers is still in its early stage. There is a lot of room to further improve the devices.

7.2.1 Further Materials optimization

Fundamentally, the maximum cooling temperature is determined by the material's thermoelectric figure of merit. Material optimization is a key for good microcooler performance. SiGe/Si and SiGeC/Si microcoolers were studied in Chapters 5 and 6, other material systems, such as Ge/Si, SiGeC/SiGe and SiGe/SiGe, are also worth a try. Ge/Si superlattices can have high band offsets and low thermal conductivity due to large phonon impedance mismatch [1]. SiGeC/SiGe superlattice can be adjusted to have its average lattice constant match to that of Si and keep a low average thermal conductivity. Material optimization includes composition, doping, superlattice periods, thickness, etc. Due to materials growth limitations, the SiGe/Si and SiGeC/Si superlattices used in Chapters 5 and 6 are uniformly doped. Modulation doping would give more freedom in band structure engineering to take advantage of thermionic cooling. In addition to the mono-crystalline materials, doped amorphous silicon and poly silicon can also be used for silicon microcoolers.

To characterize the figure of merit, Seebeck coefficient, electrical conductivity and thermal conductivity need to be measured. For thin film materials like superlattice, thermoelectric properties can be difference for in-plane direction and cross-plane direction. In Chapter 4, the measurement of

thermal conductivity in the cross-plane direction and Seebeck coefficient and electrical conductivity of in-plane direction are described for SiGe/Si and SiGeC/Si superlattices. Complete measurements for the thermoelectric properties in both in-plane and cross-plane direction are needed. Recent experimental results on BiTe/BiSb superlattice showed that superlattices can have higher figure of merit than its corresponding alloy materials [2].

7.2.2 N- and p-type cooler array

The microcooler structures in our experimental work are single element microcoolers, either in n-type or p-type materials. In this kind of cooler structure, the heat conduction and Joule heating from the connection wire to the cool side of the cooler are unavoidable and large current is often needed. The way to solve this problem is to use n- and p-type cooler array, electrically in series and thermally in parallel. Microcooler arrays are difficult to assemble in the same way as conventional bulk TE coolers. Monolithically integrated microcooler array is a better choice. One possible device structure was shown in Figure 5.36 of Chapter 5.

7.2.3. In-plane transport devices

The microcooler structures in this thesis used cross-place transport and their advantages include high cooling power density and robust. Due to its low aspect ratio, contact resistance is one of the barriers to improve device performance and the current or current density is generally large. Using in-plane transport cooler structure, high cooler aspect ratio can be easily achieved. With the in-plane transport cooler structure, the contact resistance can have less serous impact on device performance than that of in-plane transport cooler structure and operation current can be very small. To thermally isolate the cold side of the cooler from the heat sink, substrate removal is usually required. With deep silicon reactive ion etch, the substrate can be selectively etched off. In-plane transport microcoolers can be expected to have better cooling temperature and smaller cooling power compared with cross-plane transport microcooler. Besides cooling applications, they can also be used as thermal sensors or power generators.

7.2.4 Monolithic integration

The ideal way to use the microcoolers is to monolithically integrate them with other microelectronic or optoelectronic devices. This integration has two folds. First, integrate the microcoolers with temperature sensitive devices to

improve device performance and reliability. Secondly, integrate the microcoolers with its control circuits etc. Silicon-based microcoolers are advantageous for its processing compatibility with silicon integrated circuit (IC) technology. Monolithic integration of InGaAs/InP microcoolers with semiconductor lasers has been reported [3]. SiGe/Si has better thermoelectric performance than InGaAs/InP system. With further materials and microcooler structure optimization, monolithic integration of Si-based microcoolers with silicon integrated circuits should be feasible.

7.3 Conclusions

Integrated silicon microcoolers are a new research area and rapid progress has been made in UCSB in the past three years. Both n- and p-type SiGe/Si microcoolers with epitaxial layers on the order of several microns were demonstrated with silicon IC processing technology, which paved the road to make n- and p-type cooler arrays. Micro thermocouples, thermal reflectance method and integrated thin film metal resistors were used to characterize the microcoolers. Cooling up to 4.3 and 13.8 K were measured at heat sink temperatures of 25 °C and 250 °C respectively. Microcooler response time in

the order of 15~30 μs and maximum cooling power density in the order of hundreds of W/cm^2 were measured, which are over four orders faster [2] and over one order larger than those of conventional bulk coolers. To facilitate material growth and device integration, lattice matched SiGeC/Si microcoolers were demonstrated with a measured cooling power density up to 700 W/cm^2 at room temperature. Silicon-based microcoolers are an attractive way for integrated spot cooling. However, their current maximum cooling temperature is still too small for commercial applications at room temperature. Further material optimization to increase its TE figure of merit and further device optimization to reduce non-ideal effects for the microcoolers are needed.

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