UNIVERSITY OF CALIFORNIA
Santa Barbara

Ultra-Wideband WDM VCSEL Arrays by Lateral Heterogeneous Integration

A Dissertation submitted in partial satisfaction of the
requirements for the degree Doctor of Philosophy
in Electrical and Computer Engineering

by

Jon Geske

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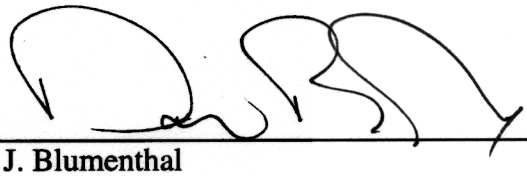
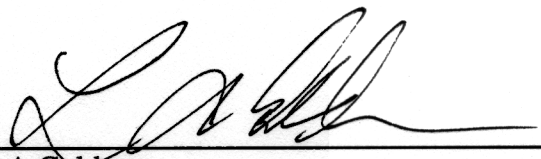
June 2004

The dissertation of Jon Geske is approved.



Daniel J. Blumenthal



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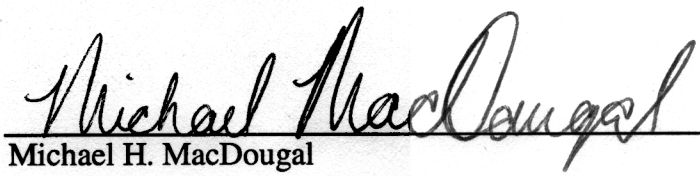

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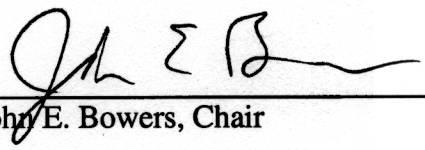

John E. Bowers, Chair

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This dissertation is dedicated

to my wife,

Hani

Acknowledgements

In 1999, floating on the telecom bubble was an exciting place to be. It wasn't easy for me to decide to leave a VCSEL job I loved with people whom I had learned so much from. My future wife, Hani, really helped me put it all in perspective of my long-term ambitions. Without her support then, and over the years, this dissertation would never have happened. She has shown understanding and patience these last five years of school and first five years of our marriage. My parents and family have always been supportive of me and the decision I made to leave my home in Minnesota nearly 12 years ago to begin a life in California. They taught me to place my faith in God and trust Him for the future.

Looking back, there have been numerous individuals who have been responsible for my decision to pursue a Ph.D. Professor Dan Dapkus and Michael MacDougal introduced me to the field and were an inspiration when I didn't always feel up to the challenge. Vijay Jayaraman and Frank Peters were instrumental in my decision to attend UCSB' a decision I am glad I made. Vijay's technical input over the years has played a key role in developing the work of this thesis and I am much indebted to him.

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Curriculum Vitæ

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Abstract

Ultra-Wideband WDM VCSEL Arrays by Lateral Heterogeneous Integration

by

Jon Geske

Advancements in heterogeneous integration are a driving factor in the development of evermore sophisticated and functional electronic and photonic devices. Such advancements will merge the optical and electronic capabilities of different material systems onto a common integrated device platform.

This thesis presents a new lateral heterogeneous integration technology called nonplanar wafer bonding. The technique is capable of integrating multiple dissimilar semiconductor device structures on the surface of a substrate in a single wafer bond step, leaving different integrated device structures adjacent to each other on the wafer surface. Material characterization and numerical simulations confirm that the material quality is not compromised during the process.

Nonplanar wafer bonding is used to fabricate ultra-wideband wavelength division multiplexed (WDM) vertical-cavity surface-emitting laser (VCSEL) arrays. The optically-pumped VCSEL arrays span 140 nm from 1470 to 1610 nm, a record wavelength span for devices operating in this wavelength range.

The array uses eight wavelength channels to span the 140 nm with all channels separated by precisely 20 nm. All channels in the array operate single mode to at least 65 °C with output power uniformity of +/- 1 dB. The ultra-wideband WDM VCSEL arrays are a significant first step toward the development of a single-chip source for optical networks based on coarse WDM (CWDM), a low-cost alternative to traditional dense WDM.

The CWDM VCSEL arrays make use of fully-oxidized distributed Bragg reflectors (DBRs) to provide the wideband reflectivity required for optical feedback and lasing across 140 nm. In addition, a novel optically-pumped active region design is presented. It is demonstrated, with an analytical model and experimental results, that the new active-region design significantly improves the carrier uniformity in the quantum wells and results in a 50% lasing threshold reduction and a 20 °C improvement in the peak operating temperature of the devices.

This thesis investigates the integration and fabrication technologies required to fabricate ultra-wideband WDM VCSEL arrays. The complete device design and fabrication process is presented along with actual device results from completed CWDM VCSEL arrays. Future recommendations for improvements are presented, along with a roadmap toward a final electrically-pumped single-chip source for CWDM applications.

Contents

Chapter 1

Introduction

The need for increased functionality in optoelectronic devices has fueled extensive research into advanced integration techniques. By developing techniques that allow for the integration of dissimilar device structures, a multitude of optical and electronic capabilities can be combined into a single chip and entirely new types of systems can be built. Integration promises to lead to increased functionality while simultaneously reducing chip power consumption, size, and cost. In the area of optical transmitters, advanced integration is required to achieve high performance laser arrays covering wavelength spans beyond what can be achieved with traditional epitaxial structures.

In this thesis work, a novel advanced integration technique was developed. The technique is the first of its kind and is capable of integrating

multiple dissimilar epitaxial device structures laterally adjacent to each other on the surface of a wafer. Using this technique, multi-wavelength vertical-cavity surface-emitting laser (VCSEL) arrays spanning a record wide wavelength span of 140 nm were successfully fabricated. Such lasers have profound practical applications in low-cost optical communications networks. To achieve these results further advances in VCSEL active region and mirror design were required. This thesis will present and discuss these technological innovations and advancements.

1.1 The Need For Integration

Advancements in the development of optoelectronics will be driven by advancements in device integration techniques. The common analogies between the present levels of integration in optoelectronics and the transistor based small-scale integrated circuits of the 1960's fail to capture the complexity of true optoelectronic integration. The challenge of optoelectronic integration greatly surpasses that of pure electronic device integration. As structure matches function in the natural world so it goes in the optoelectronic IC world. The large contrast between the material and design differences in electronic and photonic devices, and between photonic devices with different functions, leads to difficulties in achieving high levels of integration in these circuits. Interconnection complications exist; mixed signal electronic components must

be electrically interconnected with the optical components which are themselves optically interconnected. The existing interconnect technologies are not enough to route and deliver these electronic and photonic signals.

While the challenge in optoelectronic integration is great, the reward for success is astounding. The potential application limits for components and systems with complex electronic and photonic functionalities are nearly limitless. Beyond enhanced functionality, integration is instrumental to reducing system costs through reduced package counts, reduced package Input/Output (I/O) sizes, and reduced power consumption related to inter-chip I/O. The benefits of enhanced integration do not belong only to future advanced components. The need for enhanced integration technology is immediate and exists in at least three areas: extension of electronic IC capabilities by the addition of a photonic layer, extension of photonic IC capabilities by the addition of electronic device capabilities, and enhanced device integration in photonic ICs.

As an extension of the natural progression in electronic IC development, photonics offer a solution to key technical challenges. The integration of a photonic signal layer on tomorrows larger, more advanced electronic ICs will provide an effective means for intra-chip signal and clock routing. Photonic layer intra-chip transport of these signals will solve noise, timing, and power issues complicating the advancement of ever faster and larger ICs. Inter-chip

input and output routing is another issue plaguing the IC industry. I/O functions consume large amounts of silicon real estate and power resources, while requiring massive parallel buses to maintain the desired I/O data rates. High speed serial and parallel photonic transport between chips will operate at lower powers and ultimately consume less space.

Integration of photonic and electronic components can further the development of traditional photonic components. Lasers, modulators, and detectors integrated with drive and control electronics, biasing circuits and amplifier circuits will consume less space, enable higher speed operation, and ultimately cost less to build and deploy. By combining all required electronic functions into a single chip, this optoelectronic technology will be ready to meet application requirements deeper inside systems and enhance the photonic role from a simple box to box interconnect method to an intra-chip interconnect technology.

The modern photonic integrated circuit (PIC) consists of a few select components integrated on a common chip and interconnected by semiconductor waveguide structures. These components include devices such as semiconductor optical amplifiers, Lasers, modulators (electro absorption modulators and Mach-Zehnder), and detectors. Through careful design and compromise, epitaxial structures can be designed that meet the basic needs of multiple components of the integrated structure and a variety of integration

techniques have been developed to modify wafer sections to allow for improved designs and performance. PIC functionality and capabilities can benefit from enhanced integration techniques that would allow for the arbitrary integration of differing device structures exactly designed for their specific function. Additional optical processing capabilities in differing materials and structures could be added as well as out of plane signal routing and integration with on-chip electronic processing capabilities. Enhanced integration capabilities will allow for the combination of the most recent advancements in photonic crystals, and other novel optical components, with more established PIC components. These integration techniques will allow for the integration of electronic control and monitoring layers that will greatly enhance the capability of even so-called all-optical PICs. Through integration, novel and still unimagined PIC capabilities can be realized.

1.2 Integration Approaches

Research into integration techniques has developed a variety of approaches and forms. These approaches vary from the wafer-scale integration of epitaxial materials to flip-chip die attach techniques. These approaches can be classified in a variety of ways with some approaches satisfying multiple criteria. Integration techniques can allow for vertical or lateral integration, meaning that the devices or materials being combined can differ in the direction normal or

parallel to the plane of the wafer. Lateral integration techniques can allow for completely different material structures to be integrated, or allow for only structures that are substantially similar to be integrated. Integration techniques can be wafer scale, or done on a piecewise basis. Finally, some integration techniques allow for the materials and structures integrated together to be internal to a single device such that the integrated components, once combined together, form a completed device. This type of integration will be referred to as device-intrinsic integration as opposed to device-extrinsic integration where the materials and structures are integrated together in such a way that they are not combined together to form a device. Common integration techniques will be presented and classified based on these criteria.

Many integration techniques that combine materials and device structures can be broadly classified as vertical integration or lateral integration, or in some cases an integration technique can be classified as both. Here, vertical integration (Figure 1.1) refers to combining materials in a direction normal to the surface of the host wafer in a manner other than traditional epitaxial growth. Flip-chip bonding is such an approach (Figure 1.2), as is wafer bonding (Figure 1.3) and heteroepitaxy techniques such as pseudo-morphic growth. Lateral integration refers to the combination of differing devices or material structures such that they are laterally adjacent to each other on the wafer surface (Figure 1.4). Many lateral integration techniques accomplish

lateral integration through repeated application of a process step. This is the case with flip-chip bonding. Epitaxial regrowth is a lateral integration technique that integrates two regions of differing material structures adjacent to each other on the wafer surface (Figure 1.5). Each time the wafer is regrown in an etched area, another device structure is laterally integrated. Lateral integration can be accomplished through Selective Area Growth (SAG) [1, 2], with different epitaxial structure thicknesses deposited in each region of a different width (Figure 1.6). Repeated application of localized selective area wafer bonding can also be used to achieve lateral integration [3] (Figure 1.7). Recent advances in quantum-well intermixing have demonstrated the technique's capability to accomplish lateral device region integration by shifting the quantum-well band gap of the material in a well-controlled way [4] (Figure 1.8).

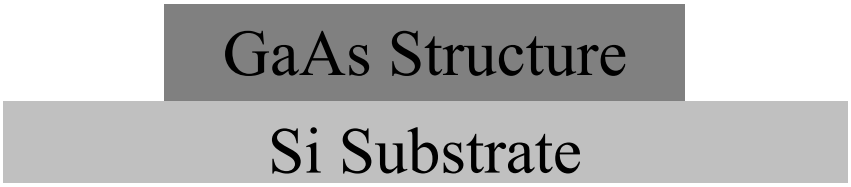

Figure 1.1. Vertical integration

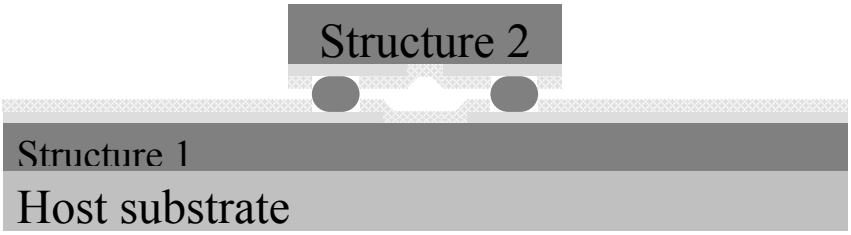

Figure 1.2. Flip-chip bonding

Figure 1.3. Planar wafer bonding

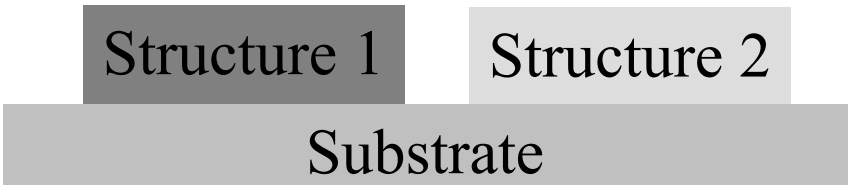

Figure 1.4. Lateral integration

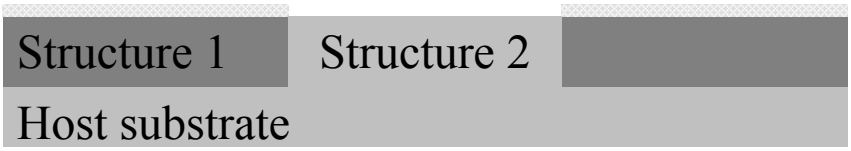

Figure 1.5. Epitaxial regrowth

Figure 1.6. Selective area growth (SAG)

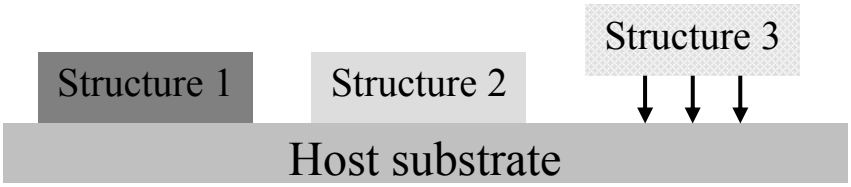

Figure 1.7. Selective area bonding

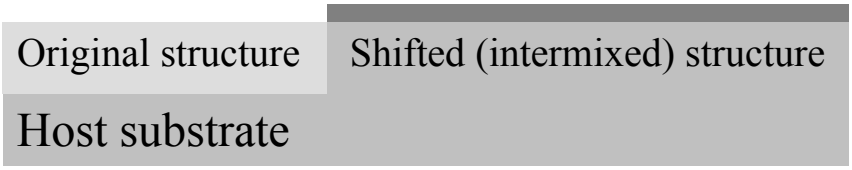

Figure 1.8. Quantum-well intermixing

A second key differentiation between different lateral integration techniques is the amount of device variation the technique can accommodate. Integration techniques can allow for completely different material structures to

be integrated, or allow for only structures that are substantially similar to be integrated. Techniques such as flip-chip, epitaxial regrowth and selective area bonding allow for the lateral integration of completely different material structures and compositions. These techniques are not limited to the types of devices that can be laterally integrated, as long as they can be grown on the same host substrate or attached by flip-chip or bonding. Single-step SAG and quantum-well intermixing alone do not allow for the integration of arbitrary structures. These techniques integrate structures that are substantially similar except for modified layer thicknesses in the case of SAG and modified band gaps in the case of quantum-well intermixing.

Some integration techniques are not well suited for wafer scale application. Flip-chip bonding and selective area bonding are typically done on a die-by-die basis or a region-by-region basis. Wafer bonding, epitaxial regrowth, SAG, and quantum-well intermixing can all be applied as a wafer scale process.

Most of the integration techniques reviewed here allow for the materials and structures integrated together to be intrinsic to a single device. The exception is the flip-chip bonding technique. In flip-chip bonding, the integration interface – the solder bumps shown in Figure 1.2 – is external to any device and hence only complete devices or groups of devices can be integrated in such a fashion. This is typically the case with other hybrid integration

techniques that have been developed for the electronics industry. The device intrinsic techniques, such as regrowth, allow the two integration regions to form different portions of the same device and thus allow for more complex devices to be fabricated.

All these integration techniques play a useful role in the development of high performance and high functionality optoelectronic chips. Unfortunately, no single technique meets all the needs of all applications. One specific combination of qualities is not satisfied by any of these techniques. A device intrinsic, wafer-scale integration technique capable of simultaneous vertical integration and lateral integration of arbitrarily varying structures is not embodied by any of the before mentioned techniques. The combination of heteroepitaxy and epitaxial regrowth would have these qualities but the combined complexity of the two techniques does not bode well for the success of this approach. In this thesis work, a novel approach with the desired capabilities was developed and will be presented in detail in Chapter 2.

1.3 Coarse Wavelength Division Multiplexing

The research conducted for this thesis project was focused on the development of fundamental integration capabilities as well as meeting objectives for a specific relevant application in fiber optic communications. The specific application area was Coarse Wavelength Division Multiplexing or CWDM.

CWDM is the same as traditional Dense Wavelength Division Multiplexing (DWDM – though often just referred to as WDM) except it uses a wider wavelength spacing between data channels and hence allows for un-cooled operation of system components.

The concept behind WDM is to take full advantage of the properties of the fiber optic transport media. WDM is really just frequency division multiplexing, such as that used in radio frequency systems, applied to the fiber optic transport media at much shorter wavelengths. Photons, as Bosons, do not interact with each other directly, but can only interact with each other through a third medium, such as the transport media in which they travel. At moderate powers levels and to a first order approximation, photons within a fiber optic cable do not interact with each other (there a numerous exceptions to this statement and much research and many Ph.D.s are based on these exceptions). In addition, the glass from which most fiber optic cables are formed can efficiently transport light covering a wavelength span over 500 nm (1200 nm to 1700 nm). With these properties, it is possible to build fiber based communications systems capable of carrying hundreds or even thousands of different data channels, all separated from each other by a fraction of a nanometer in wavelength (GHz frequency spacing).

DWDM systems use frequency separations as small as 25 GHz (about 0.2 nm). With such small frequency separations between channels, precise

filters are used to combine and select each of the frequency differentiated data channels. It is also necessary for the wavelength of the laser source generating the signal to be precisely controlled. The precision required for DWDM applications makes these high performance systems expensive to design and build.

The expense associated with DWDM systems is prohibitive in applications where hundreds of data channels are not needed. In these applications a lower cost approach is needed. CWDM is such an approach. The modern CWDM system is based on the International Telecommunication Union's ITU-T G.694.2 CWDM Grid Specification (the most recent active revision was December 2003 at the time of this publication). This document defines a course wavelength grid from 1271 nm to 1611 nm with 20-nm channel spacing. It also allows for a +/- 6-7 nm source wavelength variation and filter guard bands of 6-7 nm. With these liberal tolerances, it is possible to use less expensive filter and laser source components. With CWDM, it is possible to fabricate lasers that will emit in the proper wavelength window and these lasers do not need to be packaged with expensive temperature stabilizing thermal electric coolers.

Because CWDM uses such coarse wavelength spacing, the same components can be used in many network architectures supporting many different types of services and data rates. Some specific application areas for

CWDM include metropolitan networks and access networks connecting users to a variety of services. These application areas are growing rapidly and low-cost alternatives like CWDM are needed to make their deployment affordable. A recent ITU report (ITU, June 2002) predicts that CWDM is positioned to capture substantial portion of predicted $4.5 billion 2005 market for optical metropolitan networks. The applicability of CWDM devices to multiple topologies promises to allow for additional volume-based cost reductions.

In low-cost applications, data is typically encoded onto the optical carrier by direct modulation of the source laser because higher costs are associated with externally modulating the laser light. Because the wide wavelength span of CWDM networks typically precludes the use of all optical amplification techniques such as erbium doped fiber amplifiers, transmission lengths typically do not cover lengths greater than 80 km. Thus signal strength is a primary limiting factor in many of these systems, and the degradation in signal quality resulting from the use of direct modulation is not as serious an issue as in long distance DWDM networks.

The Vertical-Cavity Surface-Emitting Laser (VCSEL) is an excellent source candidate for use in CWDM network applications. VCSELs offer advantages in low-cost manufacturing and packaging made possible by wafer-scale fabrication and testability, low-power dissipation, low-divergence circular-output beams, and the relative ease of fabricating one and two-dimensional

VCSEL arrays. The low power dissipation of these devices and the ability to directly modulate them also position them as a true low-cost source for the emerging CWDM market.

Further reductions in CWDM system costs can be achieved through the use of single-chip multi-wavelength sources. Many network positions require transmission at multiple wavelengths. Typically multiple lasers are used at these nodes and each laser is individually packaged with all the required electrical connections and optical alignments. Each of these alignment and packaging steps incurs substantial costs. For a typical system operating across 140 nm from 1471 nm to 1610 nm, eight separate lasers are needed along with eight packages and eight fiber alignments. By integrating all the lasers on a single chip, a single package and a single arrayed drive circuit can be used. If the multi-wavelength devices are actually fabricated together on the same chip, they will all be perfectly aligned to each other, thereby allowing for a single optical alignment of a fiber array. This thesis work lead to the development of the first ever single-chip source for these CWDM applications.

1.4 Multi-Wavelength VCSEL Array Development

Recognizing the potentially substantial cost benefits of a single-chip multi-wavelength VCSEL array for CWDM applications, much research has been

conducted toward their development. Such research has primarily focused on modifying the length of the VCSEL active region, or the entire VCSEL epitaxial layer stack across the wafer surface, to induce a wavelength shift along the lateral position in the final processed laser array. Some techniques have focused on accomplishing this thickness variation during the growth process. One approach has been to hold the wafer at an angle while it is grown [5]. This technique has been used near 980 nm and generated nearly 40 nm of wavelength variation [6]. Another technique has been to pattern the backside of the wafer to induce a thermal gradient during MBE growth [7]. This technique has achieved 20-nm wavelength variation near 980 nm. The most successful of the growth-rate variation approaches in attaining wide wavelength span arrays has been the use of patterned substrate growth [8, 9]. In patterned area growth, the local gradient of the chemical species in the gas phase on the patterned substrate surface changes the growth rate [10]. With patterned area growth, Arai *et al.* have been able to simultaneously grow VCSEL arrays spanning 100 nm. These VCSELs, grown using strained InGaAs quantum wells on GaAs, have a lasing wavelengths ranging from 1030 nm to 1130 nm. Though this range is well outside the wavelength span needed for CWDM applications it is still a significant advancement. In fact, the lasing wavelength window achieved with patterned area growth is not a fundamental limitation as growth technology advancements have continuously pushed the wavelength limits for what can be

achieved on GaAs [11] and epitaxially grown VCSELs at 1550 nm on InP have been demonstrated as well [12]. The more fundamental limitations of this technique are the ability to precisely control the lasing wavelength of the elements of the array, the wavelength separation between the channels, and the quantum-well properties of the across all elements of the array. The work of this thesis overcomes these limitations.

Other techniques for the generation CWDM VCSEL arrays have focused on creating post growth modifications to the VCSEL cavity length. These approaches have included air gaps at wafer bonded interfaces [13], wedge shaped oxidation layers [14], stepped wafer surface etching prior to wafer bonding [15-17], or regrowth of the top mirror [18]. The techniques using wafer bonding have been demonstrated near 1310 nm and 1550 nm and have shown 20 nm of wavelength tuning while the techniques relying on fabrication of devices using traditional growth on GaAs have demonstrated tuning as large as 48 nm near 980 nm [14]. The tuning ranges demonstrated are not fundamental and ranges beyond 48 nm for each technique can be expected as long as there is sufficient gain from the active region to support lasing at the given wavelength. In addition, many of these post growth tuning techniques offer the potential for precise wavelength control. This is specifically true of the air gap and stepped wafer surface etching techniques.

CHAPTER 1: INTRODUCTION

In order to fabricate CWDM arrays that can be used in actual systems, the technology must be capable of precisely positioning the wavelength channels within the array over a wavelength range spanning hundreds of nanometers. In addition, and just as important as the wavelength control, the uniformity of the performance of the wide wavelength span array over temperature must be maintained. In order for all channels in the laser array to function within an un-cooled package in ambient environments that vary as much as 70°C, it is critical that the gain of each of the lasers in the array be properly aligned to the lasing wavelength (cavity-mode) of the laser element in the array. This requirement for control of the alignment between the cavity-mode and gain-peak (also called gain-mode offset) across the array requires that the multi-wavelength laser integration technique be capable of simultaneously controlling the thickness and the material composition of the VCSEL active regions in the CWDM VCSEL array. Patterned area growth is not capable of this level of simultaneous control and neither are any of the other post growth approaches that have been previously applied to VCSELs.

In this thesis work, a technique capable of simultaneously maintaining the required thickness and composition control was developed. For the first time ever, a single-chip multi-wavelength source VCSEL array spanning a 140 nm and meeting many of the requirements of CWDM applications was fabricated.

1.5 This Thesis

This thesis investigates the development of a novel lateral and vertical heterogeneous integration technique called nonplanar wafer bonding [19] and the application of this technique to develop the first ultra-wideband long-wavelength WDM VCSEL arrays ever reported [20]. Nonplanar wafer bonding is a device intrinsic, wafer-scale integration technique capable of simultaneous vertical and lateral integration of arbitrarily device structures and is the first integration technique capable of these functions. The long-wavelength VCSEL arrays fabricated using this technique spanned a record 140 nm on the ITU specified CWDM grid from about 1470 to 1610 nm.

In Chapter 2 nonplanar wafer bonding is presented and developed. In this thesis work, as many as four different complete lattice-matched VCSEL active regions were integrated at a time onto a lattice-mismatched substrate with a single wafer bonding step [19]. The process does not degrade the epitaxial material, is simple, and requires no regrowth steps. Chapter 2 discusses the nonplanar wafer bonding method as well as the scope of applicability of the process to integration applications.

Chapter 3 presents a novel active-region design for enhanced VCSEL performance when optical pumping is used [21]. The new design allows for uniform carrier injection into each quantum well while simultaneously allowing

for pump power absorption efficiencies greater than 80 %. A model to describe the performance of the new design is developed and the performance improvements are verified experimentally. In Chapter 4, the design of an optically-pumped 2-dimensional (2-D) CWDM VCSEL array spanning 140 nm from 1470 to 1610 nm is presented [20]. The design makes use of two integrated active regions to provide gain across all 140 nm of the array. To support the oscillation feedback for the VCSEL across the entire lasing range the design makes use of fully oxidized Distributed Bragg Reflectors (DBRs). The design also uses the newly developed optically-pumped active-region design.

Chapter 5 describes the processing steps involved in the fabrication of the 2-D CWDM VCSEL array. These steps involve the details of the nonplanar wafer bonding process, the fabrication of the fully oxidized DBRs, and the steps required to fabricate the entire VCSEL array. Chapter 6 then presents the successful CWDM array results and analysis of the test results. The finished arrays spanned 140 nm from 1470 to 1610 nm, operated single mode to temperatures above 65 °C, demonstrated precise wavelength control, and had only +/1 dB of output power variability. In Chapter 7 the thesis work is summarized and conclusions about the integration technique and the CWDM VCSEL array approach are drawn. Directions for future research are presented in Chapter 7 as well.

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Chapter 2

Integration by Nonplanar Wafer Bonding

Many types of heterogeneous integration techniques have been developed to combine different optoelectronic device structures on a single chip. One subset of these techniques allows for the different integrated structures to be internal and intrinsic to the device being fabricated. These device intrinsic techniques allow more complicated device structures to be fabricated through a combination of multiple simpler structures. Such device intrinsic integration techniques are important to advanced single-chip PICs.

A prominent device intrinsic integration technique is the wafer bonding of III-V semiconductor materials [1]. Wafer bonding is a wafer-scale vertical integration technique that has been proven to be of great utility in the fabrication of high performance VCSELs [2-4] by allowing for the integration of high-

performance AlGaAs DBRs with high-quality InP-based active regions. The details of this type of integration have been well specified and explored [5, 6].

In order to develop wideband multi-wavelength VCSEL arrays for applications such as CWDM, it is necessary to create a well controlled lateral variation in peak gain wavelength across the surface of the wafer. In optically-pumped structures, periodic gain is often employed to maximize performance and a separate quantum well, or cluster of wells, is located at each standing wave peak within the VCSEL active region. For wide wavelength span arrays, this requires the structure of the VCSEL active region also to be modified across the surface of the wafer so that the widely varying periodicity of the standing wave peak across the multi-wavelength array will match the periodicity of the active-region quantum-well spacing. Such structural variation is also necessary to control the thickness of the active region and to allow for different numbers and types of quantum wells to be used for different elements in the array.

Thus, to fabricate high-performance wideband CWDM VCSEL arrays it is necessary to have a wafer-scale device intrinsic vertical and lateral heterogeneous integration technique. Such a technique has been developed in this thesis work and is presented here. This technique may allow for the monolithic integration of various optical, electrical, and micromechanical components on a single wafer. Nonplanar wafer bonding allows epitaxial regions, optimized for specific applications, to be integrated onto a single planar

wafer in a single step. As an integration technique it is generic in its application and is well suited for many types of lateral and vertical integration challenges, including wavelength division multiplexed laser arrays and the integration of electronics with lasers, photodetectors, and modulators.

2.1 General Nonplanar Wafer Bonding Concept

The technique of nonplanar wafer bonding has been developed in this work as a means to achieve a wafer with multiple epitaxial regions in a single wafer bond step [7]. Nonplanar wafer bonding can achieve lateral heterogeneous integration by means of a vertical to lateral transformation of epitaxially grown structures. This technique allows for large-scale monolithic integration of lattice-mismatched materials in the vertical direction and the lateral integration of dissimilar lattice-matched structures.

Two different types of nonplanar wafer bonding were explored in this thesis work. The first type is called backside-processed nonplanar wafer bonding. The second process is called nonplanar pressure block nonplanar wafer bonding. As is obvious from the names, both techniques involve the bonding of nonplanar wafer surfaces, but they differ in how this bonding is accomplished. The first process was developed to prove the principle but involved more difficult processing. The second technique is easier to process

but requires more carefully designed wafer-bonding fixtures. The majority of the process and bonding details will be reserved for Chapter 5.

In this chapter, both types of nonplanar wafer bonding will be described and experimentally verified. A mechanical model for the nonplanar pressure block technique was developed and is presented here. Both techniques were used in this thesis to fabricate multi-wavelength VCSEL arrays, but the final wideband CWDM array was fabricated using the nonplanar pressure block approach and these results will be withheld until Chapter 6. Laser results utilizing the backside processed technique are presented here but only in summary form as these results are only for demonstrating the proof of principle.

2.2 Backside Processed Nonplanar Wafer Bonding

General nonplanar wafer bonding begins with multiple epitaxial regions grown vertically on a wafer as shown for the case of four different quantum-well regions in Figure 2.1. The epitaxial surface is then etched with a step shaped profile to reveal a different epitaxial region on the landing of each step level as shown in Figure 2.2(a). In backside processed nonplanar wafer bonding, the backside of the wafer is also etched with a profile complementary to the step etched epitaxial film side of the wafer, as shown in Figure 2.2(b). This substrate thickness adjustment etch is designed to yield an identical substrate plus sides of the wafer, it is then prepared for direct wafer bonding [5] to a transfer substrate

as shown in the schematic in Figure 2.2(c). The bonding takes place in a graphite pressure fixture at elevated temperatures near 600°C and at pressures

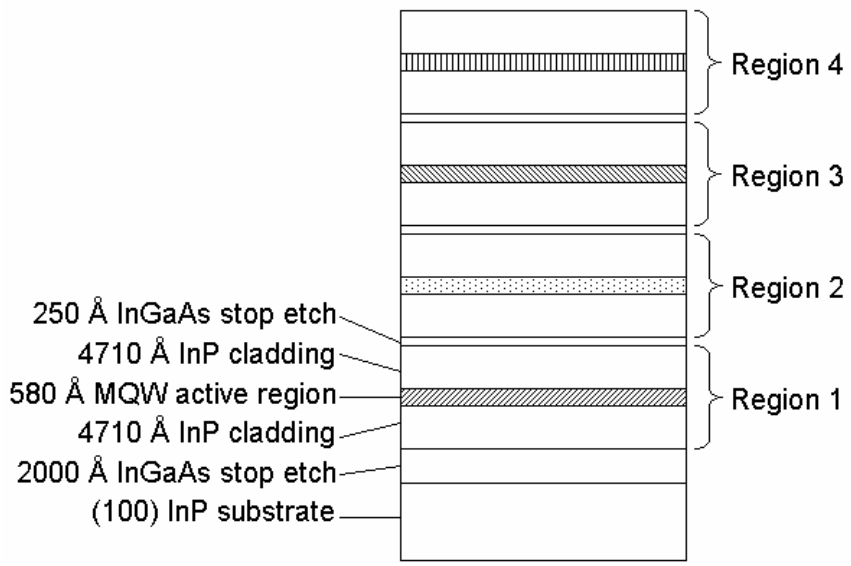

Figure 2.1. Schematic of an example structure with four quantum-well regions epitaxially grown on a substrate.

around 1.7 MPa. The transfer substrate may have a crystal lattice constant that differs from the growth substrate. In this research the growth substrates used were InP and the transfer substrates were GaAs. After the wafers are wafer bonded to each other, they are removed from the graphite fixture at room temperature. The original growth substrate is etched off and the epitaxial layers remain attached to the transfer substrate as depicted by Figure 2.2(d). It is clear that at each lateral position a stack of epitaxial material remains, including material that is in excess of what is ultimately desired. Thus, the excess epitaxial layers are etched back, leaving one different epitaxial region at each

lateral position on the transfer substrate as represented by Figure 2.2(e).

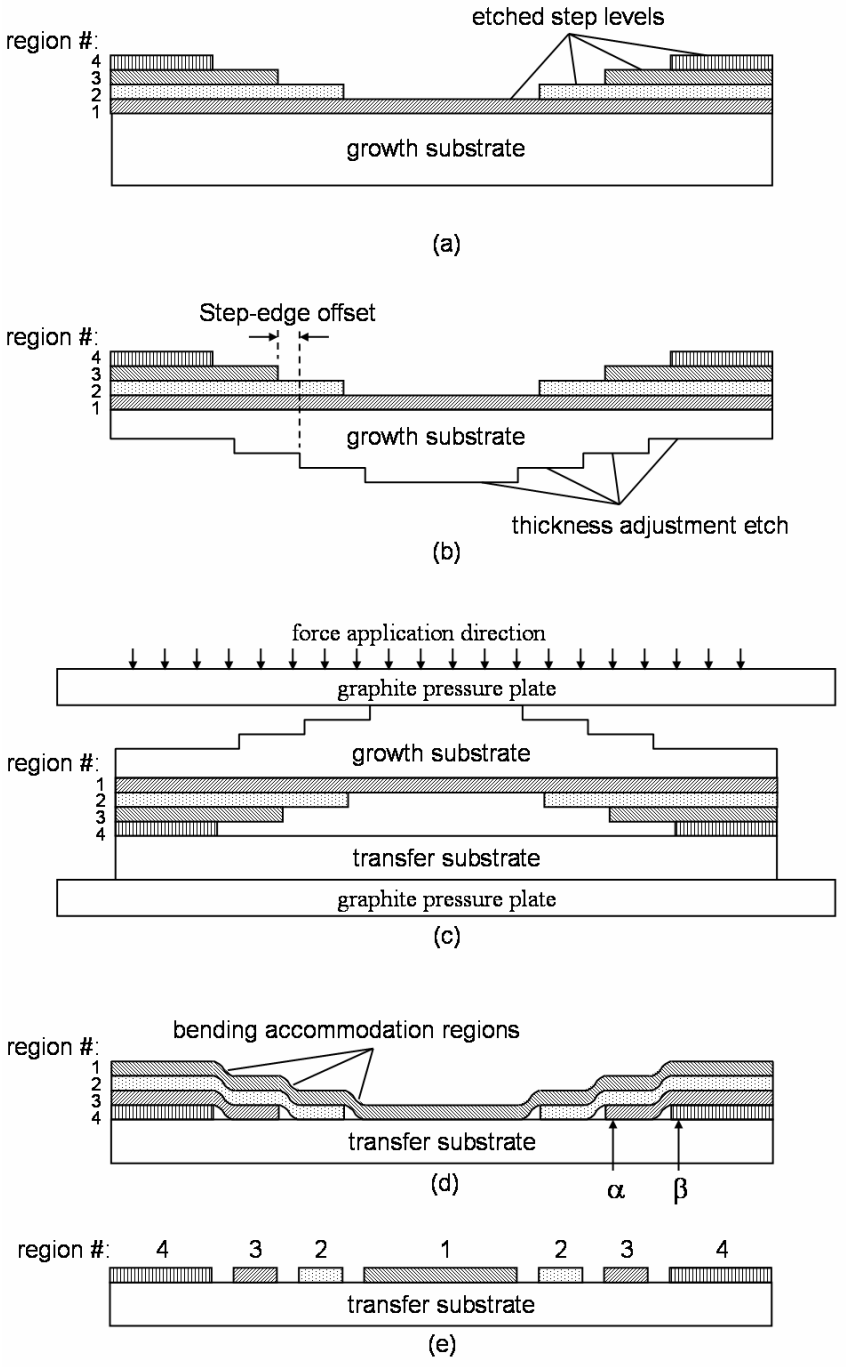

Figure 2.2. Cross-section schematics depicting: (a) the epitaxial film side of the as-grown wafer etched with a step profile, (b) the epitaxial film side and backside of the as-grown wafer etched with a step profile, (c) the step-etched sample undergoing direct wafer bonding to the transfer substrate prior to elastic deformation, (d) the epitaxial layers bonded to the transfer substrate with the growth substrate removed (α and β denote the observations points for Figure 2.5), (e) the original vertically grown epitaxial regions now laterally integrated on the transfer substrate after nonplanar bonding, growth substrate removal, and the etch-back of the excess epitaxial layers.

The technique relies on the ability of the wafer to bend slightly under pressure. This bending has been shown previously for very small step heights on the order of hundreds of angstroms [8, 9]. The present technique can accommodate greater step heights by using a backside thickness adjustment etch to promote bending of the wafer and by using a lateral offset between the step edges on the epitaxial film side of the wafer and the step edges of the backside etch. These step-edge offsets are shown in Figure 2.2(b). When pressure is applied during direct wafer bonding, pressure on the backside of the wafer will be concentrated on the step edges and will be transferred through the substrate and promote the flattening of the step-etched epitaxial layers against the transfer substrate. The lateral offset between the front-side and backside step edges determines the distance over which the substrate and epitaxial layers must bend. These bending accommodation regions are etched away during the growth substrate removal steps and during the removal of the excess epitaxial material. The laterally varying epitaxial regions remaining on the transfer substrate after the etch-back step have not been bent and retain their material qualities after bonding, as has been verified by the experiment outlined below.

2.2.1 Experimental Verification

To test the suitability of the backside processed nonplanar wafer bonding technique for heterogeneous integration, four different unstrained multi-quantum-well (MQW) active regions were grown on (100) InP by metal organic chemical vapor deposition (Figure 2.1). The MQW active regions consisted of three 60 Å InGaAsP quaternary (Q) quantum wells with 100 Å 1.1 μm Q barriers. Each of the four regions was separated by a 250 Å InGaAs stop etch layer for ease of processing and substrate removal. The photoluminescence (PL) peaks of the four regions were intentionally made different to ultimately achieve different PL peaks at laterally adjacent regions on the wafer. The regions had PL peaks at 1280, 1336, 1260, and 1320 nm, listed in order of their growth on the substrate. Each region had a thickness of 1 μm, for a total epitaxial film thickness of about 4 μm.

The epitaxial layers were selectively chemical etched with a step profile to reveal a different region on each step level. The step levels were 500 μm wide and 1.025 μm high. The one square centimeter sample was thinned to 200 μm and the backside was chemically etched with the same step profile as the epitaxial film side, except with a 200 μm lateral step-edge offset. The photoluminescence of the wafer was measured at each step level prior to the

direct wafer bonding of the epitaxial layers to a (100) GaAs substrate. The semiconductor direct wafer bond was performed at 630 °C for 30 min in a nitrogen gas ambient under pressure in a graphite fixture. The pressure used in this verification experiment was 3 MPa. This pressure is similar to the pressure used in the planar bonding of InP to GaAs in the fabrication of 1.55 μm vertical-cavity surface-emitting lasers. Subsequent research has revealed that this pressure can be reduced if the InP substrate thickness is further reduced (the stiffness of the substrate is proportional to the cube of the thickness). The bond temperature has also been reduced to 600 °C in subsequent experiments. This temperature reduction is desirable to ensure that the quantum wells are not damaged by the bonding temperature.

After direct bonding the InP to the GaAs transfer substrate, the InP substrate was removed by a selective chemical etching. The excess epitaxial layers and the deformation accommodation regions were etched back by selective chemical etching to reveal bonded stripes of MQW active regions across the GaAs transfer substrate surface.

Figure 2.3 shows the stripes of bonded epitaxial regions separated by the etched deformation accommodation regions. The majority of the sample surface was bonded. The roughness of the deformation accommodation regions is due to the uneven etching of the GaAs transfer substrate during the etch-back process. The horizontal stripes present in some of the regions are due to

bonding channels that were intentionally etched into the surface to allow for fluid escape during bonding. Subsequent work has determined that the bending regions are sufficient for this purpose and the extra channels are not necessary. PL measurements recorded after wafer bonding are shown in Figure 2.4. The PL prior to wafer bonding is not shown, but comparison with the PL plots in Figure 2.4 indicates no degradation in the intensity, no shift in the wavelength, and no broadening of the PL peaks after wafer bonding. Optical inspection of the surface shows a well-bonded surface with little damage due to bonding. Scanning electron microscopy of the bonded interface also reveals a uniform wafer bonded interface (Figure 2.5).

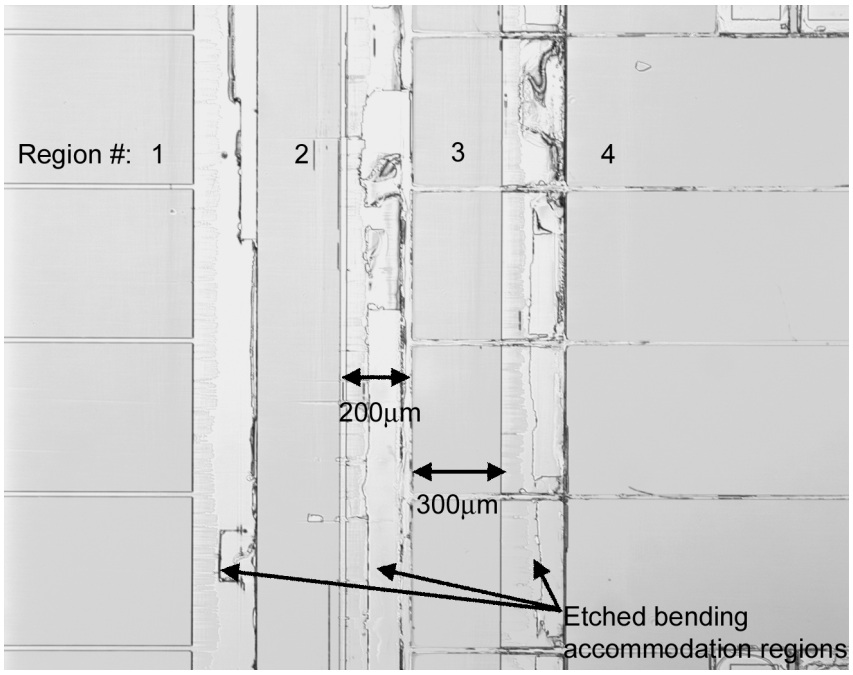

Figure 2.3. Optical photograph of the surface of the transfer substrate after substrate removal and the etch-back of the excess epitaxial layers. Etched bending accommodation regions separate the four bonded regions.

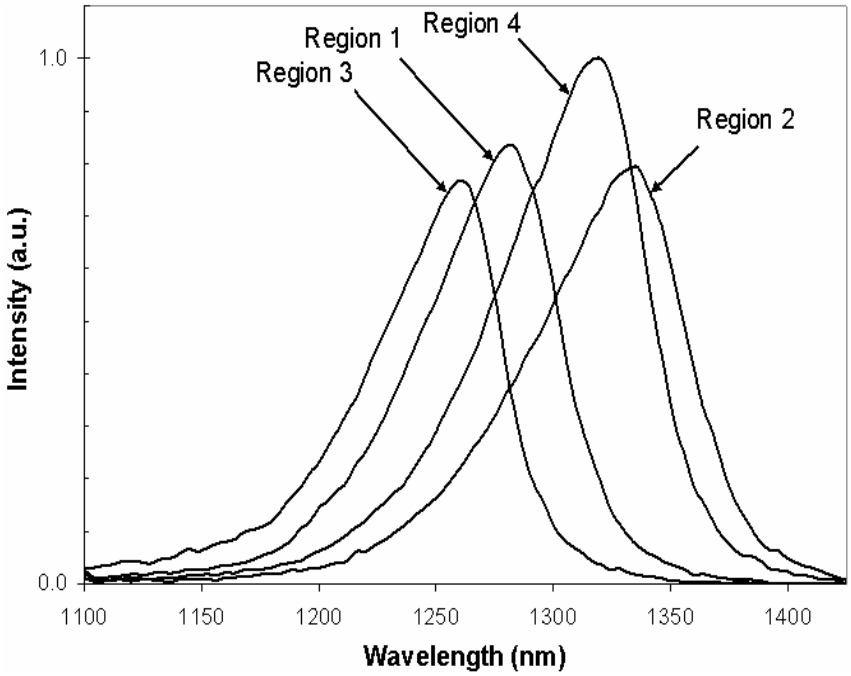

Figure 2.4. Photoluminescence from the four different bonded epitaxial regions after the nonplanar wafer bonding process.

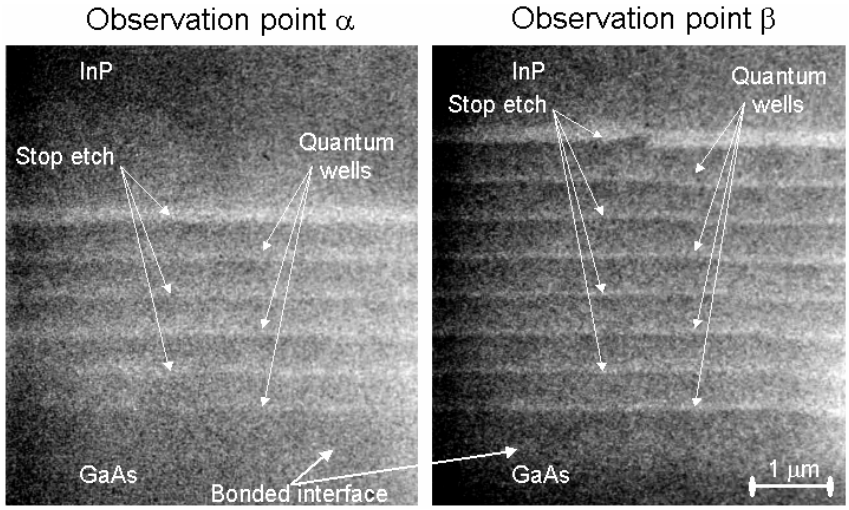

Figure 2.5. Cross-section scanning electron micrographs of the bonded interface recorded at the two observation points schematically depicted in Figure 2.2(d). These micrographs were recorded prior to the InP substrate removal.

The combination of good PL and a mechanically well-bonded surface leads to the conclusion that the backside processed nonplanar wafer bonding

technique is a viable method for achieving vertical and lateral heterogeneous integration across a wafer.

With this initial experiment, the use of nonplanar wafer bonding to achieve vertical and lateral heterogeneous integration on a wafer has been demonstrated. Scanning electron microscopy and optical inspection have confirmed the good bond quality of the direct nonplanar wafer bond. Photoluminescence after wafer bonding confirms that the optical properties of the MQW active regions were maintained after the bonding process.

2.2.2 Laser Results

In order to verify the suitability of nonplanar wafer bonding and the backside processed approach, a 2-dimensional (2-D) multi-wavelength laser array was fabricated using two active regions integrated with nonplanar wafer bonding. The optically-pumped multi-wavelength VCSEL was the first two-dimensional WDM VCSEL array covering the C-band ever fabricated. The array used eight channels on an approximately 4.5-nm pitch to extend from 1532 nm to 1565 nm. Details regarding the design of the active region, optical pumping, the modal confinement, and the wavelength control will be reserved for the VCSEL design section of Chapter 4.

The nonplanar wafer bonding procedure used is similar to that just described except only two active regions were integrated. The fabrication of the

device began with two strained periodic-gain multi-quantum-well long-wavelength VCSEL active regions grown vertically on an InP wafer and separated by an etch-stop layer. The active regions had optical-cavity lengths of 2.5 wavelengths at 1565 nm and 1547 nm and, for this demonstration both had photoluminescence peaks at 1530 nm. In addition, the active regions used a two-period superlattice on one side that could be used for additional wavelength control in the second axis of the final two-dimensional array [8, 9]. The details of this superlattice and its design are covered in Chapter 4 and References 9 and 10 give a thorough description.

The wafer surface is etched with a single step profile to reveal each of the two active regions on a different step level. Again, the backside of the wafer is etched to have a profile complementary to the step-etched active-region side of the wafer, as shown in Figure 2.6(a). The nonplanar wafer is direct wafer bonded to a 40-period AlGaAs distributed Bragg reflector (DBR) grown on a GaAs substrate. The original InP growth substrate is removed, leaving the two laser active regions attached to the AlGaAs DBR on the GaAs substrate as depicted in Figure 2.6(b). After removal of the excess active-region material and the bending regions, a different active region is left at alternating lateral positions on the AlGaAs mirror as represented by Figure 2.6(c). At this point, the original superlattice that was grown on each active region is etched with a step-shaped profile to trim the cavity resonance of each of the two separate

active regions in the second dimension of the wafer surface. Figure 2.7 shows a schematic of a small section of the wafer surface after the superlattice etches.

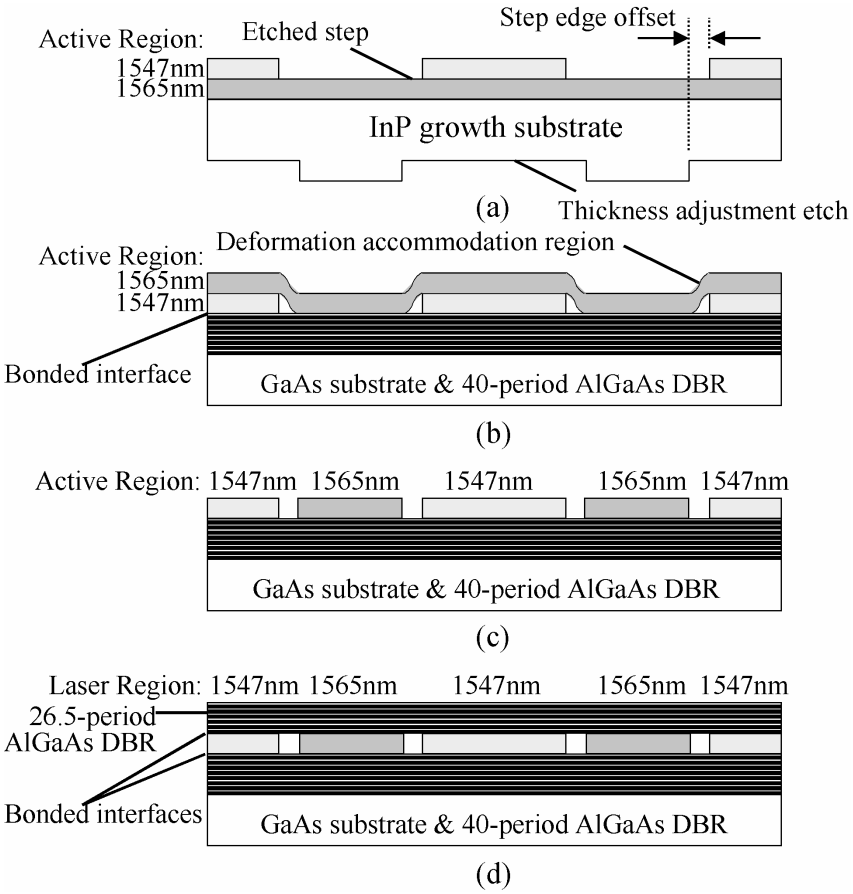

Figure 2.6. Process-flow cross-section schematic depicting: (a) the epitaxial-film side and backside of the as-grown wafer etched with a step profile, revealing separate VCSEL active regions at different lateral points on the wafer surface, (b) the VCSEL active regions bonded to the AlGaAs DBR with the InP growth substrate removed, (c) the original vertically-grown VCSEL active regions now laterally integrated on the AlGaAs-DBR surface after nonplanar wafer bonding, growth substrate removal, and the etch back of the excess epitaxial layers, (d) the complete VCSEL array structure after bonding the second AlGaAs DBR and removing the GaAs substrate.

Figure 2.8 is a photograph of the wafer surface in the same region shown in Figure 2.7 and indicates the location of the eight channels in the final VCSEL structure. Each of the separate wavelength regions is about 500 μm wide. A

250-μm region where the deformation accommodation region was removed separates the two active regions from each other. A second, 27-period, AlGaAs DBR is bonded by traditional semiconductor-direct bonding to create the structure shown in Figure 2.6(d). One half-period of the mirror is used as the etch-stop layer for the substrate removal, leaving a 26.5-period DBR. Figure 2.6(d) shows a cross-section schematic of the eight-wavelength VCSEL array structure. Index guiding in the VCSEL structure is accomplished with 30-nm tall, circular post index guides that are etched into the surface of the top DBR prior to the second wafer bond. The index guides are 8 μm in diameter and are located at the bonded interface in the final device structure.

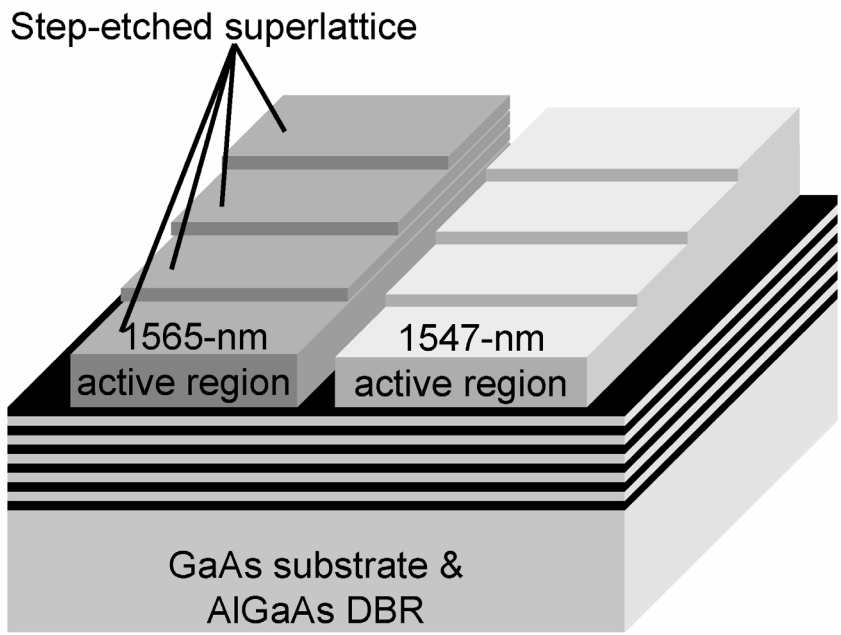

Figure 2.7. Three-dimensional schematic of a small section of the wafer surface after the completed nonplanar wafer bonding of the VCSEL active regions in the first dimension and the completion of the superlattice etches in the second dimension.

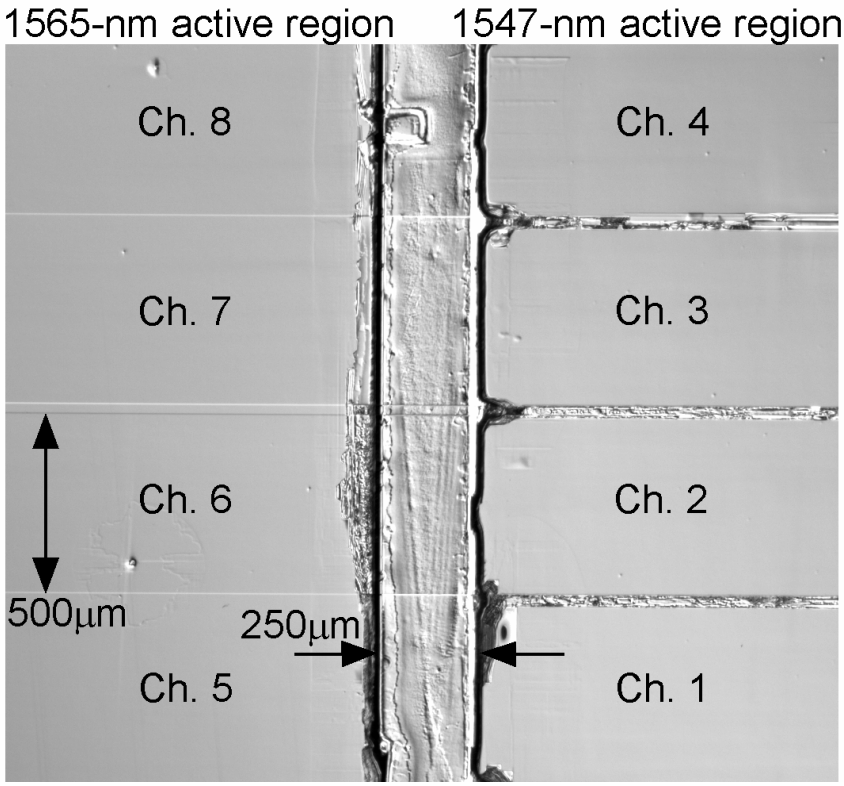

Figure 2.8. Photograph of the wafer surface showing the two VCSEL active regions laterally adjacent on the AlGaAs DBR after nonplanar wafer bonding. Four separate wavelength-channel locations per active region are defined by the superlattice etch.

The final structure was an eight-channel, two-dimensional, WDM VCSEL array. The array is optically pumped with a 980-nm pump laser, a technique that has been commercially implemented in a wafer-scale process [3, 11]. The periodic-gain active regions utilize about 680 nm of 1.35-μm InGaAsP barrier material and have single-pass absorption efficiencies of about 80%. Figure 2.9 shows the room-temperature lasing spectra at a constant absorbed pump power of 10.5 mW for each device. There is a 2-dB variation in the output power at this constant pump power. The devices all exhibit single-mode

operation with the worst-case side-mode suppression ratio of 43 dB occurring in the fourth channel. The excess wavelength separation between the fourth and the fifth channel is a result of a growth-rate error during the growth of the 1565-nm active region.

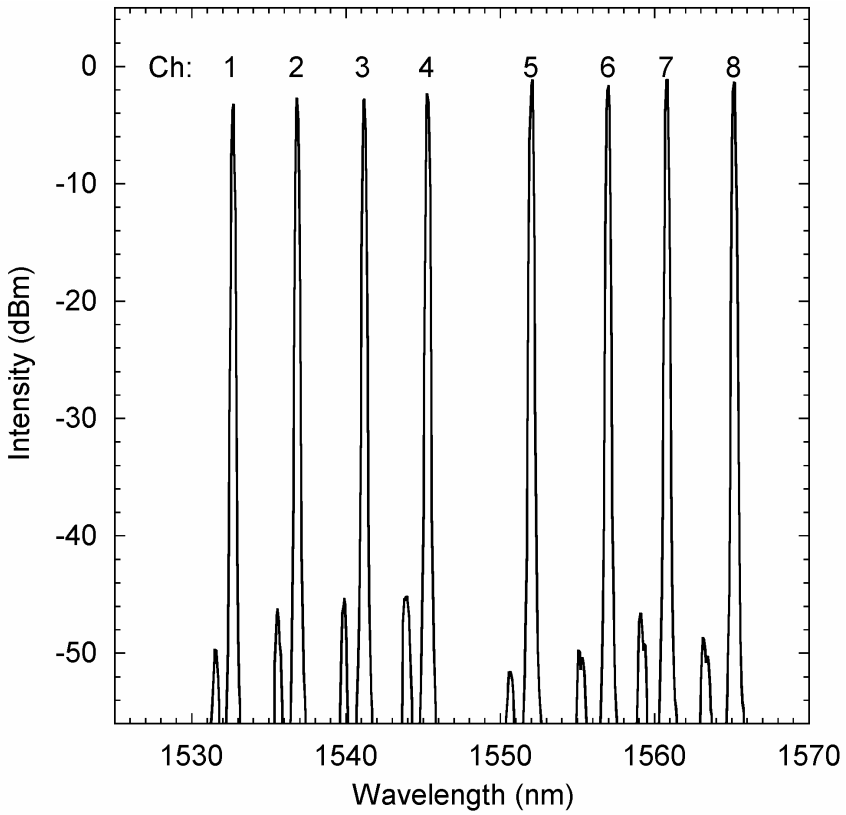

Figure 2.9. Superimposed room-temperature VCSEL emission spectra from the eight-channel WDM VCSEL array measured at a constant absorbed pump power of 10.5mW.

By using nonplanar wafer bonding, the first long-wavelength, two-dimensional, WDM VCSEL array was fabricated. The devices exhibited high-quality single-mode emission over the range of 1532 nm to 1565 nm. This demonstration, though simple and not necessarily requiring nonplanar wafer

bonding to implement, showed that nonplanar wafer bonding can be used as a lateral heterogeneous-integration technique in the fabrication of VCSEL arrays.

As will be discussed in detail in Chapter 5 when the nonplanar bonding process is elaborated, the greatest challenge with the backside processed nonplanar wafer bonding in the processing of the backside of the sample. The next section describes an alternative approach that solves this difficulty.

2.3 Nonplanar Wafer Bonding With a Nonplanar Pressure Block

In order to simplify the processing and improve the reproducibility of the nonplanar wafer bonding process, a second approach was developed [12]. The approach makes use of a nonplanar pressure block placed against backside of the thinned growth substrate instead of processing the backside of the substrate. The nonplanar pressure block is fabricated in InP and it is anticipated that the pressure block could be reused in a manufacturing environment requiring repeated application of the process on multi-wafer lots. The simplified technique is described here along with actual integration results and a numerical simulation and optimization of the integration technique.

The nonplanar pressure block process flow is shown in Fig. 2.10 for the case of the integration of two active regions. The first steps of the

heterogeneous integration technique are similar to those used for the backside processed nonplanar wafer bonding approach. The technique begins with the growth of at least two separate and distinct epitaxial device structures on a wafer such as InP. These structures are grown one after the other on the growth substrate, as shown in Figure 2.10(a). After growth, the wafer surface is etched with a step-shaped profile to reveal a different device structure on the top of each step level as shown in Figure 2.10(b). The backside of the growth substrate is typically lapped to a final thickness of about 100 μm. The wafer surface is cleaned to remove particles and then placed in contact with a transfer substrate such as GaAs. The epitaxial layers are wafer bonded to the transfer substrate layers by applying pressure and heat in a graphite fixture. A reusable nonplanar pressure block insert is used adjacent to the back of the InP growth substrate in the bonding fixture as shown in Figure 2.10(c).

As in the backside processed approach, there is a lateral offset between the step corners on the nonplanar pressure block and the step corners on the InP epitaxially grown surface. This step-edge offset allows a space for the wafer material to bend when pressure is applied. The length of this step edge offset is typically about 200 μm. The alignment of the steps in the pressure block to the steps on the front of the growth substrate is critical and is described in the Chapter 5. The nonplanar pressure block is fabricated from InP with step heights equal to those on the front of the growth substrate. InP is used for the

pressure block to match the thermal expansion of the growth substrate and maintain the front-side to backside alignment.

The shape of the nonplanar pressure block causes the growth substrate to conform to the transfer wafer surface when pressure is applied, as shown in Figure 2.10(d). The bending of the material in the step-edge offset region is visible in this figure. With about 1.7 MPa of pressure applied, the wafer stack is baked at 600°C for 30 minutes thus bonding the epitaxial structures to the GaAs transfer substrate. Figure 2.10(e) depicts the InP wafer bonded to the GaAs transfer substrate after removal from the bonding fixture. At this point, the epitaxial device structures exposed on the surface of the InP growth substrate have been transferred to the planar surface of the GaAs transfer substrate. The original InP growth substrate is then removed along with the excess epitaxy. What remains are different epitaxial device structures located adjacent to each other on the surface of the transfer substrate as shown in Figure 2.10(f).

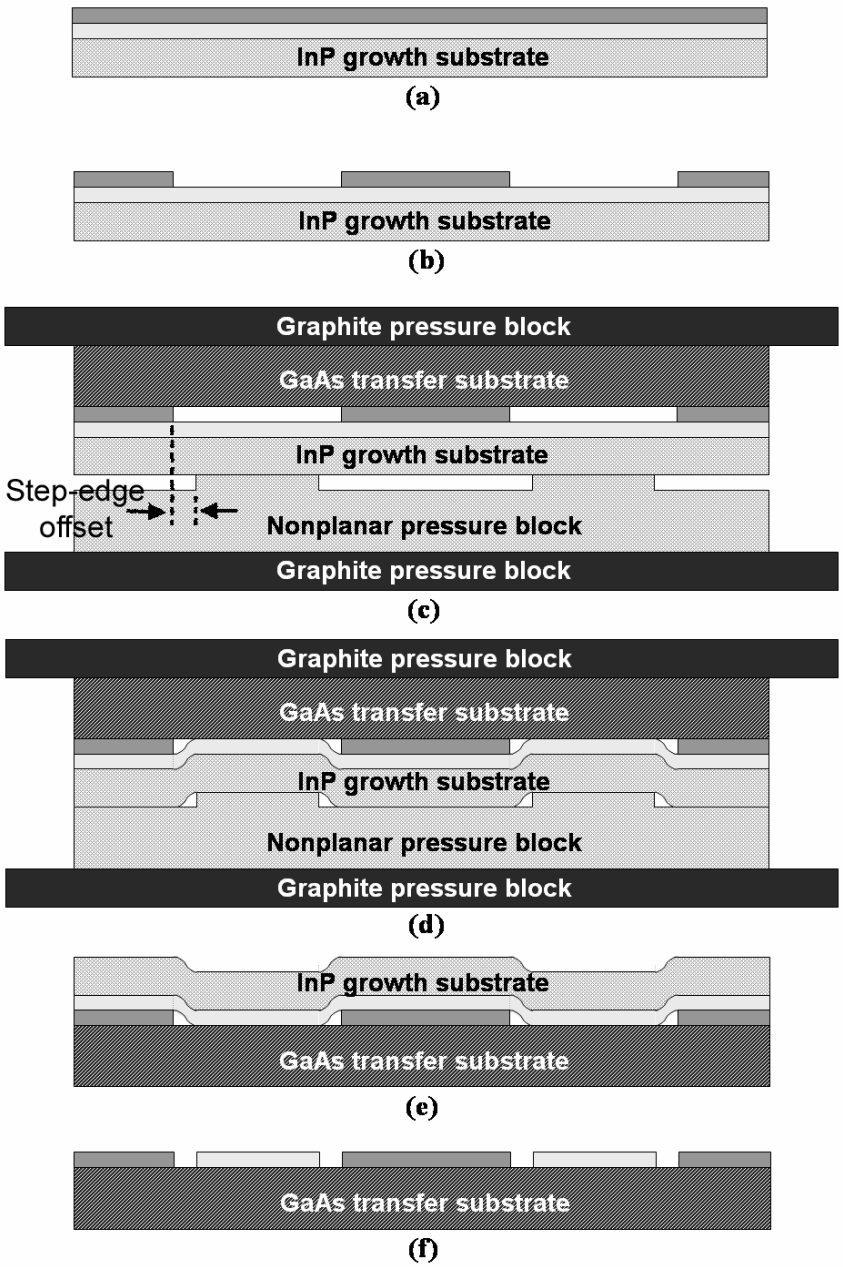

Figure 2.10. Simplified nonplanar wafer bonding process flow schematic.

Comparison of Figures 2.2 and 2.10 shows that the second process does not require any nonstandard process techniques such as the backside processing

shown in Figure 2.2. Other than this change, the two techniques are fundamentally the same.

Figure 2.11 is a photograph of a small region of a sample surface after using nonplanar wafer bonding to integrate two VCSEL active-region structures with a pressure of 1.7 MPa. For this demonstration, the InP substrate was lapped to a thickness of 100 μm and the step-edge offset used was 200 μm. The excess epitaxy was etched back an extra 50 μm on each side of the top-level epitaxial layer region to yield the 250-μm gaps shown. This photograph is typical of the sample surface after nonplanar wafer bonding and the area yield across the sample was estimated to be about 80%.

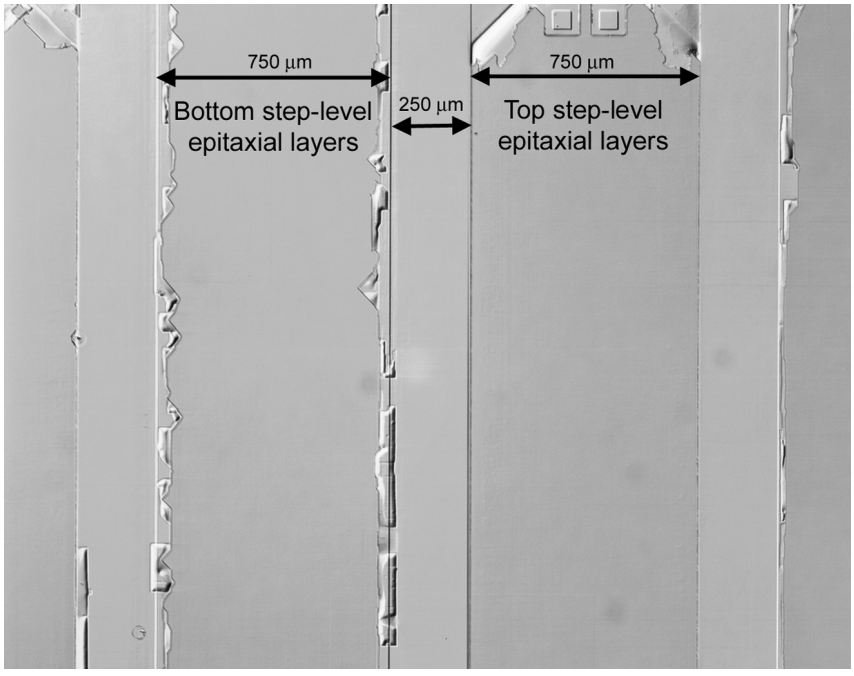

Figure 2.11. Photograph of two laser active regions integrated by nonplanar wafer bonding using 1.7 MPa of applied pressure. The square features in the upper right side of the photo are alignment targets.

2.3.1 Simulation

Numerical simulations of the nonplanar wafer bonding process using ANSYS was performed to better understand the compliance of the InP wafer during the application of pressure. ANSYS allows a complete mechanical model of the nonplanar wafer bonding process to be built. The primary parameters that are desired from such a model are the uniformity of the pressure, the size and position of the predicted voids, and the total stress in the epitaxial material on the surface of the InP growth substrate that is being integrated onto the GaAs substrate. Issues related to heating and cooling the sample were not investigated and a steady state analysis at a fixed temperature was conducted.

Figure 2.12 shows the results of nonplanar bonding when only 1.1 MPa is used. Large voids are visible at the edges of the alternating regions of the top step-level epitaxial regions. These voids occur when there is insufficient pressure to achieve full contact between the InP and the GaAs substrates. The ANSYS simulations were calibrated to the experimental observations in Figures 2.11 and 2.12 using the value of the Young's Modulus for InP at 600 °C as the fitting parameter. The pattern of bonded area and voids in the actual bonds shown in Figures 2.11 and 2.12 were matched to the simulation by adjusting the modulus from its room temperature value of 61 GPa [13] to 13 GPa at 600 °C.

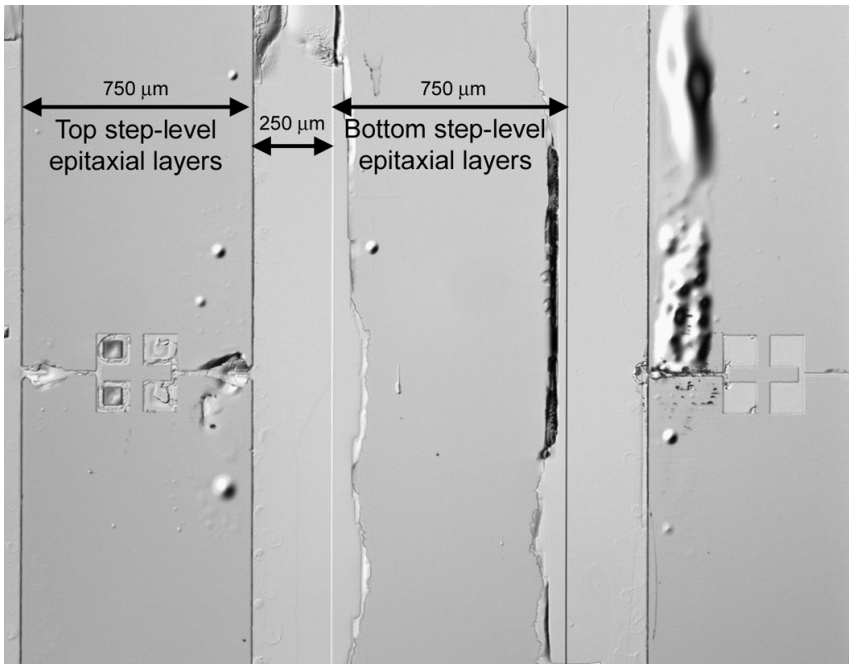

Figure 2.12. Photograph of two laser active regions integrated by nonplanar wafer bonding using 1.1 MPa of applied pressure.

Figure 2.13 shows the predicted von Mises stress in the nonplanar bonded epitaxial layers during the bonding step shown in Figure 2.10(d). The von Mises stress is given by Equation 2.1 where σ_x, σ_y, and σ_z are the principle stresses acting normal to the surface of a unit cube of the material (an isotropic material is assumed) [14]. The von Mises stress accounts for the coupling between the three principle stresses and can be used to analyze the total stress at a given point in the material. Areas of high stress are located near the corners of the steps and in the bending regions defined by the step-edge offset. Figure 2.13 also shows the measured full width at half maximum intensity (FWHM) of a small spot (5 μm) photoluminescence (PL) scan across the integrated active regions shown in Figure 2.11. As expected, the FWHM rises sharply as the total

stress increases, indicating localized permanent material damage near the edges of the integrated regions. The majority of the area is not subjected to excessive stress and no degradation of the PL is observed. From Figure 2.13 it is possible to estimate the stress threshold for degradation of the PL. This threshold estimate is 5 MPa.

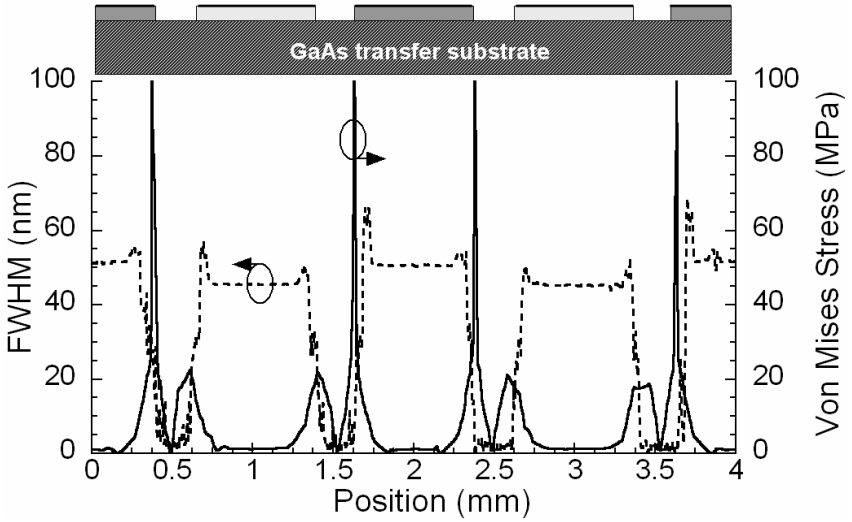

Figure 2.13. Measured PL FWHM and calculated von Mises stress resulting from the application of nonplanar wafer bonding to integrate two laser active regions (stress peaks are truncated for scaling purposes).

$$(2.1)\ \sigma_v = \sqrt{\frac{(\sigma_x - \sigma_y)^2 + (\sigma_y - \sigma_z)^2 + (\sigma_x - \sigma_z)^2}{2}}$$

2.3.2 Optimization Predictions

With a calibrated numerical module for the nonplanar wafer bonding process, and an estimate for the threshold of the stress induced damage to the PL of the quantum wells, it was possible to experiment numerically with different sample

geometries to optimize the nonplanar bonding process and predict the extent of its capabilities. The geometry modified in this investigation was the thickness of the lapped InP substrate. The goal of optimization is to find a nonplanar bonding geometry that maximizes the fraction of undamaged bonded area while maximizing the thickness of the lapped InP substrate for practical wafer handling reasons. The numerical model allows us to find the optimal InP substrate thickness and applied pressure conditions to meet this goal.

In the simulations, 50-μm, 100-μm, and 200-μm lapped InP substrate thicknesses with a 200-μm step-edge offset length were investigated. The nominal width of the top-level epitaxial regions was 750 μm with a 2-mm center-to-center spacing. The anticipated maximum bonded area with this geometry is 80%. Figure 2.14 shows a plot of the fraction of undamaged and fully bonded area for each of the different geometries for differing amounts of applied pressure. The fraction of undamaged bonded area is determined from the results of the simulation by summing the areas shown to be in full contact and subtracting the portions where the total stress in the contacted material exceeds 5 MPa. These regions are expected to yield bonded area with uncompromised PL that is suitable for semiconductor devices. The pressure range was limited on the low side by the ability of the numerical simulation to converge to a solution.

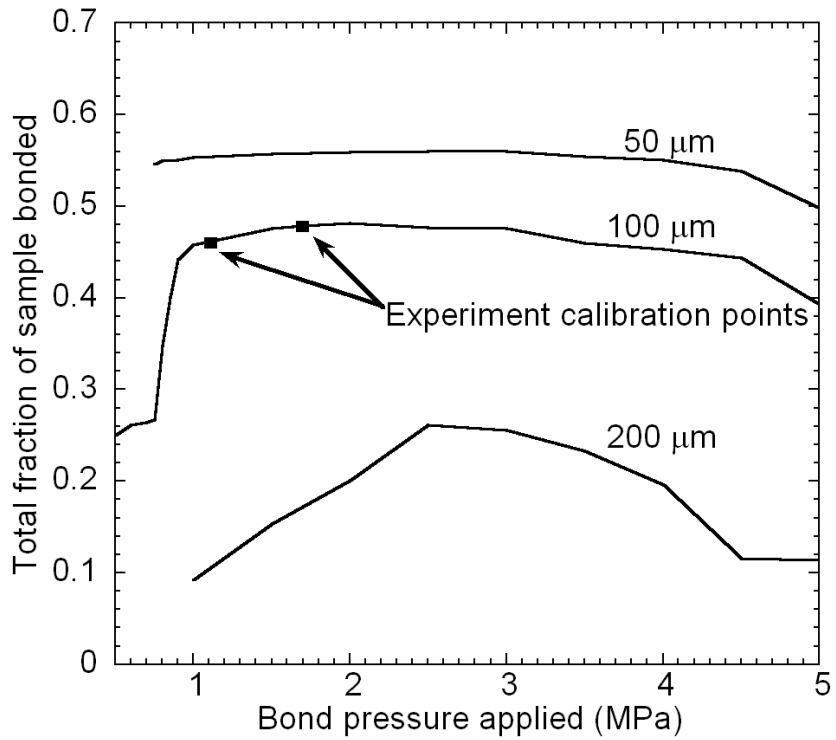

Figure 2.14. Simulation results comparing nonplanar wafer bonding using three different InP substrate thicknesses.

From the plot in Figure 2.14, it is evident that the substrate thickness of 200 μm is not suitable for nonplanar bonding, at least with 200-μm step-edge offsets. With this thick substrate, the stepped epitaxial surface is not able to conform to the planar GaAs surface without applying excessive stress to the epitaxial material. For both the 100-μm and 50-μm thick substrates a wide range of acceptable pressures, spanning from 1.5 MPa to 3 MPa, exist for which the process can be successfully applied. Below this range, voids are present in the bonded material and above the range the excessive stress begins to damage the material. It is clearly advantageous to thin the InP substrate to improve the

usable bonding area. By thinning the substrate by a factor of ½, from 100 μm to 50 μm, the peak bonded area fraction improves by 16 % to 56 %. This improvement comes at a cost of added difficulty in handling the thinned wafer and the 100-μm thick substrate is likely a more suitable operating point. For the 100-μm thick substrate, the peak usable bonded area fraction is about 48 %. For many applications, such as laser and drive electronic integration and multi-wavelength laser emitter integration, this usable area ratio is sufficient and the added chip functionality enabled by nonplanar bonding justifies the reduction in usable area.

2.4 Alternate Nonplanar Wafer Bonding Configurations

The previous sections have described two specific methods of applying nonplanar wafer bonding. Both of the methods demonstrated used 200-μm bending regions. In addition, the pattern of the laterally integrated device structures matched the growth ordering on the sample and repeated continuously across the wafer surface. Thus an A-B-C-D growth ordering resulted in an A-B-C-D-C-B-A repeating pattern for the laterally integrated regions. The nonplanar wafer bonding integration technique, as it has been presented here, was designed to simplify the process and increase the likelihood of success.

The bending region length and integrated structure ordering is not intrinsic to the general technique of nonplanar wafer bonding. Techniques such as reducing the bending region length can increase the amount of usable area on the finished substrate. This however requires a thinner substrate to allow the wafer to conform to the transfer substrate surface. In addition using alternate laterally-integrated layer ordering on the transfer substrate increases the flexibility of the integrated chip design but requires the use of greater step heights during nonplanar wafer bonding.

Figure 2.15 demonstrates a potential alternate technique for nonplanar wafer bonding which would allow for arbitrary lateral structure ordering. Such an approach requires exposing the appropriate layers adjacent to each other on the wafer surface. With this approach the step heights required will be higher than those of the previously demonstrated approaches. With non-uniform step heights, the bending region lengths required will not be uniform as is evident in Figure 2.15(b). Such an approach will benefit greatly from a reduction in the bending region length. The most natural way to accomplish this is to reduce the substrate thickness. The substrate thickness can generally be reduced anywhere along the continuum from the full substrate thickness to only the epitaxial layer thickness as long as a suitable method for handing the structure is employed.

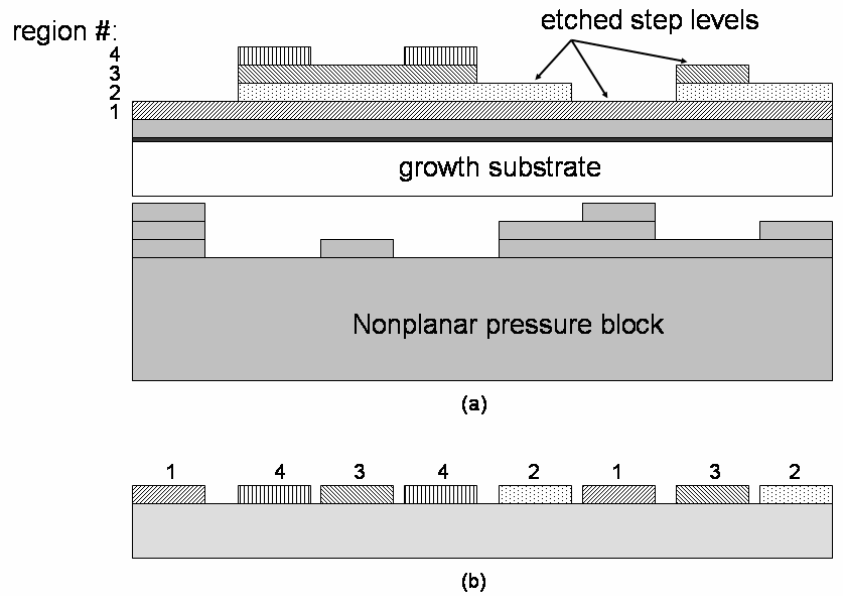

Figure 2.15. Schematic of alternate nonplanar bonding approach demonstrating arbitrary lateral structure ordering.

2.5 Nonplanar Wafer Bonding Summary

The results of both experiment and numerical simulation confirm that nonplanar wafer bonding is a technique can be used to integrate many different device structures on a single chip and represents an advance in the level of optical, electrical, and micromechanical integration possible. It is the only wafer-scale vertical and lateral heterogeneous integration technique and it allows for the simultaneous integration of multiple device regions with an integration interface that can be intrinsic to the device. Using the technique, the first ever long-wavelength 2-D WDM VCSEL array was fabricated.

Nonplanar wafer bonding allows for multiple dissimilar device regions to be integrated using a single wafer bonding step. No selective area growth,

regrowth, or repeated high temperature processing is required. The technique can be used in combination with other integration approaches when necessary to enable even more complex structures to be built.

Nonplanar wafer bonding is not without its challenges. Like traditional wafer bonding and regrowth, it requires very clean surfaces in order to achieve high area yield bonds. It requires that the structures to be integrated be grown on the same wafer and hence be lattice matched to each other, though they can be integrated with lattice mismatched materials on the transfer wafer surface. These stacked epitaxial structures can, in some cases, lead to thick overall growths that may be challenging to realize. The lattice matched structures also must be separated by some type of layer that allows controlled etching to achieve smooth stepped surfaces prior to the wafer bonding step. These challenges will be discussed more in Chapter 5 when the processing of the structures is discussed.

Once the materials are laterally and vertically integrated on the transfer substrate, the geometry of the integrated regions imposed by nonplanar wafer bonding may not be well suited for all types of applications. As Figure 2.14 shows, at most only about 56% of the total surface is usable for active devices. For some applications this is more than sufficient. For WDM VCSEL arrays, only about 0.08% of the wafer surface requires active material (50 μm^2 active areas with devices on a 250-μm pitch), the rest of the surface is used for wire

bond pads, labels, and other features. In general arrays of structures, such as lasers, are well suited to the geometry of the nonplanar wafer bonding integration technique. The integration of electronic devices with photonic devices may also not be concerned with this loss of space to the bending regions because it can be used for thermal isolation and for routing transmission lines and other electrical interconnects.

One integration technique can not meet all the challenges for all applications and this fact applies to nonplanar wafer bonding as well. Nonplanar wafer bonding is not well suited for the realization of devices such as multicolor dense detector and light emitting device arrays because of the area loss. Also, for in-plane integration applications such as the combining of optimized laser epitaxial structures with optimized modulator structures, a method of optical interconnect between the regions is needed between the nonplanar wafer bonded regions. 3-D on-chip interconnection capabilities have been developed and could be applied to this integration platform but this certainly adds complexity and the drawbacks may outweigh the benefits.

The development of a suitable heterogeneous integration technique was a requirement for the fabrication of the wideband CWDM arrays of this thesis work. The next chapter will begin presenting the novel VCSEL design aspects of this work. Specifically a novel optically-pumped active region designed for uniform carrier injection into the quantum wells will be presented [15]. The

newly designed active-region structures will be integrated using nonplanar wafer bonding in Chapters 4 and 5 to fabricate record wavelength span long-wavelength WDM VCSEL arrays [16].

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Chapter 3

Active-Region Modeling and Design

In the pursuit of commercial quality VCSELs operating at 1310 and 1550 nm, optically-pumped VCSELs have been used not only as a development tools, but also in commercial products [1-3]. Reference 3 describes a technology developed by Gore Photonics, the company funding this research project, and was the approach selected for the CWDM VCSEL array technology developed in this thesis work. In Gore's approach, the optical pump laser is a GaAs-based short-wavelength VCSEL operating at 850 nm. The pump laser is grown in the same epitaxial stack as the top mirror of the long-wavelength VCSEL and hence, is automatically integrated with the long-wavelength VCSEL when the structure is assembled during wafer bonding. A schematic cross section of the structure and an angled top view scanning electron micrograph of the actual device are shown in Figure 3.1. The short-wavelength VCSEL is electrically

pumped and is processed above the long-wavelength VCSEL. The pump light emits downward and optically pumps the bottom VCSEL which can be designed to emit back up through the top VCSEL, or to emit down through the substrate. Two modal confinement structures layers exist; one for the top, short-wavelength VCSEL, and one for the bottom long-wavelength VCSEL. In both cases, the modal confinement structures is layer of AlAs partially oxidized to form a ring of lower index AlO_x, surrounding a central region of higher index AlAs material. Both modal confinement layers are automatically aligned to each other because both layers are accessed from the same deep-etched holes and oxidized in the same step [4].

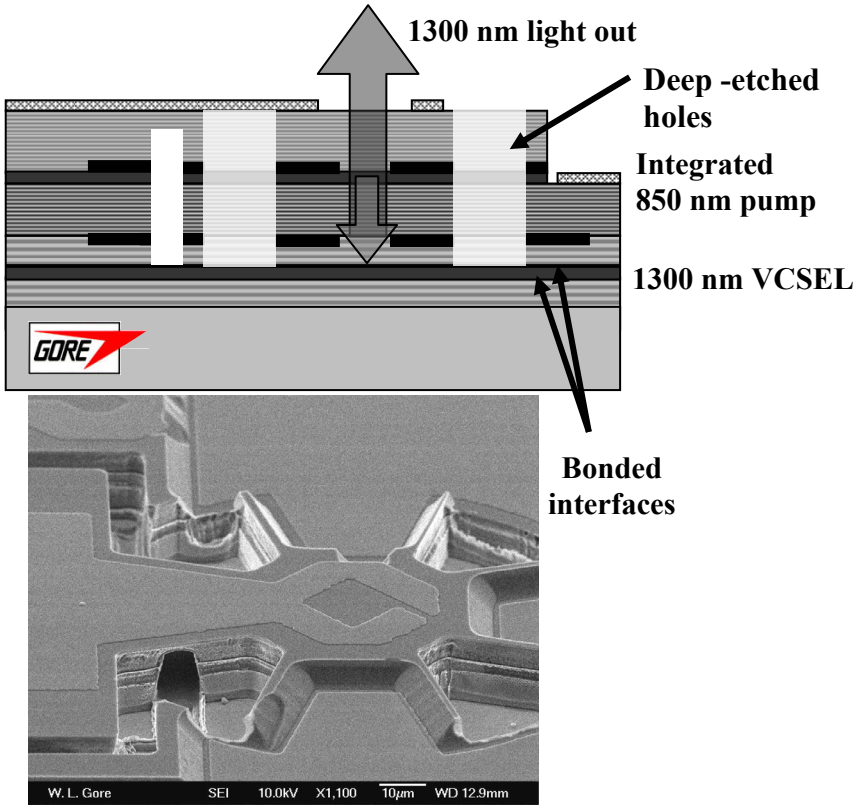

Figure 3.1. Schematic cross section of the Gore optically-pumped long-wavelength VCSEL structure and an angled top view scanning electron micrograph of the actual device.

In the design of optically-pumped active regions, it is desirable to make use of a long pump absorber region for high pumping efficiency. A long absorber is achieved by using the quantum-well barrier region as the absorber region. Carriers generated in the barrier diffuse to the quantum wells and provide gain for the lasing mode. Because no external bias is applied to an optically-pumped device, there is little driving force to distribute the carriers among clusters of wells. For this reason, research using optically-pumped active regions with long absorbers has made use of active-region designs with

periodically spaced single quantum wells, each positioned on a standing wave peak of the longitudinal field the VCSEL oscillator [5, 6]. These periodic-gain designs allow carriers, optically generated in long barrier regions, to diffuse directly to the nearest quantum well without passing over other wells.

Inherent in the periodic-gain design is the exponential decay of the pump beam throughout the length of the barrier. Because of the exponential decay in the carrier generation rate, the quantum wells are not uniformly populated and the first quantum well is pumped harder than the last well. Material gain does not increase linearly with quantum-well carrier density, so the first well produces less gain per carrier that the last well, resulting in a reduction in device efficiency and higher device thresholds and lower peak operating temperatures.

Because the ultra-wideband CWDM VCSEL array for this thesis work would be optically pumped, an improved optically-pumped active-region design has been developed and used for improved device performance [7]. Precisely placed carrier-blocking layers are incorporated to segment the absorber/barrier to control the diffusion of carriers to specific quantum wells. This improved Segmented-absorber Periodic-Gain (SAPG) active-region design results in high pump efficiencies while simultaneously achieving uniform filling of the periodically spaced quantum wells. A model for the carrier distribution in the traditional and new SAPG design is built and a design technique is presented. The quantum-well injection uniformity, C_{inj}, is defined as a metric to compare

the carrier uniformity in the quantum wells and is calculated for the new SAPG and traditional active-region designs. The results of this modeling and design work are then experimentally verified by building and comparing two optically-pumped 1540-nm VCSEL structures utilizing each active-region design.

3.1 VCSEL Active-Region Model

Figure 3.2 shows the conduction-band diagram for a traditional optically-pumped active-region structure and for the new SAPG active-region design concept. Both designs utilize a long barrier material designed to efficiently absorb the incident pump power. Figure 3.2 illustrates the decay of a 980-nm pump beam incident upon each active region for a barrier material of 1.22-Q InGaAsP with an 18000 cm^{-1} absorption coefficient. Between the wells of the new segmented-absorber design are larger band-gap InP carrier-blocking layers. The purpose of these layers is to segment the absorber and to corral the optically-generated carriers and force them to diffuse toward a specific quantum well. To determine the effect of these layers, the carrier distribution in the barriers and the carrier density in each quantum well are desired. By determining the carrier density in each quantum well for different optical-pumping conditions, the gain available from the traditional and new SAPG design can be compared and the laser threshold for both designs can be

predicted. Knowledge of the carrier density in each quantum well allows for the calculation of the quantum-well injection uniformity, C_{inj}, for each design.

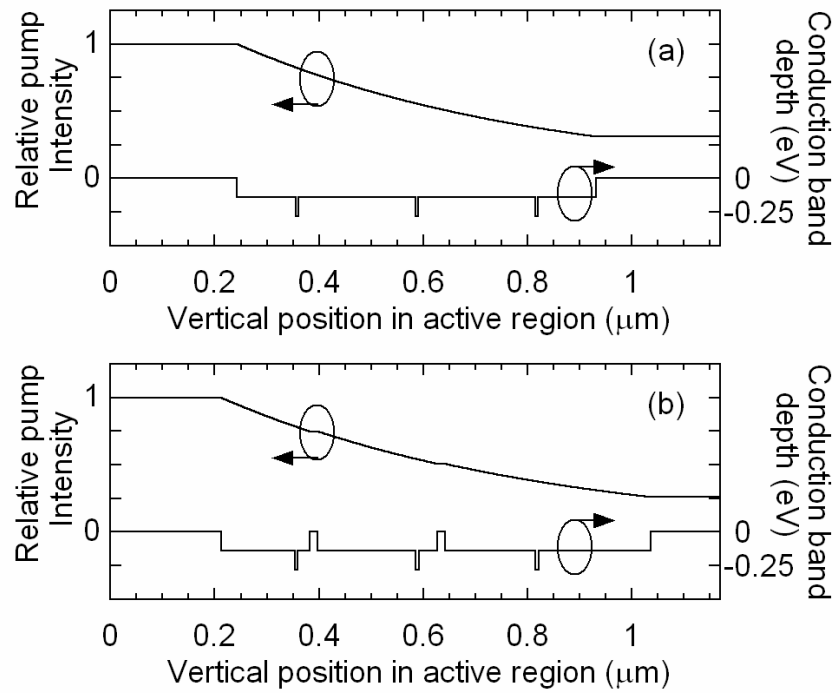

Figure 3.2. Conduction band diagram and pump attenuation in traditional (a) and segmented-absorber (b) periodic-gain optically-pumped active- region designs.

The one-dimensional carrier diffusion equation is used to solve for the carrier distribution in both types of VCSEL active regions. To solve for the carrier distribution in all regions and all the quantum wells requires the numerical solution of a system of equations under steady-state conditions. The problem is bounded by assuming there is no carrier flow over the InP layers in either active-region design and by assuming the carrier density in the barrier is continuous across the thin quantum-well layer.

The steady-state carrier balance in the quantum well is given by:

$$(3.1)\ \frac{dn_{wi}}{dt} = \frac{n_{bi}}{\tau_c} - \frac{n_{wi}}{\tau_e} - \left(An_{wi} + Bn_{wi}^2 + Cn_{wi}^3\right) = 0$$

The steady-state carrier balance in the continuous states above the quantum well is given by:

$$(3.2)\ \frac{dn_{bi}}{dt} = \frac{1}{t_{wi}}\left(J_{wi}^- - J_{wi}^+\right) - \frac{n_{bi}}{\tau_c} + \frac{n_{wi}}{\tau_e} = 0$$

where n_{bi} is the carrier density in the continuous states above the i^{th} quantum well, n_{wi} is the carrier density in the i^{th} quantum well of t_{wi} thickness, τ_c is the capture time of carriers from the barrier into the quantum well, τ_e is the thermal emission time of carriers out of the quantum well into the barrier. A, B, and C represent the defect, bimolecular, and Auger recombination coefficients, and J_{wi}^+ and J_{wi}^- represent the carrier flux density into the continuous states above the quantum well from the left and right side. Multiple wells at each quantum well region can be treated by modifying t_{wi} to be the cumulative thickness of all the quantum wells in the region.

In the barrier regions of the active region, the carrier distribution is determined by the solution to the diffusion equation:

$$(3.3)\ D_a \frac{d^2 n}{dx^2} - \frac{n}{\tau} + G = 0$$

where the general form for the generation rate is given by:

$$G' = G_0' e^{-\alpha x'}$$

and

$$G_0' = \frac{P_{in}}{h\nu} \frac{\alpha}{\pi r'^2}$$

Here n is the carrier density in the barrier, D_a is the ambipolar diffusion coefficient in the barrier, τ is the ambipolar carrier lifetime in the barrier, α is the pump absorption coefficient, and P_{in} is the pump power incident on the active region at frequency ν and with a spot radius of r. The origin of the coordinate x' is located at the beginning of the active-region barrier; hence it is shifted back from x by a length equal to the position of the barrier starting position. This must be accounted for in the final solution if this length is not zero (as is usually the case).

The general solution to Equation 3.3 is given by:

$$(4)\; n(x) = C\sinh\left(\frac{x}{L_a}\right) + C'\cosh\left(\frac{x}{L_a}\right) + n_G e^{-\alpha x}$$

with the general form for n_G given by

$$n_G' = \frac{G_0'\tau}{1-(\alpha L_a)^2}$$

and the ambipolar diffusion length is

$$L_a = \sqrt{D_a\tau}$$

To solve for the carrier distribution in the active region and the carrier densities in the quantum wells, a system of equations is built in terms of the unknown values of J_{wi}^{+} and J_{wi}^{-} and n_{bi} necessary to solve for n_{wi}, the carrier density in the quantum wells. The coupling of J_{wi}, n_{bi}, and n_{wi} in Equations 3.1 and 3.2 requires a numerical solution for the final determination of the quantum-well carrier densities. For the traditional periodic-gain design, all the regions are interdependent and are solved simultaneously. For the new SAPG design, each quantum-well region is separated from the other quantum-well regions by carrier-blocking layers. This separation allows each region to be solved independent of the other regions.

By applying the boundary conditions in the active regions, two types of solutions are attained. The first type is for a region bounded on one side by an InP barrier with no current flow over the barrier and bounded on the other side by a quantum well. This equation type is all that is needed to describe the segmented-absorber periodic-gain design with InP carrier-blocking layers between each well as shown in Figure 3.2(b). The second type of equation is needed to fully describe the carrier distribution in the regions between the quantum wells of the traditional periodic-gain design of Figure 3.2(a). This second type is bounded on both sides by quantum wells. In both solution types, the general solution in Equation 3.4 is rewritten by expressing the constants C and C' in terms of the desired unknown variables J_{wi}^{+} and J_{wi}^{-} and n_{bi} by using the relations $J_{wi}=-D_a(dn/dx)$ and $n=n_{bi}$ at the quantum-well position $x=X_i$.

The development of the first equation type is explored by looking at the first region to the left of the leftmost quantum well in Figure 3.2(a). Here the InP blocking layer is at position $x=X_a$ and the quantum well is at position $x=X_1$. The boundary condition at the InP blocking layer is $dn/dx=0$ because it is assumed that no current flows over the InP carrier-blocking layers. This boundary condition has been applied to yield:

$$n_{b1}\sinh\left(\frac{W_0}{L_a}\right)+J_{w1}^{-}\frac{L_a}{D_a}\cosh\left(\frac{W_0}{L_a}\right)=$$
$$n_G\left\{e^{-\alpha X_1}\left(\alpha L_a\cosh\left(\frac{W_0}{L_a}\right)+\sinh\left(\frac{W_0}{L_a}\right)\right)-\alpha L_a e^{-\alpha X_a}\right\}$$

here $W_0=X_1-X_a$ and

$$n_G=n_G^{'}e^{\alpha X_a}$$

The second equation type arises from applying the boundary conditions to the region located between the leftmost quantum well and center quantum well in Figure 3.2(a). The quantum well on the left of this region is at position $x=X_1$ and the right well is at position $x=X_2$. The boundary conditions at the right well are $n=n_{b2}$ and $J_{w2}=-D_a(dn/dx)$ and have been applied to attain Equations 3.5 and 3.6. $W_1=X_2-X_1$ has been defined.

$$(3.5)\ -n_{b1}\cosh\left(\frac{W_1}{L_a}\right)+n_{b2}+J_{w1}^{+}\frac{L_a}{D_a}\sinh\left(\frac{W_1}{L_a}\right)=$$
$$n_G\left\{e^{-\alpha X_1}\left(\alpha L_a\sinh\left(\frac{W_1}{L_a}\right)-\cosh\left(\frac{W_1}{L_a}\right)\right)+e^{-\alpha X_2}\right\}$$

$$(3.6)\ -n_{b1}\sinh\left(\frac{W_1}{L_a}\right)+J_{w1}^{+}\frac{L_a}{D_a}\cosh\left(\frac{W_1}{L_a}\right)-J_{w2}^{-}\frac{L_a}{D_a}=$$

$$n_G\left\{e^{-\alpha X_1}\left(\alpha L_a\cosh\left(\frac{W_1}{L_a}\right)-\sinh\left(\frac{W_1}{L_a}\right)\right)-\alpha L_a e^{-\alpha X_2}\right\}$$

Similar equations can be built by applying similar boundary conditions for the other regions of the optically-pumped active-region designs shown in Figure 3.2. Using these equations, along with Equation 3.2 and Equation 3.1 for each quantum well, a system of equations can be built and solved numerically for each quantum well. From this solution, the unknown quantities J_{wi}^{+} and J_{wi}^{-}, n_{bi}, and the quantum-well carrier density n_{wi} can be determined. Together, the quantities J_{wi}^{+} and J_{wi}^{-}, n_{bi} determine the coefficients C and C' of Equation 3.4 which describe the complete carrier distribution in the barrier regions.

Once the carrier density in each quantum well is know for each design, the available material gain from each well is determined via a numerical free-carrier gain model including band-gap renormalization, as implemented in PICS3D by Crosslight Software, Inc. These numerical calculations were performed by Professor Joachim Piprek at UCSB. The effect the new carrier-blocking layers have on the overall performance of the active region have been compared. Prior to completing the model however, the specific structure of the active-region design must be specified. This is accomplished by a design optimization approach.

3.2 VCSEL Active-Region Design

By using carrier-blocking layers positioned between the quantum well regions to segment the absorber, it is possible to compensate for the exponential decay of the carrier generation rate along the vertical length of the active region. In order to attain uniform carrier density in each quantum well of the periodic-gain structure, it is necessary to position the carrier-blocking layers in a manner that allows an equal number of carriers to diffuse into each well. To accomplish this goal, an iterative optimization approach has been utilized in the design of the active region. This approach allows for the simultaneous maximization of the amount of pump power absorbed while maintaining uniform carrier densities in each well. This approach has been generalized to allow for multiple quantum wells at each standing wave peak in the periodic-gain structure.

Figure 3.3 shows a schematic representation of the new SAPG VCSEL active-region design. The total length of the active region is 5/2 wavelengths in the material. Three quantum wells (or groups of quantum wells) are located on the middle three standing wave peaks in the cavity. A region on either side of the cavity, along the interface with the top and bottom distributed Bragg reflector (DBR), is reserved for superlattice structures that are used in the final wafer-bonded VCSEL for wavelength control and growth-rate error adjustment. The barrier material is designed to absorb the pump beam while the InP carrier-

blocking layers, located on either side of each quantum well, are transparent at the pump wavelength. The position of the carrier-blocking layers can be adjusted anywhere in the range between the quantum wells or between a quantum well and the area reserved for the superlattice regions. Minimum setback distances are used between the center of the carrier-blocking layer and the center of the quantum wells and between the edge of the carrier-blocking layers and the superlattice region on each side of the active region.

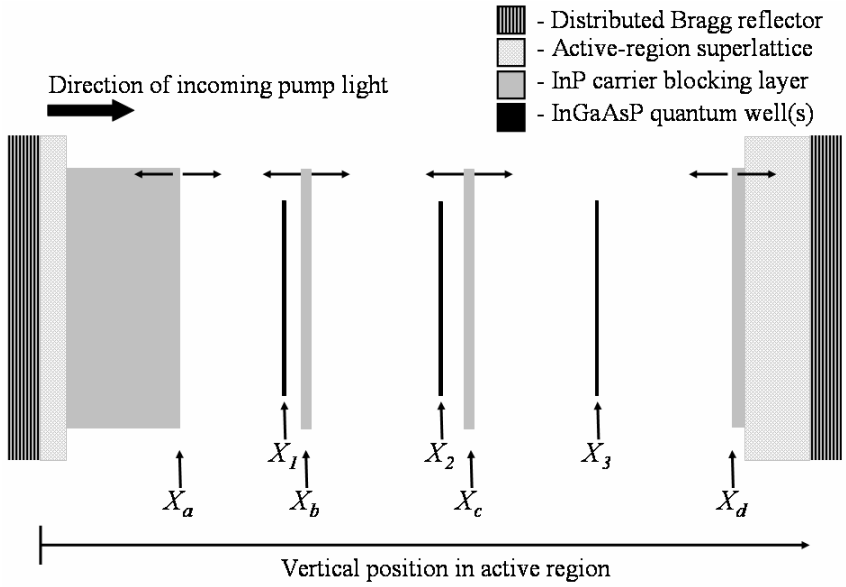

Figure 3.3. Schematic representation of the new SAPG VCSEL active-region design.

The design objective is to maximize the total absorber length while achieving an equal number of optically-generated carriers in each region. Accounting for the transparent carrier-blocking layers of thickness t_b located between each well, the pump power in the absorbing barrier regions along the horizontal axis of the active region in Figure 3.3 and shown in Figure 3.2(b) is

given by:

$$P(x)=\begin{cases} P_{in}e^{-\alpha(x-X_a)} & X_a \le x \le X_b - \dfrac{t_b}{2} \\ P_{in}e^{-\alpha(x-X_a-t_b)} & X_b + \dfrac{t_b}{2} \le x \le X_c - \dfrac{t_b}{2} \\ P_{in}e^{-\alpha(x-X_a-2t_b)} & X_c + \dfrac{t_b}{2} \le x \le X_d \end{cases}$$

Pump power reflection at the interfaces have been neglected. Given this pump power distribution, in order for each barrier region to have an equal number of optically-generated carriers the following condition must be true:

$$(3.7)\ \frac{1}{m_1}\int_0^{X_b-X_a-t_b/2} e^{-\alpha u}du = \frac{1}{m_2}\int_{X_b-X_a-t_b/2}^{X_c-X_a-3t_b/2} e^{-\alpha u}du = \frac{1}{m_3}\int_{X_c-X_a-3t_b/2}^{X_d-X_a-2t_b} e^{-\alpha u}du$$

where m_1, m_2, and m_3 are the number of quantum wells at each periodic position. From this relation X_c and X_d are expressed as:

$$X_c = -\frac{1}{\alpha}\ln\left[\left(1+\frac{m_2}{m_1}\right)e^{-\alpha\left(X_b-X_a-t_b/2\right)} - \frac{m_2}{m_1}\right] + X_a + \frac{3t_b}{2}$$

$$X_d = -\frac{1}{\alpha}\ln\left[\left(1+\frac{m_3}{m_2}\right)e^{-\alpha\left(X_c-X_a-3t_b/2\right)} - \frac{m_3}{m_2}e^{-\alpha\left(X_b-X_a-t_b/2\right)}\right] + X_a + 2t_b$$

Thus by selecting the appropriate X_a and X_b, the ideal solution that allows for the greatest pump power absorption while equalizing the number of

carriers generated in each region for each quantum well can be determined. In practice this is done by an iterative maximization of the difference between X_d and X_a while satisfying Equation 3.7 and not violating any of the defined carrier-blocking layer setback requirements. The actual problem is solved in relative units in terms of fractional wavelengths inside the material.

For the optically-pumped VCSEL designed in this thesis work [8], a 980-nm laser is used as the optical pump source and the photoluminescence peaks of the quantum wells have been chosen to be at 1520 nm. The barrier and pump absorber used is 1.22-Q InGaAsP because it has a high absorption coefficient, measured to be 18000 cm^{-1} at 980 nm, and provides a conduction band depth of 80 meV for electron confinement. In addition, the group III composition used in the 1.22-Q barrier is identical to that used in the quantum wells, facilitating the growth of high-quality wells. The active region is designed for use in a WDM array and hence has several superlattice periods on each side. This results in a front side (left side in Figure 3.3) setback of 40 nm and a backside setback of 135 nm. Single quantum wells are used at each standing-wave peak, hence $m_1=m_2=m_3=1$. The average index of the barrier material is calculated to be 3.35 at the lasing wavelength of 1540 nm and the quantum wells are positioned at wavelength units of 0.75, 1.25, and 1.75. The minimum gap allowed between the center of the two central 15-nm thick carrier-blocking layers and the center of the 5-nm thick quantum wells is 25 nm.

Based on the design parameter requirements and the design optimization approach presented here, the new SAPG active-region parameters shown in Table 3.1 have been calculated. This design gives a total expected absorption of about 74 %.

Total active-region length	1171.6 nm
X_a	212.1 nm
X_b	382.1 nm
X_c	627.7 nm
X_d	1036.6 nm
X_1	357.1 nm
X_2	588.7 nm
X_3	818.6 nm

Table 3.1. New SAPG active-region design epitaxial-layer boundary positions.

For comparison purposes, Table 3.2 shows a traditional periodic-gain structure with symmetric absorbers. This design gives a total expected absorption of about 69 %.

Total active-region length	1174.7 nm
Front Cladding	243.0 nm
Well 1	357.8 nm
Well 2	587.4 nm
Well 3	817.0 nm
Back Cladding	931.7 nm

Table 3.2. Traditional absorber design epitaxial-layer boundary positions.

3.3 VCSEL Active-Region Modeling Results

The specific traditional and new SAPG active-region designs shown in Tables 3.1 and 3.2 can be directly compared using the carrier diffusion model

developed. Additional parameters used in the model are shown in Table 3.3. R_{top}, R_{bottom}, Γ_{enh}, L_m, and g_{th} are calculated using well known techniques.

T	Temperature	293 K
τ	Ambipolar carrier lifetime in barriers	7.9 ns [9]
D_a	Ambipolar diffusion coefficient	7.4 cm^2/sec [9]
τ_c	Net quantum-well capture time	0.25 ps [10]
A	Defect recombination (fit parameter)	3 ns^{-1}
B	Bimolecular recombination	$0.3 \cdot 10^{-10}$ cm^3/sec [11]
C	Auger recombination	$6 \cdot 10^{-29}$ cm^6/sec [11]
R	980-nm pump radius	2.5 μm
α_i	VCSEL internal loss (fit parameter)	10 cm^{-1}
R_{top}, R_{bottom}	VCSEL mirror reflectivity (GaAs/AlAs)	0.99914, 0.999966
Γ_{enh}	Traditional design gain enhancement factor	1.95381
Γ_{enh}	New design gain enhancement factor	1.92539
L_m	Mirror penetration depth	0.755 μm
g_{th}	Traditional design average threshold material gain	1069 cm^{-1}
g_{th}	New design average threshold material gain	1083 cm^{-1}

Table 3.3.Parameters used in model calculations.

The recombination coefficient A and the internal loss α_i are used as fit parameters in the final model calculations to match the measured threshold of the VCSEL device fabricated using the new SAPG active region. The recombination parameter includes carrier loss due to radial carrier diffusion and defect recombination and results in a larger than expected recombination parameter [12]. The internal-loss value chosen is consistent with values typically used in VCSELs.

Using the parameters in Table 3.3 and the specific active-region geometries given in Tables 3.1 and 3.2 the carrier distribution in both active-region designs has been calculated by applying the model. Figures 3.4 and 3.5

show the results of these calculations. For comparison purposes, data is shown at the pump power input level necessary for equal total absorbed power in both designs. The absorbed pump power level corresponds to 0.5 mW, the level necessary to reach threshold in the VCSEL based on the new SAPG active-region design. Based on the expected absorption efficiencies of the two different designs, 0.5 mW of absorbed power corresponds to an input pump power of 0.68 mW for the SAPG active-region design and 0.76 mW for the traditional periodic-gain active-region design.

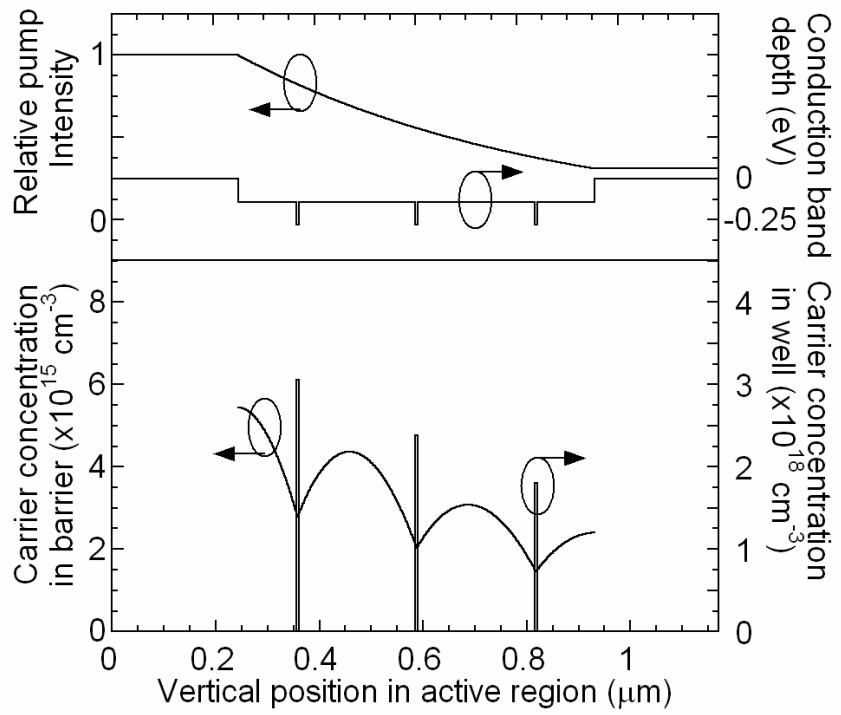

Figure 3.4. Predicted carrier distribution in barrier and quantum-well carrier density in the traditional periodic-gain optically-pumped active-region design.

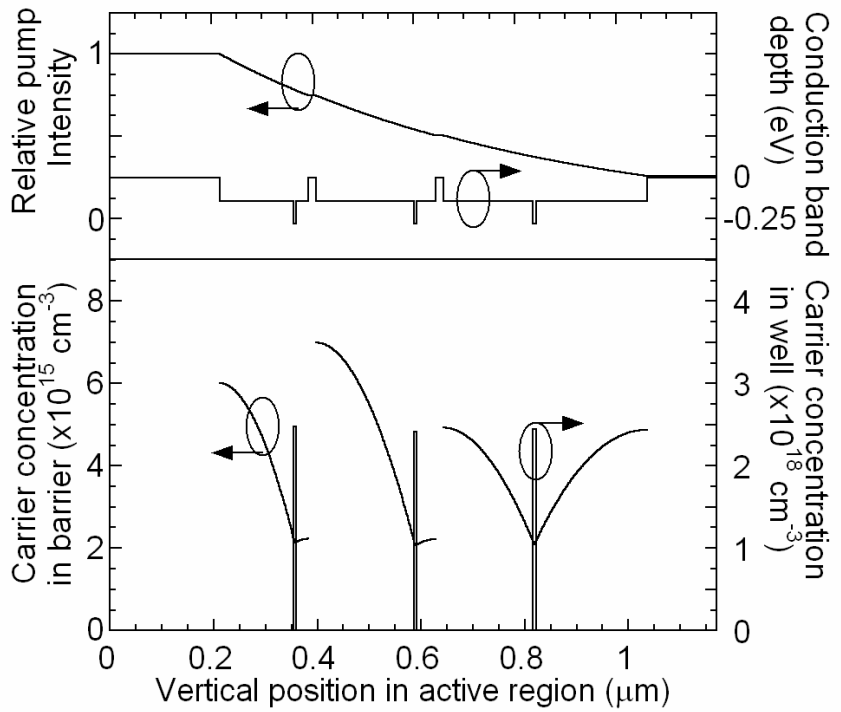

Figure 3.5. Predicted carrier distribution in barrier and quantum-well carrier density in the new SAPG optically-pumped active-region design.

The model calculations predict more uniform carrier filling of the wells in the SAPG design as is evident from a comparison of Figures 3.4 and 3.5. This uniformity translates into more uniform gain from each well of the new design as shown in Figure 3.6. The figure also shows all quantum wells of the traditional design have not yet reached transparency. Due to gain saturation effects and limitations on the highest carrier density that can be achieved in a quantum well, this carrier non-uniformity will result in higher device thresholds and less efficient device operation. The model predicts a modest 4.9 % improvement in threshold with the new design.

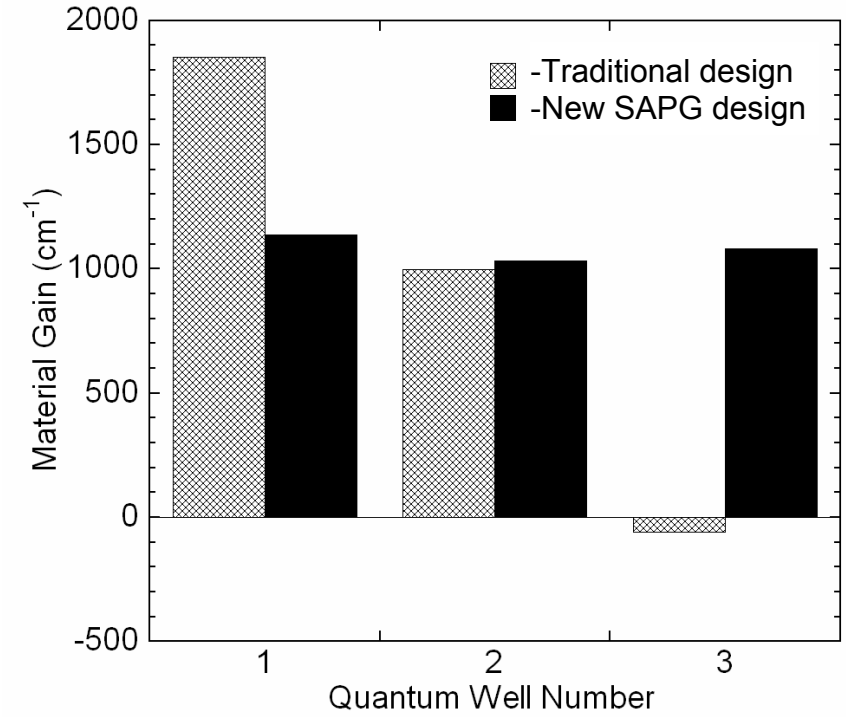

Figure 3.6. Predicted quantum-well gain in the traditional and new SAPG active-region designs. Data shown is calculated at the new design's threshold absorbed pump power of 0.5 mW.

Based on the carrier density in each quantum well, it is possible to quantify the quantum-well injection uniformity, C_{inj}, in each device. C_{inj} is defined as the ratio of the standard deviation to the mean of the carrier density in the quantum wells, $C_{inj}=\sigma/\mu$. It is desirable to minimize C_{inj} in an active-region design to most efficiently generate gain from the available carriers. C_{inj} is 0.0113 and 0.212 in the new SAPG and the traditional periodic-gain designs respectively.

3.4 Experimental Results

In order to validate the design and the model, two optically-pumped VCSEL structures were fabricated. Both active-regions used the layer designs of Table 3.1 and 3.2 with three 5-nm wide 1% compressively strained InGaAsP quantum wells. The photoluminescence peaks were identical in both wafers and were located at 1520 nm. The optically-pumped VCSEL devices were fabricated by direct wafer bonding a 40-period GaAs/AlAs bottom DBR and a 24.5-period GaAs/AlAs top DBR. The mirrors have the calculated reflectivity values given in Table 3.3. The top mirror reflectivity includes an in-phase semiconductor-air interface reflection. The device was optically pumped from the bottom with 980-nm laser emission focused to a 5-μm spot. The completed VCSELs emitted single-mode at 1540 nm. Light-out vs. light-in results over temperature are shown in Figure 3.7. For the purposes of accurate comparison, the approximate amount of power actually absorbed in each active-region design has been estimated from measurements and is plotted along the abscissa of Figure 3.7. Multiple devices were tested from two process runs and the data shown here is from devices representative of the both sets of samples.

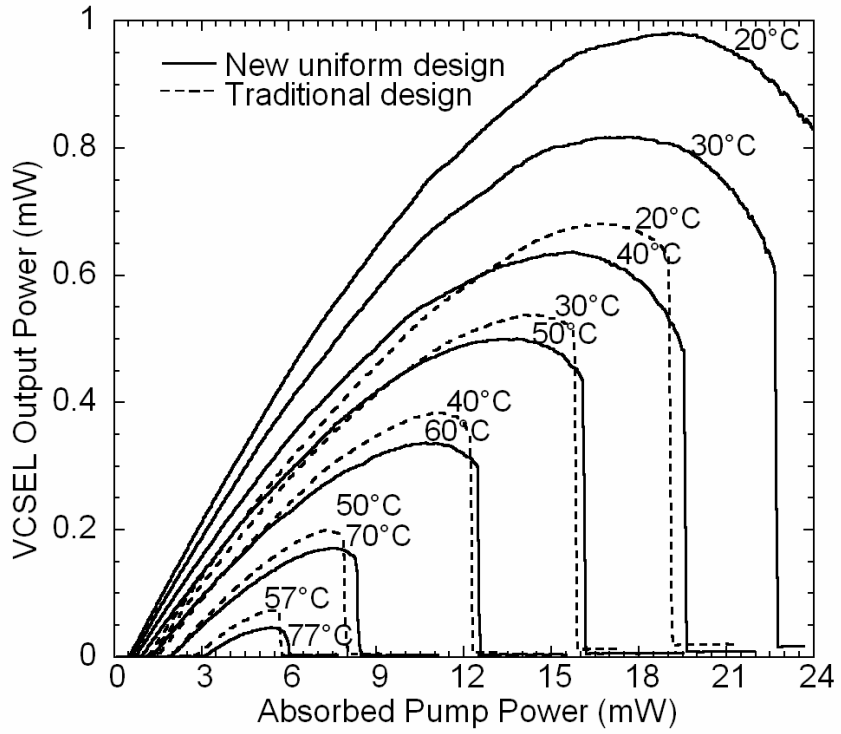

Figure 3.7. Light-out verses absorbed light-in over temperature for VCSEL structures using both the traditional and new segmented-absorber periodic-gain active-region designs.

The absorption efficiencies of the tested VCSELs based on the new and traditional active-region designs were calculated to be 84 % and 78 %. These values are calculated based on measurements made of the pump incident on the sample and passing through the sample and by accounting for the air-semiconductor reflections on the top and bottom of the sample (See Section 6.1.2 for more details). Measurements made on similarly prepared samples with no VCSEL epitaxial structures have shown a scattering loss of up to 10% off the back of the manually polished substrate upon which the pump beam is incident. By neglecting this backside scattering loss, all interface reflections inside the

VCSEL, and any pump absorption in the superlattice, the 84 % and 78 % pump efficiency values calculated from the tested devices overestimate the actual values which are likely closer to the ideal expected values of 74 % and 69 %.

Figure 3.8 shows the threshold variation with temperature for both VCSEL designs. The SAPG design has a room temperature threshold of 0.49 mW while the traditional design has a 1.2 mW threshold. This represents a threshold improvement of over 50 % with the new design. Figure 3.9 shows the peak output power over temperature for both designs. The SAPG design shows a 20-°C improvement in peak operating temperature and continues to operate up to 77 °C. Both designs have the same thermal impedance of 0.89 °C/mW and nearly identical operating wavelengths and PL wavelengths. Because great care was taken to ensure all other parameters were equal, these VCSEL improvements are attributed to the improved carrier uniformity achieved with the new segmented-absorber periodic-gain active-region design.

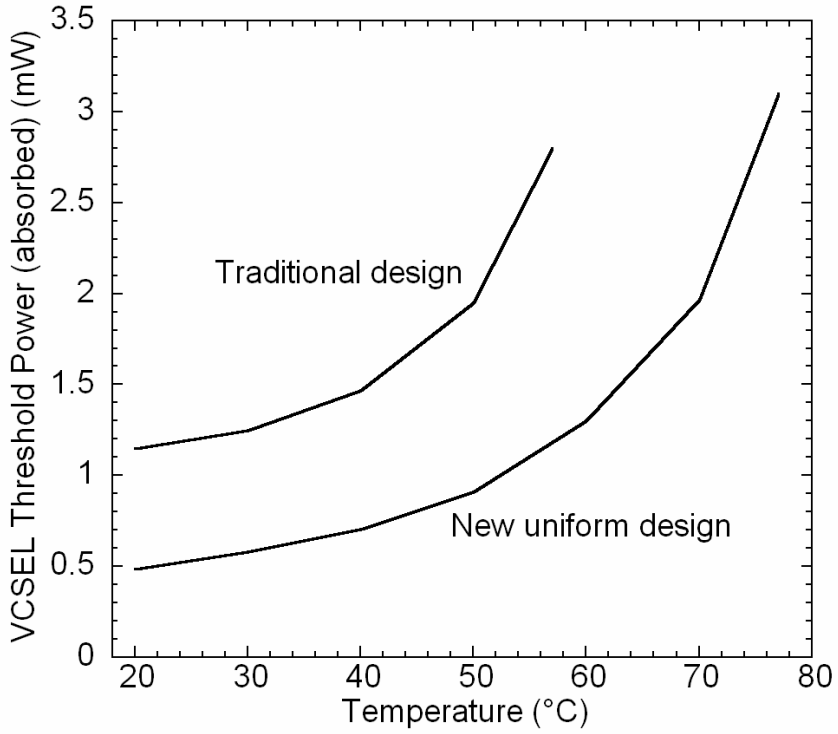

Figure 3.8. Measured VCSEL thresholds over temperature for VCSEL structures using both the traditional and new SAPG active-region designs.

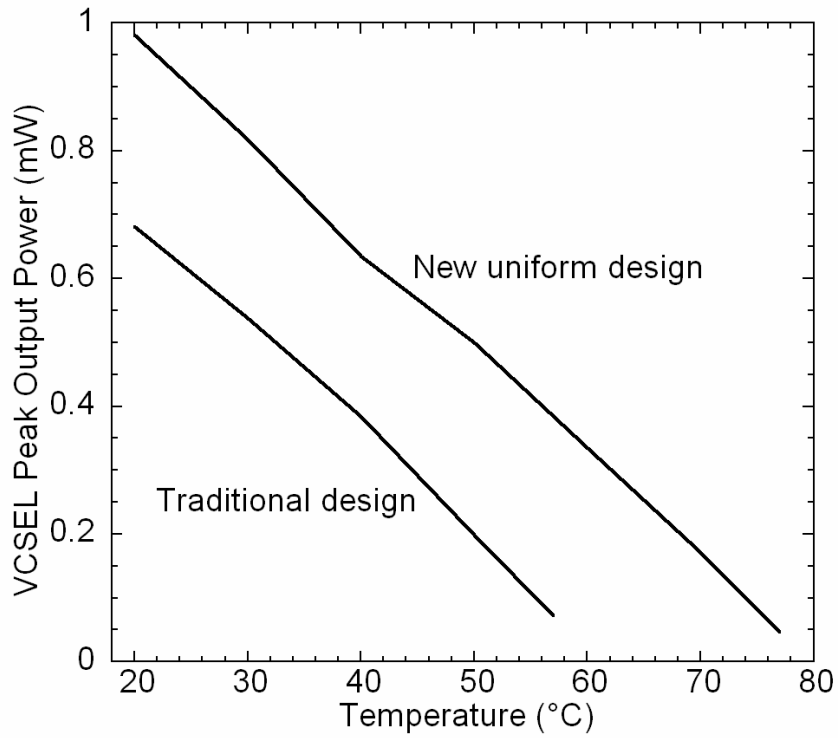

Figure 3.9. Measured VCSEL peak output power over temperature for VCSEL structures using both the traditional and new SAPG active-region designs.

3.5 Summary and Discussion

An active region designed specifically for efficient optical pumping was developed, modeled, and tested. This new improved design developed here will be used in the fabrication of the CWDM VCSEL arrays presented in Chapters 4-6. The design makes use of a long pump-absorber region for efficient pump absorption, and precisely placed carrier-blocking layers to segment the absorber and promote uniform carrier filling of the quantum wells. The model describes the carrier distribution in the active region and predicts the carrier density in each quantum well. To facilitate designing optically-pumped active regions, a

simple design method was developed. The new design approach was used to design a 5/2-wavelengths thick periodic-gain VCSEL active region with one quantum well on each of the three central standing wave peaks of the cavity. The model shows that pump efficiencies of 74% can be achieved while simultaneously filling each of the quantum wells with a uniform number of carriers. To quantitatively compare the new design to the traditional design, the quantum-well injection uniformity parameter, C_{inj}, was introduced as the ratio of the standard deviation to the mean value of the carrier density in the different quantum wells of the active region. This parameter has been calculated for the new and traditional designs and found to be 0.0113 and 0.212 respectively. Experimental results verify that the new design improves the threshold by over 50 % and the peak operating temperature by 20 °C.

The results of the model and the experiment shown the same trend toward improved thresholds with the new design, but do not agree well quantitatively. This discrepancy is due to a combination of the simplistic nature of the diffusion model used, and the lack of precision in the gain model. By improving the uniformity of the carrier population in each well, the new design avoids the gain saturation effects that can occur in quantum wells. An error in the differential gain of the gain model will translate into a change in the predicted improvement with the new design. It is postulated that the gain model used overestimates the amount of gain generated in the first well shown in

Figure 3.6. Regardless of their quantitative differences, both the experiment and the model demonstrate the improved performance of the new segmented-absorber periodic-gain active-region design.

References

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Chapter 4

Ultra-Wideband WDM Array Design

In Chapters 2 and 3 the separate tools of nonplanar wafer bonding integration and optically-pumped active-region design were developed. In this chapter these tools are combined along with others to develop a complete chip design that meets the CWDM VCSEL array requirements. This integrated chip for CWDM applications is just one of many anticipated applications for nonplanar wafer bonding and was chosen based on the industry need for such a component and to leverage the WDM VCSEL device design and fabrication skills available. By using nonplanar wafer bonding to fabricate record wavelength span VCSEL arrays, the validity of the approach as an integration technique can be demonstrated.

The final design goal is a 2-D CWDM VCSEL array with eight wavelength channels. These channels should match the industry standard ITU

CWDM grid (ITU-T G.694.2, 12-03) over the most commonly used wavelength range from about 1470 to 1610 nm [1]. The wavelength spacing of the array channels is 20 nm. It was the goal of this research to demonstrate single transverse mode lasing from all eight channels from room temperature to 70°C. A 2-D array was chosen to differentiate the VCSEL approach from the edge-emitting laser approaches but a device spacing of 250 μm was still desirable for future fiber coupling with standard arrayed fibers. Highly uniform lasing thresholds, differential efficiencies, and output powers are desirable, and the approach selected for this work is generally capable of meeting these requirements. In real industry grade products, the relevant modulation properties of relative intensity noise and modulation bandwidth would also be specified. Modulation properties where not investigated for this work; the focus was on attaining high-quality 'DC' properties.

The CWDM array design covers a 140 nm wavelength span. This wide span requires the use of at least two active regions to support lasing in the different wavelength channels of the array. Thus nonplanar wafer bonding will be used to integrate the required InP-based active regions onto the bottom AlGaAs-based mirror material. Each integrated active region can still be used to support multiple wavelength channels in the array. To maintain uniform device properties across the array, the wavelength span covered by each active region is intentionally limited. In order to create multiple wavelengths on each active

region with the proper wavelength separation, a previously developed superlattice etching technique will be used to trim the laser resonant cavity length along different positions in the array [2-4]. A similar technique will be used to tune the overall active-region lengths to account for any growth-rate errors that would force all the lasing wavelengths off their targets [5].

Because the nonplanar wafer bonding approach utilizes the same mirror for each wavelength channel in the array, the broad wavelength span of the array precludes the use of standard quarter wavelength GaAs/AlAs distributed Bragg reflector (DBR) mirrors. These standard mirrors are only practical for VCSEL arrays spanning less than 70 nm. For wider wavelength span arrays, a wider wavelength span mirror is needed. The natural candidate is one that is compatible with the nonplanar wafer bonding integration platform in its presently developed form. The mirrors selected were fully-oxidized GaAs/AlO_x DBRs that have been previously developed [6, 7] and demonstrated with short-wavelength VCSELs [7-9].

This chapter will discuss the development of each section of the VCSEL design and will tie the sections together by presenting a general design roadmap and the final array geometry. The specifics of the processing will be reserved for Chapter 5 and Appendixes A and B. Here the development of the fully-oxidized DBRs will be presented along with experimental results guiding the proper integration of these mirrors with long-wavelength VCSELs. The

epitaxial structure of the two active regions that will be used for the CWDM array will be described and a method for modal confinement in the optically-pumped structure will be given.

The simulation program used extensively in this chapter is Vertical, written by Frank Peters originally for USCB and then updated for Gore Photonics. This program was used to generate all the simulated data shown in this chapter.

4.1 Design of Fully-Oxidized Mirrors for Broad-Band Reflectivity

In order to operate properly, each VCSEL wavelength channel in the CWDM array must have adequate mirror reflectivity. Traditional AlGaAs DBRs for VCSELs use quarter wavelength thick alternating layers of AlAs and GaAs as their mirrors. The index contrast between these two materials is about 0.49 and reflectivity levels of 99% can be achieved with as few as 20 mirror periods (40 layers). Figure 4.1 shows a typical mirror reflectivity from a 20-period GaAs/AlAs DBR clad on both sides with GaAs. Unfortunately, even with the relatively large index contrast between these two materials, the total reflectivity stop band width (defined as distance between large dips to either side of reflectivity peak) is only about 200 nm. Because the reflectivity is not flat

across the stop band, the usable wavelength range can be defined as the range over which the absolute reflectivity varies by 0.5%. This definition, though somewhat arbitrary, gives an estimate of the range over which the mirror provides a fairly consistent feedback level for laser oscillation. For the traditional 20-period AlAs/GaAs DBR shown in Figure 4.1, this usable wavelength span is about 70 nm.

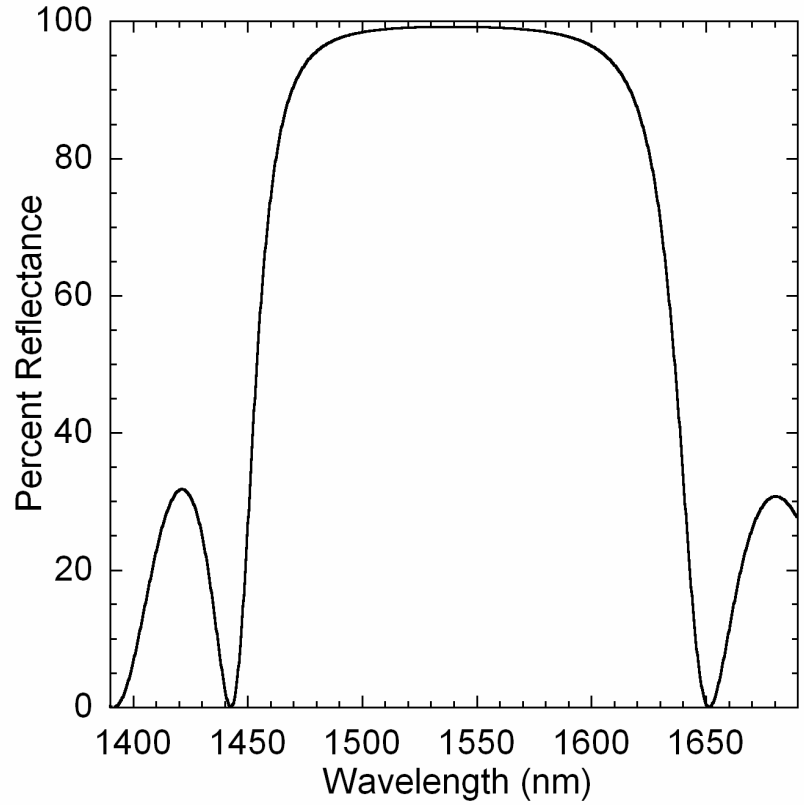

Figure 4.1. Simulated reflectivity spectrum of a 20-period GaAs/AlAs DBR clad with GaAs.

For a wide wavelength span CWDM VCSEL array, a mirror with a considerably wider reflectivity stop band and a usable wavelength span in

excess of 140 nm is needed. Wide stop band mirrors can be generated by increasing the index contrast of the quarter wavelength thick layers of the DBR. One popular way to do this is to use vacuum deposited dielectric coatings for the mirror periods. Unfortunately, the CWDM VCSEL array requires highly reflective mirrors on both sides of the active region and this presents challenges in fabricating these devices with deposited dielectric mirrors.

In addition to providing the required reflectivity across the 140 nm wavelength span of the WDM array, a highly reflective DBR with a wide stop band will have the advantage of a nearly flat and linear phase response across the usable region of the mirror. A linear phase response simplifies the design of the WDM array by causing identical incremental changes in cavity length of the active region to correspond to nearly identical shifts in lasing wavelength, regardless of the absolute lasing wavelength. Thus, all wavelength tuning layers in the active-region superlattice can be the same thickness regardless of the position of the selected wavelengths with respect to the mirror center. This wavelength tuning superlattice is described in the next section. The flatness of the phase response allows smaller changes in cavity thickness to have a larger impact on the oscillation wavelength of the VCSEL thereby making the multi-wavelength array easier to tune.

4.1.1 The Fully-Oxidized DBR Approach

An alternative strategy to the use of deposited dielectric DBRs for achieving wide reflectivity stop bands is to take advantage of the native oxide in the GaAs material system. This native oxide is AlO_x, and results from the wet thermal oxidation of AlAs [10]. During this process, the index of the AlAs converts from 2.89 to about 1.5 Thus, it is possible to increase the index contrast in the layers of a GaAs/AlAs DBR from 0.49 to greater than 1.8 by converting the AlAs to AlO_x [6, 7].

Figure 4.2 shows a simulated reflectivity spectrum of a four-period GaAs/AlO_x DBR of the design that will be developed later in this section. The mirror is simulated clad on both sides with GaAs to eliminate the influence of air-interface reflections. From the simulation, it is evident that the stop band width is about 1200 nm and the usable wavelength span is about 350 nm. This mirror is five times wider than traditional DBRs of the same peak reflectivity (99%) and is well suited for use in wafer bonded, optically-pumped CWDM VCSEL arrays.

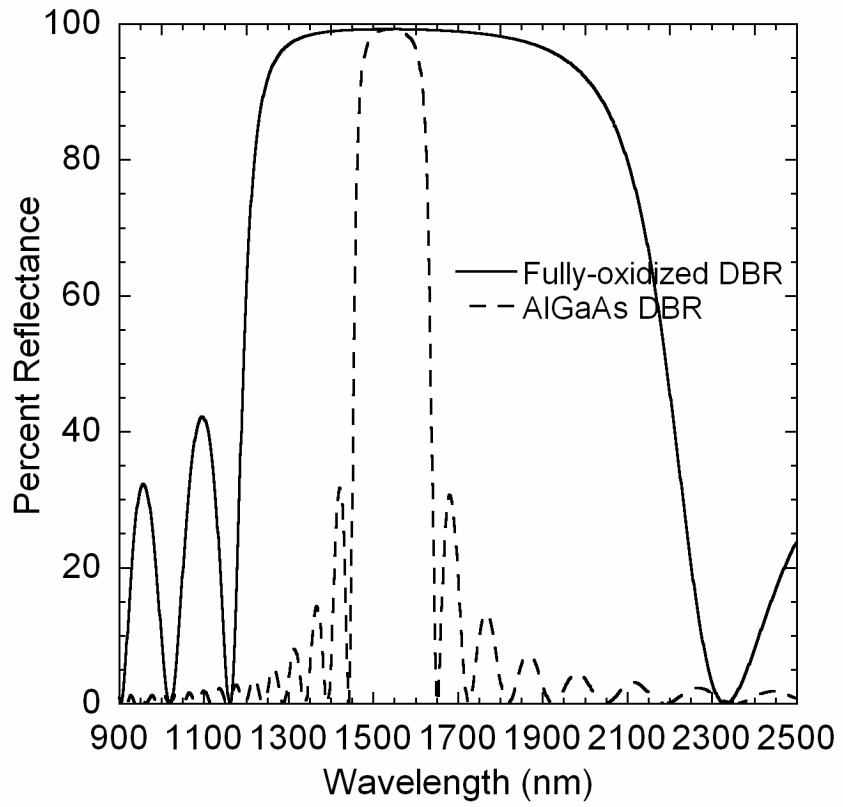

Figure 4.2. Simulated reflectivity spectrum of a 4-period GaAs/AlO_x DBR of the design described in this section (clad with GaAs), superimposed with a 20-period traditional AlGaAs DBR..

In References 8 and 9, extensive work was done to develop these mirrors for use in short-wavelength VCSELs operating near 980-nm. It has been shown that with the proper design, these all-epitaxially grown mirrors can be reproducibly fabricated. The use of graded composition layers to transition from the GaAs to the AlAs aids in the reproducibility and robustness of the process. Reference 11 describes how the linear composition grades prevent cracking and peeling of the thick oxidized mirror layers and leads to uniform oxidation fronts and high-quality VCSEL mirrors and devices.

4.1.2 Development of Fully-Oxidized DBR Epitaxial Structures

The attributes of fully-oxidized DBRs and their potentially simple integration into the double wafer-bonded VCSEL fabrication platform made them excellent candidates for use in the CWDM VCSEL arrays. Prior to use in long-wavelength VCSELs, several key design parameters were required.

The design of fully-oxidized DBRs differs from traditional DBRs in that the as-grown structure must be modified prior to its operation as a mirror at the design wavelength. Thus, the successful design of these structures requires an understanding of the relevant changes the AlAs undergoes during its conversion to AlO_x. The measurable relevant changes include three critical attributes: the change in index of refraction, the fractional change in thickness, and depth the oxidation reaction penetrates into the linear composition grade when the AlGaAs converts to AlO_x [11]. Once these three parameters are known, DBRs can be designed in a fashion similar to traditional GaAs/AlAs DBRs. The epitaxial layer cross-section of Figure 4.3 graphically depicts these three design parameters.

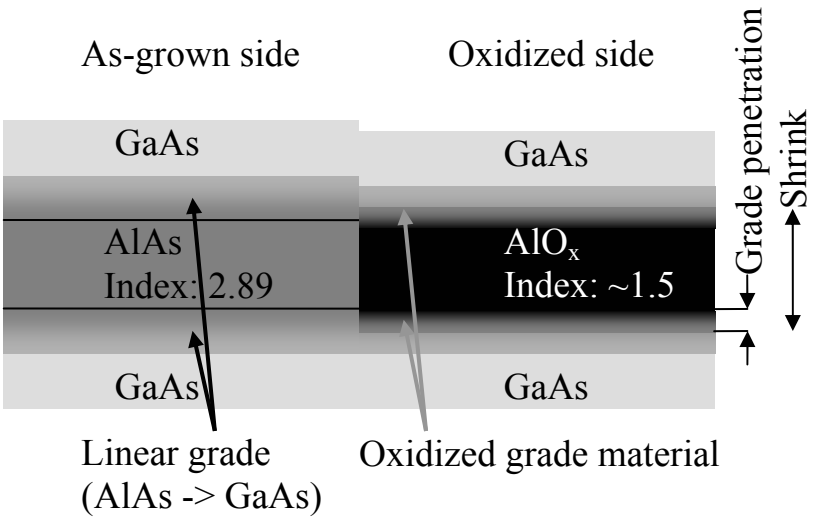

Figure 4.3. Cross-section schematic depicting the three critical design parameters for fully-oxidized DBRs: material shrink, grade penetration, and AlO_x index.

A reasonable starting guess for these values was taken from Reference 11. The starting guess assumed a 1.55 index for the AlO_x, oxidation of the linear grade up to, and including, the $Al_{0.51}Ga_{0.49}As$, and that the final thickness of the oxidized material is 88 % of the original. Based on these values, the mirror structure shown in Table 4.1 was generated and grown. The mirror is designed to be centered at 1540 nm. The linear grades were 0.05 wavelengths thick each, and for growth purposes the grade began at $Al_{0.92}Ga_{0.08}As$ and ended at $Al_{0.1}Ga_{0.9}As$. The GaAs layers were designed to be 0.2 wavelengths thick. Figure 4.4 shows the designed structure's index of refraction profile before oxidation and the anticipated index profile after oxidation. After the wafer was grown, the reflectance spectrum was measured. Figure 4.5 shows the as-grown reflectance spectrum of the wafer and the fitted simulation. For this fit, the

highest peak at 1240 was fit by uniformly adjusting the thickness of the entire structure. Based on the fit, it is estimated that the structure was grown 4 nm short.

Repetitions	Doping	X -value	Material	Thickness
4	Uid	0.100 to 0.920	AlGaAs	24.6481
4	Uid	1	AlAs	262.715
4	Uid	0.920 to 0.100	AlGaAs	24.6481
4	Uid	0	GaAs	91.1782
1	Uid	0	GaAs	11.3973

Table 4.1. Original full- oxidized DBR growth design based on values from Reference 11.

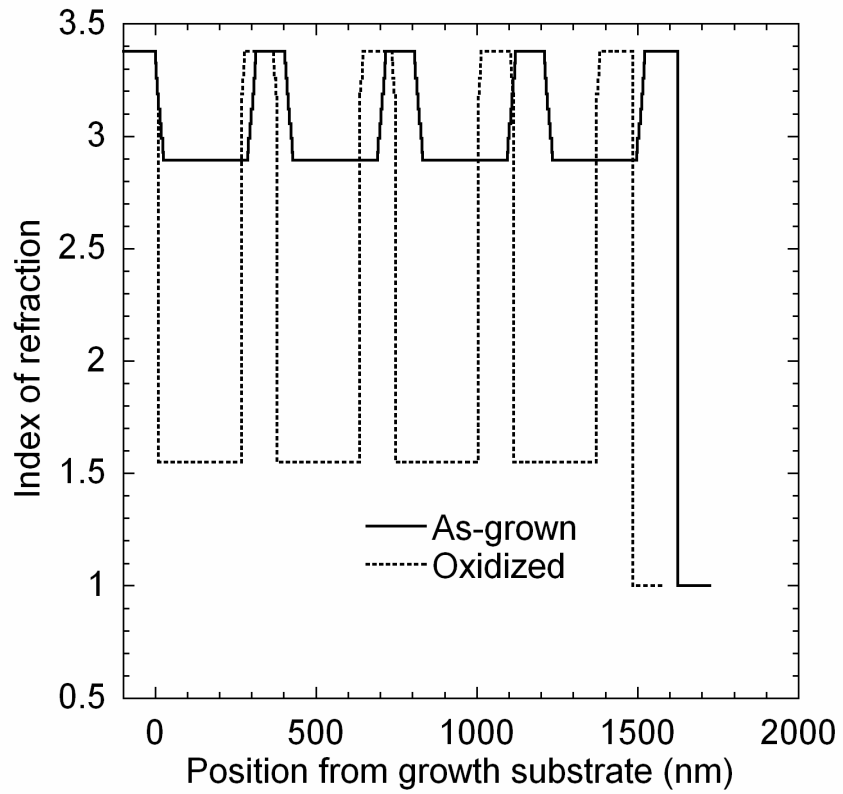

Figure 4.4. Anticipated index of refraction profile of the fully-oxidized DBR before and after oxidation.

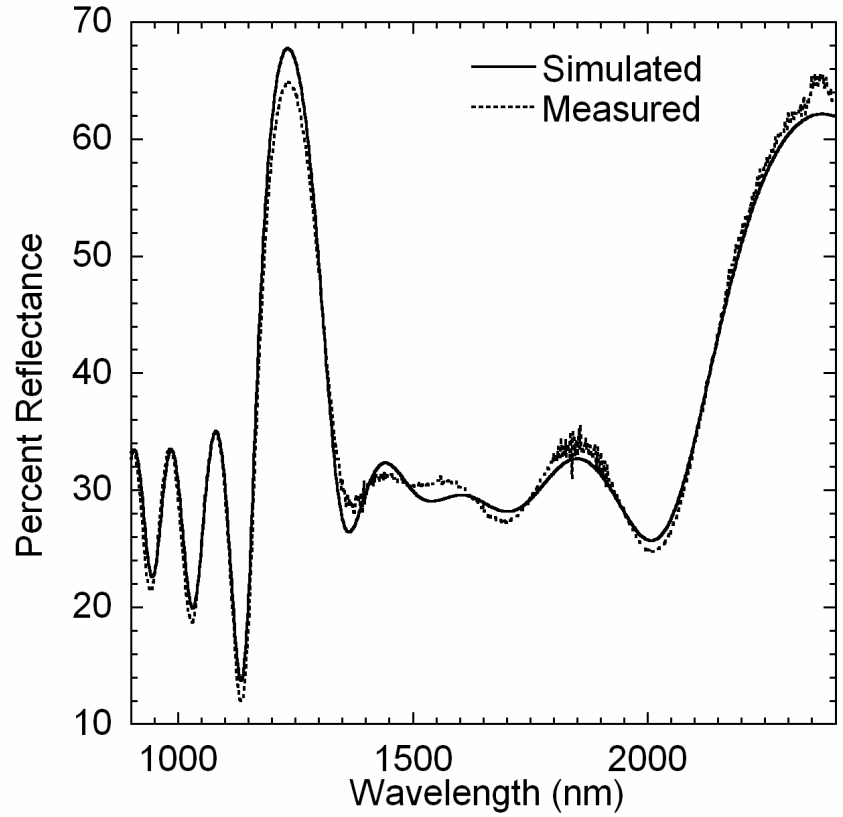

Figure 4.5. Measured and fitted reflectance spectrum from the as-grown (before oxidation) fully-oxidized DBR structure. Minor differences in shape are due to a missing growth buffer layer.

The as-grown wafer surface of the sample was etched with circular holes 15 μm in diameter (nominally), and spaced every 50 μm. The sample was oxidized as described in Chapter 5. The resulting fully-oxidized DBR reflectance spectrum shown in Figure 4.6 was measured. The shape of the measured reflectance is believed to be distorted by the relatively large holes that were etched in the sample to allow for oxidation of the AlAs layers. These holes were wet chemically etched and severe undercut took place causing the holes to enlarge to nearly 25-μm in diameter. Despite the odd shape of the stop band, it

is possible to estimate all three of the relevant oxidation attributes. The simulated fit shown in Figure 4.6 was made by assuming none of the graded material oxidized. This required the index of the AlAs to be 1.52 and the shrink value to be 89.75%. These values were used to plot the simulated fit shown in Figure 4.6. Based on this fit, the oxidized mirror structure has a peak reflectivity at 1620 nm instead of at 1534 nm, as was expected.

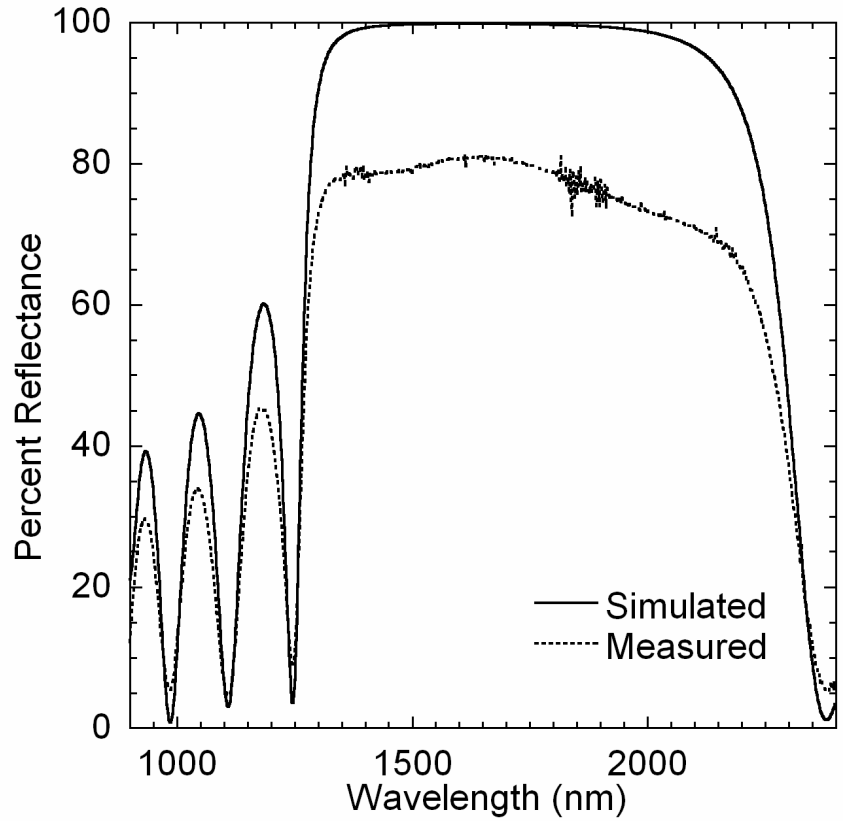

Figure 4.6. Measured and fitted reflectivity spectrum of the fully-oxidized DBR initial trial design. The fit assumed no graded material was oxidized. The peak reflectivity is near 1620 nm.

Because it is not reasonable to assume that none of the linearly composition-graded material adjacent to the AlAs layer in the DBR would oxidize, further attempts were made to fit the shape of the measured reflectivity spectrum. The process required adjusting the oxidation penetration depth first, then adjusting the index and the shrink parameter until the simulated width of the stop band and shape of the side lobes were matched to the measured reflectance data. The best fit was achieved for a shrink of 93.646%, an index of 1.537, and oxidation penetration up to and including the $Al_{0.78}Ga_{0.22}As$ layer of the composition graded material (6.46-nm penetration into the grade). Figure 4.7 shows this final fit.

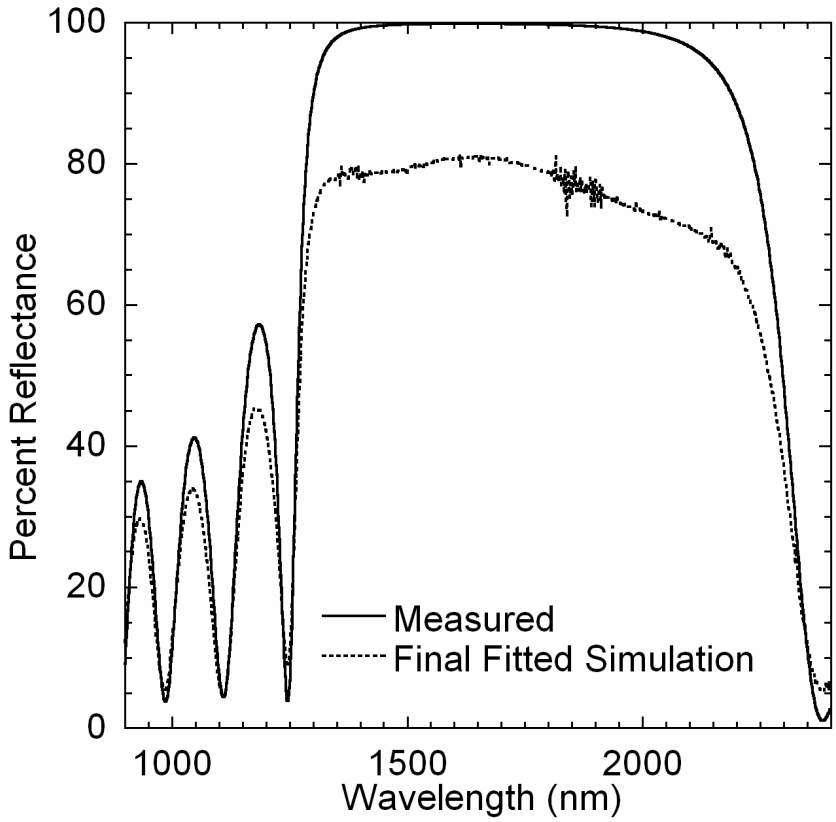

Figure 4.7. Best fit of the fully-oxidized DBR trial design. Fit assumes: shrink of 93.646%, index of 1.537 and oxidation penetration up to and including the $Al_{0.78}Ga_{0.22}As$ layer (6.46-nm penetration).

Based on the newly established design parameters, it is possible to design a fully-oxidized DBR that is centered at 1540 nm and has high mirror reflectivity over a broad wavelength range. Such a design is shown in Table 4.2 for a four-period DBR. This mirror was grown to be wafer bonded prior to testing. Once grown, the mirror was bonded to a 1 μm thick InP layer that was bonded to a GaAs substrate. This structure simulated the final VCSEL structure. The reflectivity spectrum of the same mirror after wafer bonding and oxidation is shown in Figure 4.8 along with its simulated reflectivity. The fit of the as-

grown sample, generated prior to oxidation, determined that the structure was grown 18 nm long. The fit in Figure 4.8 is based solely on the as-grown fit and the design parameters with no additional fitting to the oxidized reflectance spectrum. As is visible in Figure 4.8, the fit is very close and indicates that the design parameters are accurate and reproducible.

Repetitions	Doping	X -value	Material	Thickness	Note
1	Uid	1	AlAs	266.0401	Etch stop
1	Uid	0	GaAs	11.3973	
1	Uid	0	GaAs	91.1782	
4	Uid	0.100 to 0.920	AlGaAs	24.6772	grade
4	Uid	1	AlAs	231.423	
4	Uid	0.920 to 0.100	AlGaAs	24.6772	grade
4	Uid	0	GaAs	91.1782	
1	Uid	0	GaAs	11.3973	

Table 4.2. Final design of fully-oxidized DBR for peak reflectivity at 1540 nm. This mirror has been designed with an etch stop layer to allow it to be transferred to InP by wafer bonding.

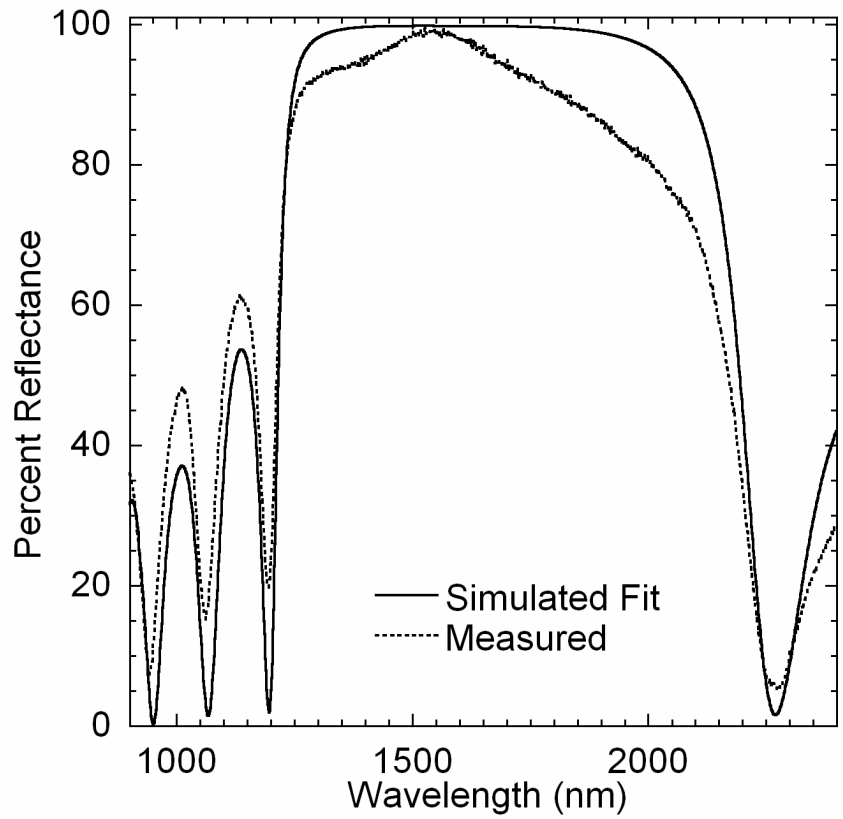

Figure 4.8. Measured and fitted reflectance spectrum of the final fully-oxidized DBR design. The mirror was wafer bonded to InP prior to oxidation. The simulated fit is based solely on the as-grown reflectance spectrum and the application of the AlAs to AlO_x design parameters. The reflectivity peak is at 1558 nm. The data has been linearly scaled to ease the comparison of the stop band and side lobe position with the simulated data.

The measured reflectivities shown in Figures 4.6, 4.7, and 4.8 clearly have a sloped stop-band shape. To investigate this shape, another series of samples was prepared and care was taken during the etching of the holes used to oxidize the samples. This mirror material had 7 mirror periods. A dry etch process was used to maintain the hole size at 15-μm diameter. With a 50-μm square pattern hole-pitch, the total area covered by the holes is only 7 %. These samples were then oxidized for various periods of time to examine the

difference this parameter made to the reflectivity peak of the mirror. Figure 4.9 shows the results. All the plots have nearly flat stop bands (the kinks near 2000 nm are a measurement artifact). The reduction in the amount of slope compared to Figures 4.6 through 4.8 is believed to be due to the reduced impact the smaller etch holes have on the large spot size reflectance off the samples. The figure shows that the mirrors shift to shorter wavelengths as the oxidation time increases. Reference 11 discusses this observation and attributes it to the increased amount of graded composition AlGaAs material that is allowed to oxidize as the oxidation time is increased. In this work, the mirror shifts 65 nm shorter as the oxidation time increased from a minimum value of 8 minutes (time required to completely oxidize all AlAs layers), to 18 minutes. With such a broad band reflectivity, the 65-nm wavelength shift is relatively minor and would have a minimal impact on a VSCEL structure. This again reflects the overall simplicity of fabricating fully-oxidized DBRs for VCSEL applications.

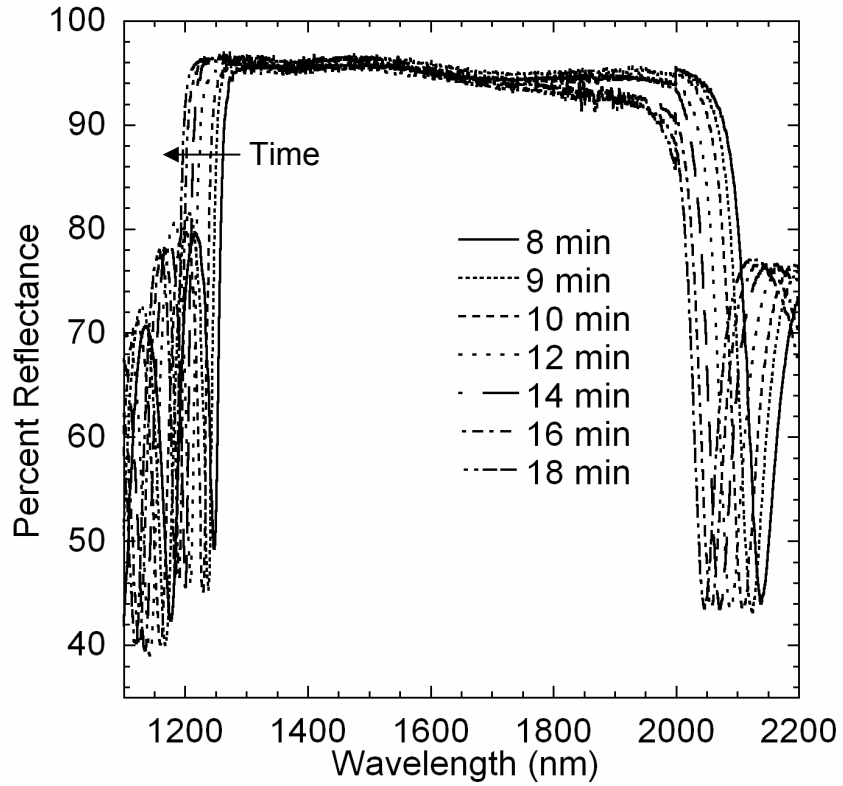

Figure 4.9. Measured reflectivity spectrums from a set of fully-oxidized mirrors that have been oxidized different lengths of time. The data has not been normalized.

4.1.3 Application of Fully-Oxidized DBRs to Long-Wavelength VCSELs

Demonstrating high-quality broad-area reflectivity from fully-oxidized DBRs is not sufficient to ensure that these mirrors can be successfully integrated with long-wavelength VCSELs operating near 1550 nm. The compatibility of the fully-oxidized DBR approach with wafer bonding, and verification that the mirrors do not induce excessive loss in the VCSEL were required to ensure successful application of these mirrors to long-wavelength VCSELs.

The loss of fully-oxidized AlO_x at the wavelengths of interest has been studied previously by others [12]. Reference 12 has found that AlO_x formed by

wet thermal oxidation exhibits a loss of 2.46 cm^{-1} at 1500 nm and 2.98 cm^{-1} at 1300 nm. These values are well within the values necessary for high-quality DBRs. This is especially true because the overall thickness for fully-oxidized DBRs is quite thin due to the limited number of mirror periods that are required. The fact Reference 9 has previously demonstrated high performance short-wavelength VCSELs using fully-oxidized DBRs also eliminated concerns regarding scattering loss at the AlGaAs/AlO_x interfaces.

Due to the small measured loss of the AlO_x, investigations were focused on the fabrication issues related to integrating fully-oxidized DBRs with long-wavelength VCSELs. Initial investigations did in fact show that optically-pumped VCSELs using the fully-oxidized DBRs could not reach lasing threshold. This section experimentally explores this problem and offers a solution and a discussion of the probable cause.

A brief description of the oxidation process is instructive to understanding the types of problems that can be encountered in fabricating long-wavelength VCSELs with fully-oxidized DBRs. The oxidation of AlAs involves the conversion of AlAs to aluminum oxide. The aluminum oxide formed is generally considered to be a non-stoichiometric amorphous material and hence is written as AlO_x. In order to oxidize an AlAs layer that has been buried in an epitaxial structure with layers of AlGaAs and GaAs, it is necessary to access the layer from the wafer surface. This access is typically accomplished

by etching mesas, holes [13], or trenches [11] in the wafer epitaxial layers. By doing so, the edge of the layer to be oxidized is exposed to the atmosphere. Though AlAs will oxidize in atmosphere, a stable oxide can rapidly be formed by exposing the material to temperatures in the 400-500°C range in a nitrogen and water vapor environment [10].

In Reference 9, VCSELs using fully-oxidized DBRs were fabricated by the mesa approach shown in Figure 4.10. The oxidation process proceeds from the edge of the mesa. As the oxidation process continues, the oxidation layer moves deeper into the structure from the edge of the mesa. These leading edges of the reaction are called the oxidation front. In the mesa VCSEL geometry of Reference 9, the oxidation fronts meet in the middle of the mesa pillar which coincides with the central axis of the VCSEL waveguide.

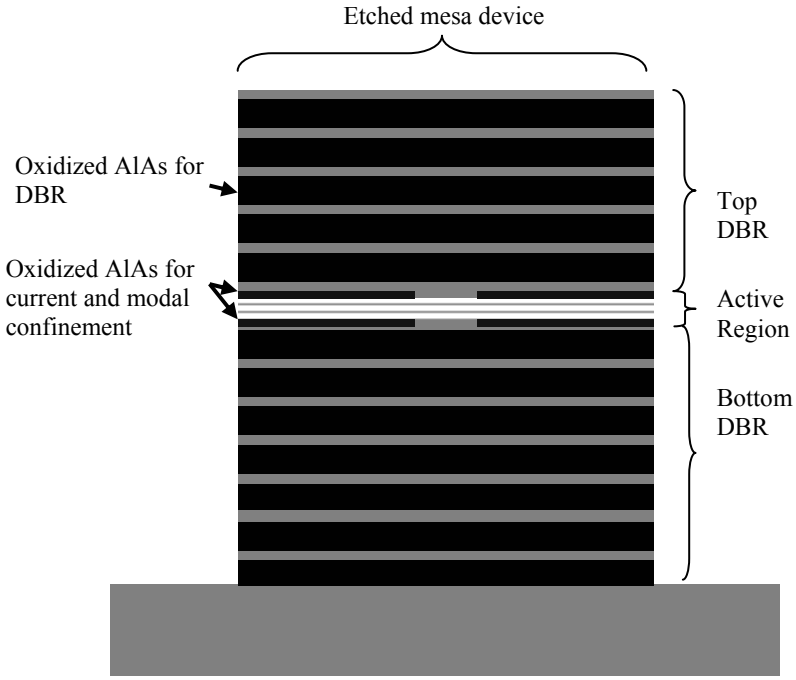

Figure 4.10. Cross-section schematic view of VCSELs successfully fabricated using fully-oxidized DBRs with a mesa approach as in Reference 9. Five top and seven bottom mirror periods are used.

In this work, double wafer-bonded VCSELs were initially fabricated using etched holes to reach the AlAs layers of the DBR (Figure 4.11). Each of the etched holes was located an equal distance from the central axis of the VCSEL so that as the oxidation progressed radially from the holes, the oxidation fronts would meet at all points equidistant from each etched hole. The central meeting point coincided with the central axis of the VCSEL. The VCSEL's central axis is defined by the center of the etched air-gap annulus waveguide that is described later in this chapter. Unlike the short-wavelength VCSELs of Reference 9, these devices did not reach lasing threshold despite multiple

process runs with different mirrors and known-good active-region wafers. Figure 4.11 shows a cross-section schematic view (a) and top view (b) of the

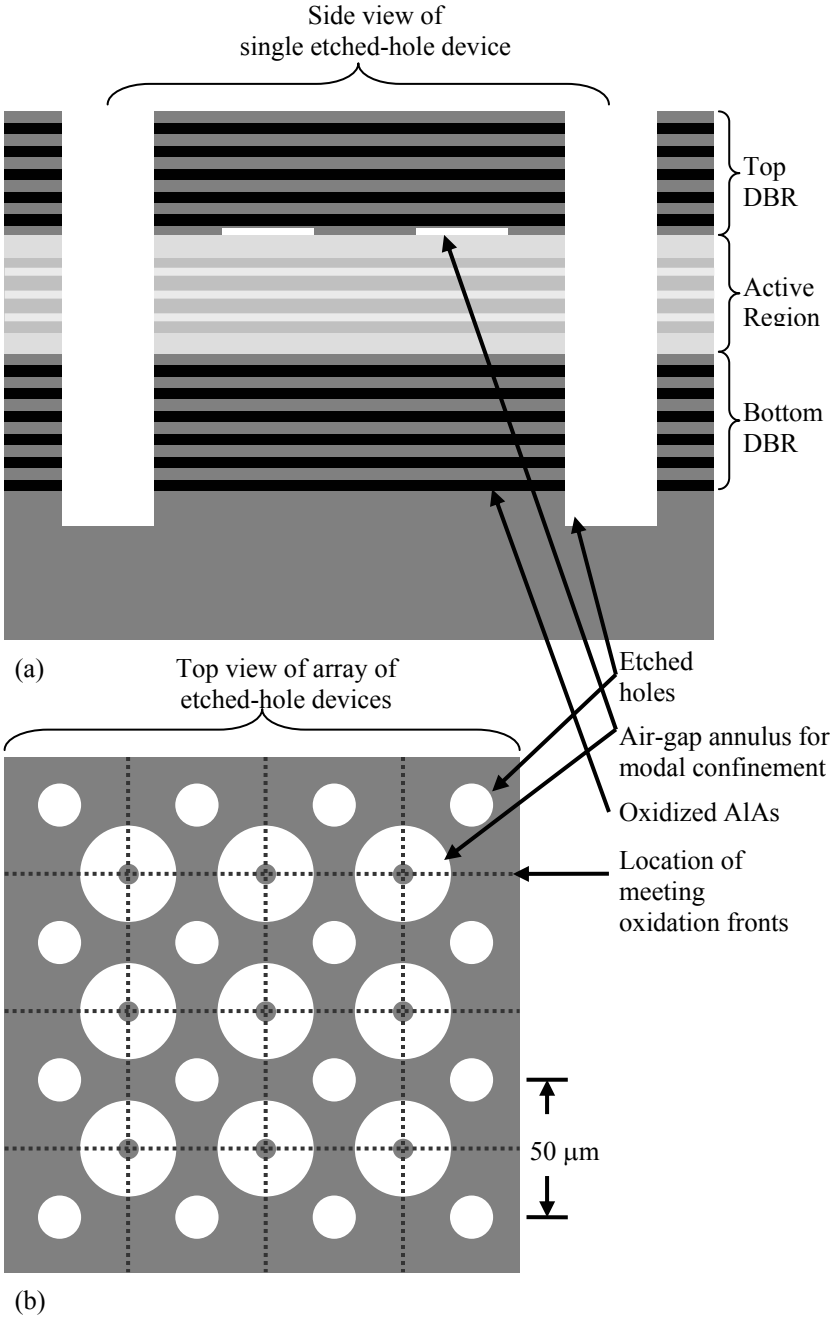

Figure 4.11. Cross-section (a) schematic view and top (b) view of the failed long-wavelength VCSEL oxidation approach using oxidation fronts centered over the VCSEL waveguide.

failed layout. Visual inspections during the oxidation calibration confirmed that the oxidation fronts proceeded in all directions at nearly the same speed and cleaved cross-sections showed all layers oxidized at the same rate.

Based on the failure of this approach, a new approach was selected to investigate the effect of the oxidation front meeting point on the VCSEL performance. Devices with their air-gap apertures offset from the oxidation front meeting point were fabricated on the same chip along side devices with centered apertures. Figure 4.12 shows the new arrangement. In this experiment, only the top DBR was a fully-oxidized mirror, the bottom DBR was a traditional AlGaAs DBR. VCSELs from this sample were tested and, once again, the centered aperture devices did not reach lasing threshold. However, the offset devices directly adjacent to each centered device did reach lasing threshold and operated as expected. This experiment verifies that the meeting of the oxidation fronts above the VCSEL aperture causes problems for long-wavelength VCSELs.

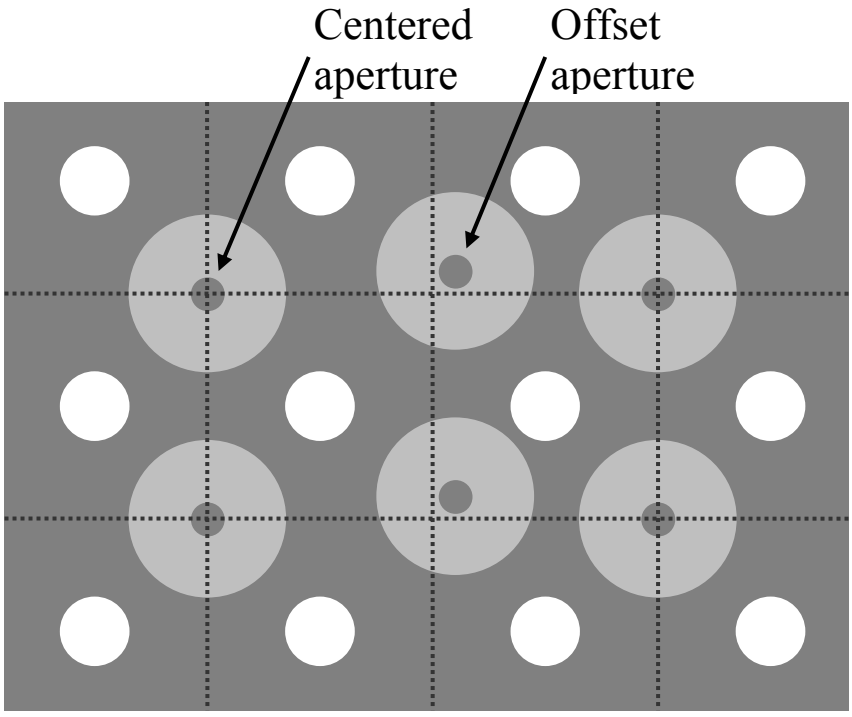

Figure 4.12. Schematic depicting diagnostic VCSEL arrangement with neighboring devices centered and offset from the oxidation front meeting point.

To investigate this effect further, small spot-size optical pumping of the VCSELs was conducted. In this technique, the VCSEL is raster scanned with a 2-μm spot-size 980-nm laser. The photoemission from the VCSEL is collected and the spectral width of the emission at half the maximum intensity (FWHM) is plotted as a function of position. The data is shown in Figure 4.13. From this figure it is evident that the mode shape of the centered VCSEL structure is severely distorted compared to its offset neighbor. This distortion may be caused by a variety of factors including stress in the material at the meeting

point of the oxidation front due to material shrinkage during oxidation. By

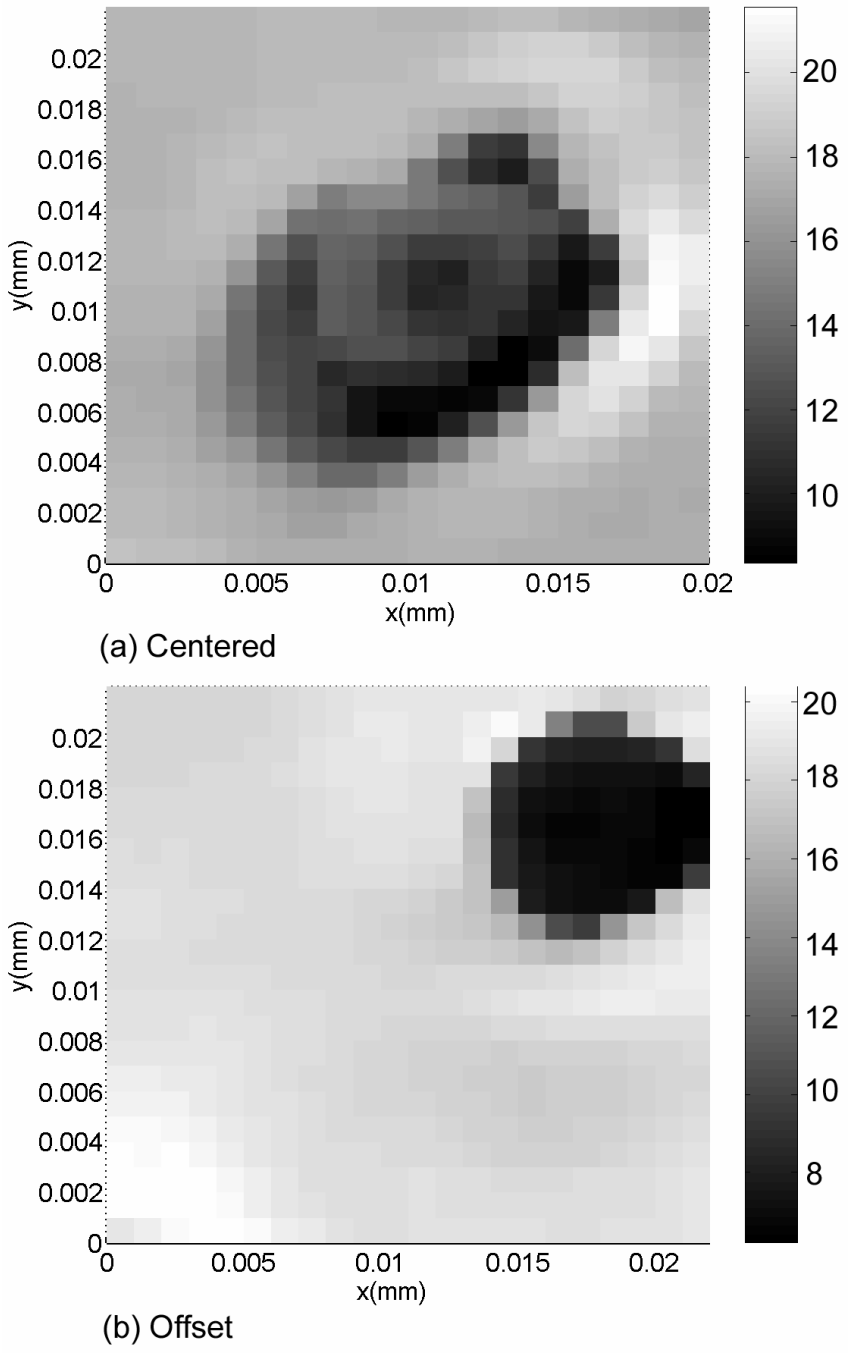

Figure 4.13. Photo emission FWHM spectral intensity maps of the centered (a) and offset (b) VCSEL designs. Distortion of the VCSEL waveguide is visible in the centered design.

offsetting the VCSEL aperture from the union point, the distortion is prevented and the devices operate normally.

4.1.4 Final Fully-Oxidized Mirror Design

Based on the material design parameters developed and the VCSEL experiments conducted, the final mirror design for the 2-D CWDM VCSEL array was developed. The VCSEL array would use a 5.5-period top DBR and a 6-period bottom DBR. To reduce the mirror reflectivity of the top DBR slightly, an SiO (index ~ 1.75) quarter wavelength anti-reflection coating was selected to minimize the air interface reflection at the output of the VCSEL. The layer design is identical to Table 4.2, except for the number of mirror periods used. Table 4.3 shows the predicted mirror reflectivities across the CWDM array with these selections.

Wavelength	Reflectivity of 5.5-period front mirror with anti-reflection coating	6-period back mirror
1470	99.837%	99.960%
1490	99.844%	99.963%
1510	99.848%	99.964%
1530	99.849%	99.965%
1550	99.849%	99.965%
1570	99.846%	99.964%
1590	99.842%	99.963%
1610	99.836%	99.960%

Table 4.3. Predicted mirror reflectivities of the selected fully-oxidized mirror designs at the CWDM wavelength positions.

In addition to the epitaxial design, a fabrication arrangement was selected. To avoid the problems associated with the placement of the oxidation

front, the etching of holes approach was discarded in favor of the trench etching approach used for diagnostic purposes in Reference 11. Each trench is 10-μm wide and they are located on a 100-μm pitch. With this approach, the oxidation fronts meet between adjacent VCSELs which are spaced 50 μm apart. Figure 4.14 shows this approach.

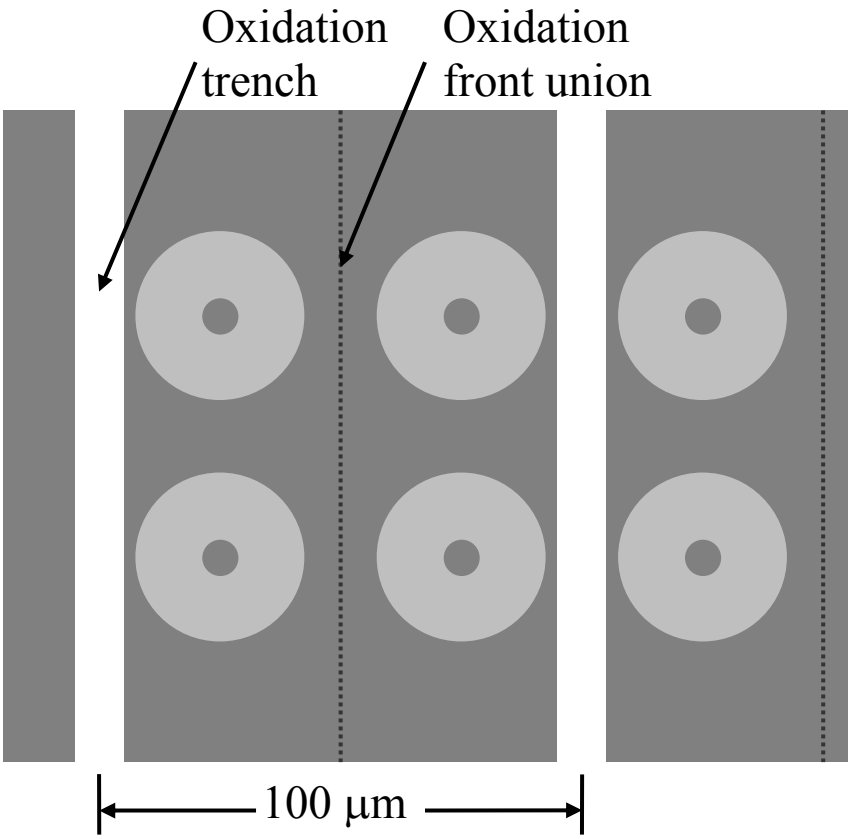

Figure 4.14. Top-view schematic of the final oxidation layout using oxidation trenches.

The fully-oxidized DBRs developed are high quality and can be integrated with the optically-pumped CWDM VCSEL arrays of this work. It should be noted that the mirrors are electrically insulating and have higher

thermal impedance than traditional AlGaAs DBRs. High-quality electrically-pumped VCSELs have been fabricated using these mirrors in an intra-cavity contacted configuration [9]. In addition, high-quality intra-cavity contacted VCSELs have been demonstrated with high thermal impedance antimonide based DBRs in other research [14]. The thermal impedance of the mirrors will be discussed in Chapter 6.

4.2 Active-Region Array Design

A properly designed quantum-well active region can provide gain across a relatively wide wavelength span. Commercial external-cavity tunable lasers use diode pumped active regions and can be designed to tune across a wavelength span over one-hundred nanometers wide. This wavelength span is still quite narrow compared to what is required for CWDM laser arrays however. To attain wide wavelength spans in commercial external-cavity tunable lasers, the diode is held at a fixed temperature, and the gain region is lengthened beyond what would normally be used in a standard edge-emitting laser. This technique works well for external-cavity tunable laser applications, but does not apply to wide wavelength span VCSEL arrays. The first problem is that the amount of single-pass gain available from an active region is dependent on the length of the gain material. For a VCSEL active region, this length is dependent on the thickness and number of quantum wells, and it is not possible to reach the

required gain necessary to reach lasing threshold across a hundred-nanometer wide wavelength span with a limited amount of gain material. The second challenge with achieving lasing across such a wide wavelength span from a quantum-well VCSEL active region is that lasing must also be supported across a range of temperatures. Though the requirements vary, most CWDM VCSEL arrays must operate un-cooled within a minimum temperature range of 0°C to 70°C. As the operating temperature increases, two processes can be observed in a VCSEL. The VCSEL's quantum-well gain peak wavelength shifts to longer wavelengths faster than the resonance cavity of the VCSEL and the quantum wells produce less overall gain. These processes can combine to reduce the amount of gain available at the lasing wavelength and further reduce the useful wavelength span a quantum-well VCSEL active region can support. To reduce the importance of these temperature effects, the room-temperature gain peak can be set to a wavelength shorter than the lasing wavelength so as the operating temperature increases the gain moves into alignment with the lasing wavelength of the VCSEL and the available gain can actually increase for a range of temperatures. The use of such a positive gain-mode offset is critical to achieving good high-temperature performance from single wavelength VCSEL chips and can help expand the lasing wavelength span a VCSEL active region can support. This span is typically less than about 70 nm.

4.2.1 Active-Region Integration and PL Selection

In order to support lasing across a wavelength span of 140 nm, more than one quantum-well active region in needed for the different wavelength channels in the CWDM VCSEL array. In this application, the 140 nm wavelength span of the array was divided into two VCSEL arrays with a 60 nm wavelength span, separated by 20 nm. The first array covered wavelength channels 1470, 1490, 1510, and 1530 nm, and the second array covered wavelength channels 1550, 1570, 1590, and 1610 nm. Each 60 nm wide wavelength group of VCSELs can be supported by a different single active region. With this grouping, only two active regions need to be integrated to support the full 140 nm wavelength span of the array. This same technique can be used with four integrated active regions to support 16 wavelength channels spanning 300 nm from 1310 nm to 1610 nm.

With each active region supporting a range of wavelengths, a compromise was needed in the wavelength placement of the PL peak of the active regions. The first active region needs to support lasing from 1470 through 1530 nm and from room temperature to 70°C. Experiments have shown that a gain-mode offset near 30 nm (gain-peak blue shifted from cavity resonance by 30 nm) gives good high-temperature performance (low threshold and high output powers) without sacrificing good room-temperature performance. Observations have also shown that gain-mode offsets larger than

50 nm can lead to poor operation because the gain at the lasing wavelength suffers at all temperatures. Hence, a maximum gain-mode offset of 40 nm is chosen. Gain simulations run by Joachim Piprek using PICS3D by Crosslight Software, Inc. show that at typical carrier injection levels the gain from the quantum wells is about 10 nm red-shifted from the PL peak. Thus for the 1470 to 1530 nm range, a PL peak of 1480 nm was chosen as the growth target. Similarly for the 1550 to 1610 nm active region, the PL target was chosen to be 1560 nm. Though these values are somewhat arbitrary, they were chosen to ensure all channels operated. Ideally, more active regions would be integrated so a positive gain-mode offset could be used for all channels in the array. The use of two active regions forces a compromise in the gain-mode offset, but demonstrates the concept of the heterogeneous integration of multiple active regions as applied to a CWDM VCSEL array.

4.2.2 Superlattice Design for Wavelength Control

Wavelength control for WDM systems is critical. With CWDM, the wavelength tolerances are 12 to 14 nm, but this tolerance also includes wavelength drift with temperature (about 7 nm of drift is typical). Thus, it is necessary to be able to control the lasing wavelength of each wavelength channel in the array to within about +/- 3 nm. This wavelength control requirement translated into two types of design requirements for VCSEL arrays. First, epitaxial growth-rate errors

must be compensated in the VCSEL fabrication process and second, a method for precisely controlling the wavelength separation between channels must be used. For wafer bonded VCSELs, both types of control can be achieved with relative ease.

Wafer bonded VCSELs involve sandwiching the laser active-region epitaxial layers grown on one substrate between two mirrors grown on separate substrates. Thus, the mirrors and the active regions are grown separately and one can fully access and measure each component of the VCSEL prior to using wafer bonding to combine the structures together. A technique has been previously developed to measure what the lasing wavelength of the completed VCSEL will be prior to wafer bonding, and then to trim the active-region thickness to adjust this predicted lasing wavelength prior to the wafer bonding assembly of the components. The detailed steps involved in this process will be described in Chapter 5 and only the concept and measurement results demonstrative of the technique will be presented here. For an in-depth discussion, see Reference 5.

Growth-rate error control adjustment begins by mounting the epitaxial layers of the active region to a glass slide with transparent wax. The active region on the glass slide forms a Fabry-Perot cavity with air on one side and wax on the other. Using a photospectrometer, the normal incidence reflectance

spectra of the mounted epitaxial layers can be measured as shown in Figure 4.15.

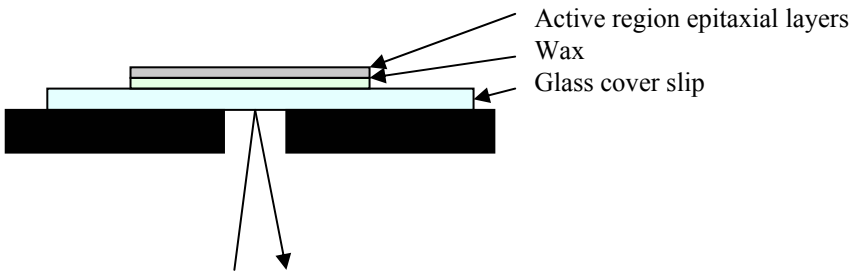

Figure 4.15. Bottom-side reflectance geometry used for the measurement of the VCSEL active-region thickness.

Once the reflectance spectra has been acquired, a transmission matrix solver such as the Vertical program can be used to fit the actual epitaxial layer structure thickness to the reflectance spectrum to determine the exact thickness of the actual epitaxial material grown. Figure 4.16 shows the actual measurement from the active region used in the devices that will be presented in Chapter 6. Here, the raw reflectance data has been fit with a simulated spectrum that takes into account the exact epitaxial layer structure of the active-region design. In this case, the growth was found to be 1.33% longer than requested.

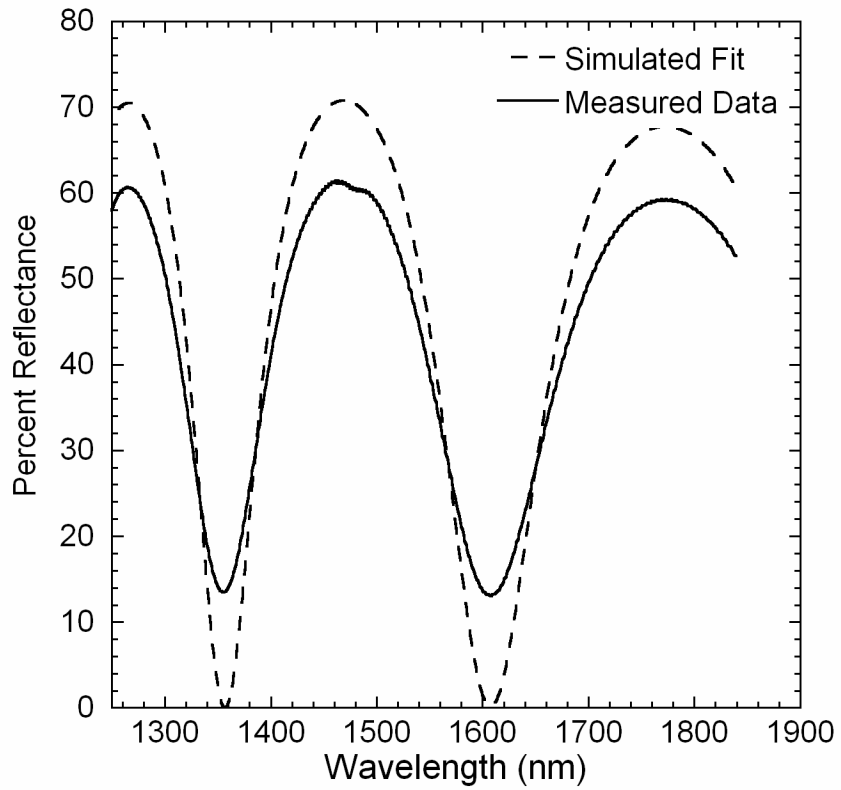

Figure 4.16. Measured and simulated reflectance spectra from the bottom 1480 nm PL active region of wafer TW 0306266-C. The fit was made by adjusting the structure thickness 1.33% longer then the requested growth thickness.

Experience predicts that MOCVD growth-rate variations can result in total active-region thickness variations of about +/- 3%. These thickness errors can be accommodated by growing superlattice periods on each side of the active region. After growth, the total thickness of the active region can be measured and the appropriate number of superlattice layers can be removed to trim the total thickness of the active region and ensure that the final lasing wavelength of the wafer bonded VCSEL is within the required wavelength window for the CDWM channel. These superlattice periods are placed on each side of the

active region because making large thickness adjustments on just one side of the active region can cause the periodically spaced quantum wells to no longer align well to the electric-field standing wave in the cavity.

Superlattice periods are also used to create the CWDM channels on each of the two active regions [2-4]. Each of the active regions will be used to fabricate lasers operating at four different wavelengths. Thus, it is necessary to be able to trim the cavity length laterally along the surface of the wafer to generate four different step levels as shown in Figure 4.17. To attain these four step levels, a minimum of 3 superlattice layers are needed. The thickness of these layers is determined by the need to change the VCSEL lasing wavelength by the CWDM channel spacing of 20 nm with the removal of each layer. The exact epitaxial thickness necessary is determined by the entire VCSEL active region and mirror structure and is calculated with the aid of the Vertical program. Because the superlattice layers are placed along the bonded interface of the active region and the high index layer of the DBR mirrors, the standing electric field is at a null at this point and the index of refraction of the superlattice material has little bearing on the amount of wavelength shift induced; only the thickness matters.

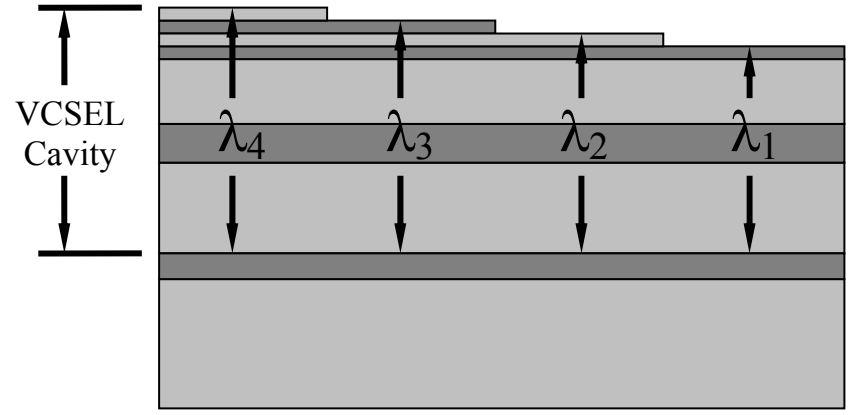

Figure 4.17. Cross-section of active-region wafer surface showing the laterally etched superlattice layers used to generate VCSEL cavity lengths of different thicknesses.

Because the growth-rate error thickness adjustment superlattice and the CDWM channel-adjustment superlattice were to be one and the same, more than the minimum of three superlattice layers were placed on the one side of the active region. Six layers designed to each adjust the VCSEL lasing wavelength by 20 nm were placed on the substrate side of the active region. Four more superlattice layers, each designed to adjust the lasing wavelength by 10 nm, were placed on the top side of the active region. If the growth is too short, then the extra three coarse and four fine superlattice layers are present to maintain the total active-region length to attain the proper lasing wavelength. In the event that the growth rate is perfect, one coarse superlattice layer and two of the fine superlattice layers can be removed. If the growth is too long, then as many as three coarse control layers and four fine control layers can be removed to maintain the proper lasing wavelength. The combination of the coarse-pitch superlattice and the fine-pitch superlattice layers allows for the simultaneous

elimination of +/- 3% total growth-rate errors to hit wavelength specifications within +/- 5 nm and the precise control of the 20-nm CWDM channel spacing.

For the VCSEL mirror and active-region design used in this work, a change in the physical length of the laser cavity of 11.6 nm would induce a lasing wavelength shift of 10 nm. Thus the four layers of the fine-pitch superlattice on the top of the active region required a total of 46.4 nm of material and the six layers of the bottom coarse superlattice were a total of 139.2 nm thick. Because growth-rate errors can cause the total structure to be too long or too short, one coarse superlattice layer and two of the fine superlattice layers are added for the event that the growth is too short and they would be removed if the growth rate were perfect. Thus, the superlattice thickness of the layers remaining under perfect growth conditions would be 23.2 nm for the fine superlattice layers and 116 nm for the coarse superlattice layers.

4.2.3 Final Active-Region Epitaxial Design

In Chapter 3, a new optically-pumped period-gain active-region design was presented. This design demonstrated improved temperature performance and lower optically-pumped laser thresholds. The new design uses InP carrier-blocking layers to achieve uniform carrier filling of the quantum wells and thus more efficiently uses optically-generated carriers. Chapter 3 also presented a design optimization routine to properly place the InP carrier-blocking layers

when other active-region parameters are known. These parameters include the lasing wavelength, the number of quantum wells, the optical thickness of the active region, the thickness of the superlattice regions, and the optical absorption of the pump wavelength in the barrier materials.

As in the VCSELs designed in Chapter 3, the CWDM array active region was designed to use a total of 3 quantum wells in each active region. The optical cavity length of each of the two active regions was chosen to be 2.5 wavelengths at the center of the wavelength spanned by each active region. Thus, the longer PL active region (1560 nm), for the wavelength span from 1550 to 1610 nm, was designed to be 2.5 wavelengths at 1580 nm. The shorter PL active region (1480 nm) was designed to be 2.5 wavelengths at 1500 nm, midway between the 1470- to 1530-nm range of this active region. This wavelength also was used as the design wavelength for the proper placement of the quantum wells to ensure the wells would be centered on the standing electric field in the VCSEL cavity. Based on the measured transmission loss through the devices in Chapter 3, the absorption of the 1.22-Q InGaAsP barrier material at the optical pump wavelength of 980 nm was estimated to be approximately 20000 cm^{-1}.

With these parameters, and the design algorithm of Chapter 3, the final design for the two optically-pumped active regions was generated. These designs are shown in Table 4.1. The VCSEL array is to be optically pumped

from the backside, hence the active regions are grown upside-down from their final orientation on the VCSEL chip. These active regions were grown by an outside supplier and the exact composition required to achieve the requested strain and PL target is not known precisely. Layers B-1 through B-23 correspond to the 1480-nm PL active region and are grown on the bottom of the stack. T-1 through T-23 correspond to the 1560-nm PL active region and are grown on the top of the stack. No intentional doping was used. The total single pass pump absorption efficiencies of these two active regions was estimated to be 79% for the bottom active region and 82% for the top active region.

To simplify the growth and processing of the active region, only five different composition materials are used in the entire double active-region stack. InGaAs is used as an etch-stop layer between each active region and between the bottom active region and the substrate. InP is used as a cladding layer, carrier-blocking layer, and a layer of the superlattice structures. 1.22-Q InGaAsP is used as the pump absorbing barrier material and a layer of the superlattice structures. Finally, two different InGaAsP layer compositions are used in each of the quantum-wells designs.

#	Material	Thick (nm)	Composition	Strain	Comment
	InP	--------	InP	None	Growth Buffer Layer
	InGaAs	200	InGaAs	LM	Etch Stop Layer
B-1	InP	23.2	InP	LM	Superlattice
B-2	InGaAsP	23.2	BG: 1.22 μm	Tensile	Superlattice
B-3	InP	23.2	InP	LM	Superlattice
B-4	InGaAsP	23.2	BG: 1.22 μm	Tensile	Superlattice

B-5	InP	23.2	InP	LM	Superlattice
B-6	InGaAsP	23.2	BG: 1.22 μm	Tensile	Superlattice
B-7	InP	20.7	InP	LM	Cladding
B-8	InGaAsP	226.2	BG: 1.22 μm	Tensile	Barrier
B-9	InGaAsP	5.7	PL : 1480 nm	Compressive	Quantum Well
B-10	InGaAsP	177	BG: 1.22 μm	Tensile	Barrier
B-11	InP	15	InP	LM	Carrier-blocking Layer
B-12	InGaAsP	27	BG: 1.22 μm	Tensile	Barrier
B-13	InGaAsP	5.7	PL : 1480nm	Compressive	Quantum Well
B-14	InGaAsP	189.2	BG: 1.22 μm	Tensile	Barrier
B-15	InP	15	InP	LM	Carrier-blocking Layer
B-16	InGaAsP	14.65	BG: 1.22 μm	Tensile	Barrier
B-17	InGaAsP	5.7	PL : 1480nm	Compressive	Quantum Well
B-18	InGaAsP	132.8	BG: 1.22 μm	Tensile	Barrier
B-19	InP	181	InP	LM	Cladding
B-20	InGaAsP	11.6	BG: 1.22 μm	Tensile	Superlattice
B-21	InP	11.6	InP	LM	Superlattice
B-22	InGaAsP	11.6	BG: 1.22 μm	Tensile	Superlattice
B-23	InP	11.6	InP	LM	Superlattice
	InGaAs	20	InGaAs	LM	Etch Stop Layer
T-1	InP	23.2	InP	LM	Superlattice
T-2	InGaAsP	23.2	BG: 1.22 μm	Tensile	Superlattice
T-3	InP	23.2	InP	LM	Superlattice
T-4	InGaAsP	23.2	BG: 1.22 μm	Tensile	Superlattice
T-5	InP	23.2	InP	LM	Superlattice
T-6	InGaAsP	23.2	BG: 1.22 μm	Tensile	Superlattice
T-7	InP	21	InP	LM	Cladding
T-8	InGaAsP	256	BG: 1.22 μm	Tensile	Barrier
T-9	InGaAsP	6	PL : 1560nm	Compressive	Quantum Well
T-10	InGaAsP	190.5	BG: 1.22 μm	Tensile	Barrier
T-11	InP	15	InP	LM	Carrier-blocking Layer
T-12	InGaAsP	25.6	BG: 1.22 μm	Tensile	Barrier
T-13	InGaAsP	6	PL : 1560nm	Compressive	Quantum Well
T-14	InGaAsP	202	BG: 1.22 μm	Tensile	Barrier
T-15	InP	15	InP	LM	Carrier-blocking Layer
T-16	InGaAsP	14.5	BG: 1.22 μm	Tensile	Barrier
T-17	InGaAsP	6	PL : 1560nm	Compressive	Quantum Well
T-18	InGaAsP	138.1	BG: 1.22 μm	Tensile	Barrier
T-19	InP	207	InP	LM	Cladding
T-20	InGaAsP	11.6	BG: 1.22 μm	Tensile	Superlattice
T-21	InP	11.6	InP	LM	Superlattice
T-22	InGaAsP	11.6	BG: 1.22 μm	Tensile	Superlattice
T-23	InP	11.6	InP	LM	Superlattice

Table 4.4. Dual active-region epitaxial design for CDWM array spanning 140 nm. All Tensile layers are -300 ppm, compressive layers are +1%, and LM means lattice matched.

In a multi-wavelength VCSEL array using a single active region, the position of the peaks and valleys of the standing-wave electric field shifts with respect to the quantum wells for each different wavelength VCSEL. This effect is simulated and shown in Figure 4.18 for a 1470 and 1530-nm VCSEL using the same active region and the same fully-oxidized DBR (three 23.2-nm superlattice periods are removed from the right side of the active region to tune the wavelength by 60 nm). As is evident from the figure, the overlap of the standing wave field with the quantum wells differs for each of the two wavelengths much as it would for the 1490 nm and 1510 nm VCSELs of the array. This difference in overlap leads to a different gain enhancement factor (Γ_{enh}) for each wavelength channel in the multi-wavelength VCSEL array [15]. By careful design, this effect has been minimized by centering the wells on the standing wave peaks when the lasing wavelength is in the middle of the wavelength span covered by each active region. This corresponds to 1500 nm and 1580 nm for the two active regions of the CWDM array. Table 4.5 shows the predicted enhancement factor for each channel in the WDM VCSEL array. These values are calculated using Vertical and the final VCSEL design structure (mirrors and active region). All channels maintain at least a 1.9 gain enhancement factor.

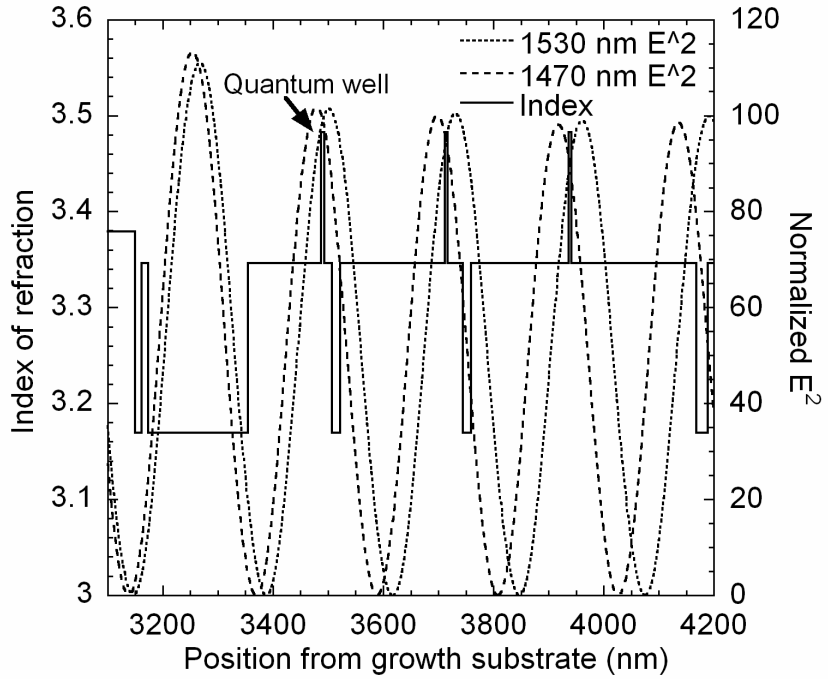

Figure 4.18. Simulation of the shifting of the standing wave in the VCSEL for two different wavelength VCSELs in the array.

Channel Number	Wavelength	Active Region	Enhancement Factor (Γ_{enh})
1	1470	Bottom (1480 PL)	1.90
2	1490	Bottom (1480 PL)	1.96
3	1510	Bottom (1480 PL)	1.96
4	1530	Bottom (1480 PL)	1.90
5	1550	Top (1560 PL)	1.91
6	1570	Top (1560 PL)	1.97
7	1590	Top (1560 PL)	1.96
8	1610	Top (1560 PL)	1.91

Table 4.5. Predicted gain enhancement factor for each wavelength channel of the CWDM VCSEL array.

4.2.4 Final Active-region Integration Design

The final active-region design aspect involves the integration of the InP-based active regions on the AlGaAs-based DBR wafer. Nonplanar wafer bonding was presented in Chapter 2 as viable approach for integrating different epitaxial

device structures on the surface of a wafer. In Chapter 2 the approach was successfully applied in the fabrication of a 2-D WDM VCSEL array. Nonplanar wafer bonding will be used to laterally integrate the two active regions designed in this chapter onto AlGaAs DBR material grown on a GaAs substrate. The precise process details of this integration will be reserved for Chapter 5. In this section, the final integration geometry will be selected based on the work completed in Chapter 2. The integration geometry includes the spacing of the active regions integrated on the AlGaAs DBR and the superlattice etching that will be used to generate the total of eight wavelength-differentiated channels on each CWDM VCSEL chip.

The VCSELs demonstrated in Chapter 2 were fabricated by the backside processed nonplanar wafer bonding technique. It was ascertained at the time that the success of this approach and the PL data from the nonplanar pressure block approach ensured the validity of the nonplanar pressure block approach which had been chosen for the final CWDM array. Chapter 6 will support this conclusion with the successful test results from the CWDM array.

Two active regions are to be integrated onto the bottom AlGaAs DBR by nonplanar pressure block nonplanar wafer bonding. The final structure is to be an eight-channel, two-dimensional, CWDM VCSEL array. Each active region supports 4 wavelength channels and the lateral spacing between these device regions was selected to be 250 μm. The width of each of the integrated active-

region stripes was chosen to be 750 μm with 250 μm etched-back bending accommodation regions separating the integrated top and bottom grown active regions. The actual bending accommodation regions are only 200 μm but during the etch-back step an extra 50 μm is removed to ensure that devices are not placed directly on stress damaged material. Figure 4.19 depicts the lateral placement of the different active regions and the location of the etched superlattice regions for each different laser in the array.

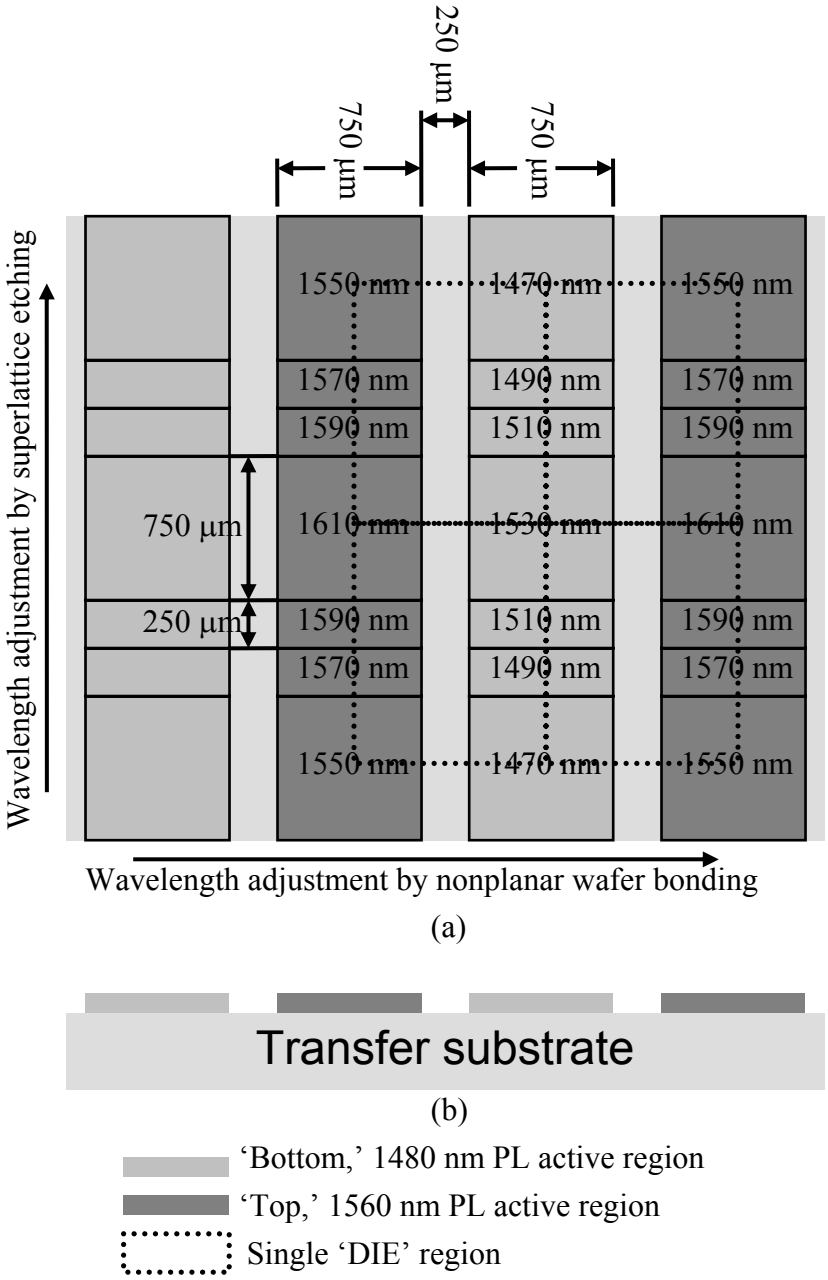

Figure 4.19. Schematic showing (a) a top view of the placement of the different active regions and the location of the etched superlattice regions for each different laser in the array, and (b) a side view with the two integrated active regions.

The final die size for the CDWM array chip is 1 by 1.25 mm. Channels groups 1-4 (1470 – 1530 nm) and 5-8 (1550 – 1610 nm) are spatially separated by 500 μm with an inter-channel spacing of 250 μm. The inter-channel spacing of 250 μm was chosen to be compatible with commercially available fiber arrays. The 500 μm separation between channel groups from each active region was chosen to avoid placing the VCSEL device too close to the etched-back bending region associated with the nonplanar wafer bonding process.

4.3 Mode Control in the Optically-Pumped VCSEL

In order for the VCSELs of the CWDM array to operate in a single transverse mode, a method for mode control was required. The typical method of using oxidized AlAs layers was not well suited to this structure because oxidation was already being used to fabricate the mirrors and it would be difficult to separate the oxidation of the mirror layers and the modal confinement layer. Extensive research has been done on mode confinement techniques in VCSELs [16] and the development of this theory is beyond the scope of this thesis. This section describes the approach selected, and presents and justifies the design.

Modal confinement is not needed just to maintain single-mode properties; it also works to maximize the overlap of the mode with the gain in the active region. With a well defined mode size, a pump-beam size can be

determined that maximizes the overlap of the lasing mode and the gain to minimize the laser threshold and prevent non-linear 'kinks' near VCSEL threshold. The strength of the waveguide also determines how many modes will be supported.

It is important to maintain a waveguide with weak enough confinement to support only one lasing mode, but strong enough to prevent the mode size from extending beyond the range of efficient pumping. To make matters difficult, the same modal structure does not lead to the same confinement in VCSELs spanning a wide wavelength span. The approach in this section was developed to deal with all these issues.

4.3.1 Aperture Guiding With Patterned Wafer Bonding

The technique selected for mode confinement was the use of an etched air-gap annulus aperture buried in the VCSEL structure. This air gap is actually formed by etching a ring on the top mirror wafer surface prior to wafer bonding. Thus, after wafer bonding the etched ring is located at the bonded interface against the surface of the VCSEL active region. Because the wafer-bonded interfaces are designed to be located at the electric-field standing wave null in the cavity, the air gap has a weak effect on the VCSEL. This was the method selected for creating weak modal confinement in the CWDM VCSEL array elements.

The benefits of this approach are twofold. First, the approach is simple to implement in wafer bonded structures because of the complete access to the active-region/mirror interfaces prior to wafer bonding. Second, the aperture strength can be easily adjusted by varying only one dimension, the depth of the etched annulus. Figure 4.20 shows a schematic of the aperture. In this work, the aperture is etched on the top GaAs layer of the AlGaAs DBR prior to wafer bonding. This was done so the thickness of the required superlattice layers on the active-region surface would not interfere with the air-gap etch-depth design flexibility. The top GaAs surface of the wafer is over 100-nm thick, so any etch-depth up to 100 nm would not hit the reactive AlAs layers and interfere with other processing aspects of the device.

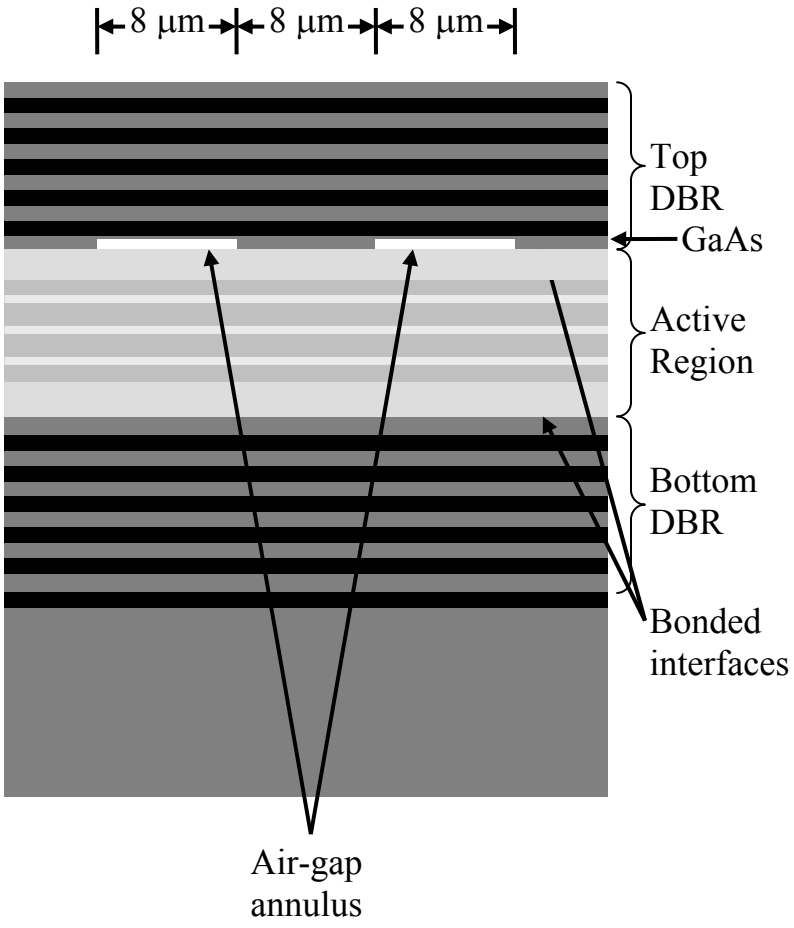

Figure 4.20. Schematic of the air-gap annulus aperture for modal confinement in the optically-pumped wafer bonded VCSEL array.

Previous work conducted by Gore Photonics [unpublished] verified that optically-pumped single-mode VCSELs using aperture guiding structures have their lowest thresholds and highest temperature performance when the index guide structure is 7-8 μm in diameter. Because of the similarity of the devices of this work and those developed at Gore, an 8-μm diameter was also targeted for this work. Another reason for choosing 8-μm diameters for these devices

was to match the available spot size of the 980-nm pump laser fiber focuser used in testing. The focuser has a 5-μm diameter spot size at the beam waist. Because the beam waist is fairly long (10's of microns) this is a favorable place to operate because it aids the pump/sample alignment process. Thus for testing purposes, devices significantly larger than 5 μm are not desirable. Despite these reasons, other device diameter sizes were explored (5, 8, 11, 14 μm). In these tests, the 5 μm devices were difficult to test because their small size and large single-mode diameter required precise pump alignment and yielded poor gain-mode overlap. The 11 and 14 μm device sizes were multimode, and using a shallower etch depth to weaken the confinement would only enlarge the mode and reduce its overlap with the pump spot. In the end, a decision was made to use 8 μm as the device diameter.

A simple way to calculate the strength of the modal confinement is to use an effective index approach and a normalized frequency approach from fiber theory. The effective index approach calculates the electric field standing wave in the central portion of the VCSEL without the air-gap aperture and uses this to determine the effective index of the entire VCSEL structure. This index is considered the 'core' index of the VCSEL waveguide in the subsequent normalized frequency analysis. Next, the same standing wave is overlapped with the air-gap of the air-gap annulus and the new effective index it calculated

that takes the thin air-gap region into account. This index is considered the 'cladding' index of the VCSEL waveguide.

With the core and cladding index values known (n_{core} and $n_{cladding}$), and the VCSEL wavelength (λ) and waveguide annulus center diameter known (d=8 μm), the waveguide is treated in the same fashion as a fiber waveguide and the normalized frequency is calculated by: $V = \pi d\sqrt{n_{core}^2 - n_{cladding}^2}\,/\lambda$ [17]. This value is referred to as the V-parameter. Fiber waveguide theory tells us that the V-parameter must be below 2.405 for a waveguide to remain single mode.

Because the VCSEL waveguide is formed by an aperture guiding technique the fiber analysis is not directly applicable. Regardless, the V-parameter is simple and allows for waveguide strengths to be compared relative to each other. The ease of use and its successful results justify the approach. Section 6.2 will discuss the impact the design of the modal confinement structure has on the VCSEL performance. Experience in this project has shown that for VCSEL air-gap abrupt apertures V-parameter values close to 3.5 function best.

Due to the shift in the position of the standing wave electric field in a WDM VCSEL array, the overlap of the standing wave field null with the air-gap annulus is increased for the shorter wavelength devices. This leads to stronger modal confinement for longer wavelength lasers. Figures 4.21 and 4.22 show a

1470 nm VCSEL and a 1530 nm VCSEL of the design used in this work. The air gap on the AlGaAs mirror side of the wafer-bonded interface is visible. The figures show that the standing wave null of the electric field is closer to the air gap in the shorter wavelength laser and hence has less impact on the effective index and leads to smaller V-parameter and weaker guiding of the lasing mode. This pattern is systematically true. For a given active region and air-gap annulus, the shorter wavelength lasers all have weaker confinement.

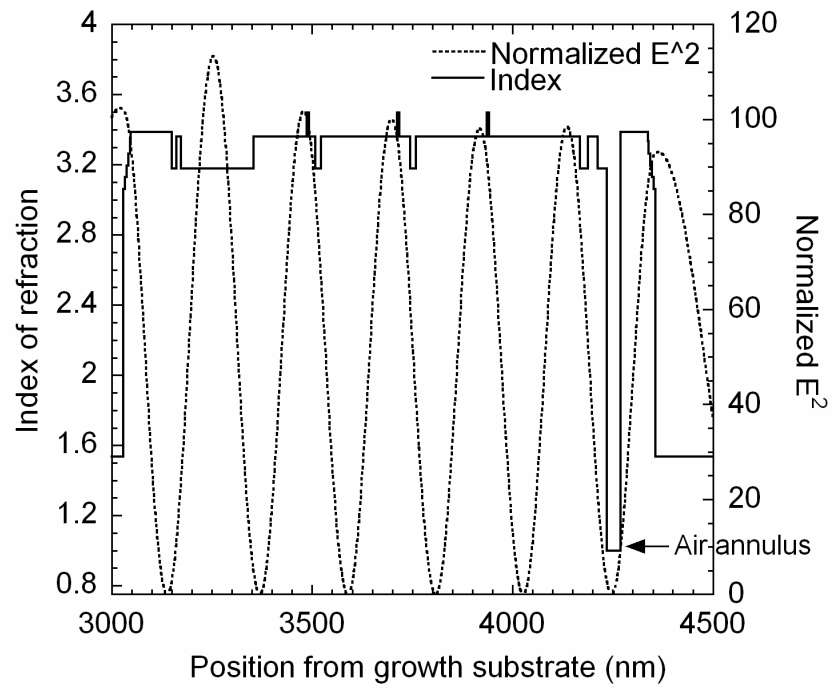

Figure 4.21. Standing wave plot superimposed on design structure plot for a VCSEL operating at 1470 nm and using the 1480 nm PL peak active region. Note the overlap of the standing wave with the air-gap aperture.

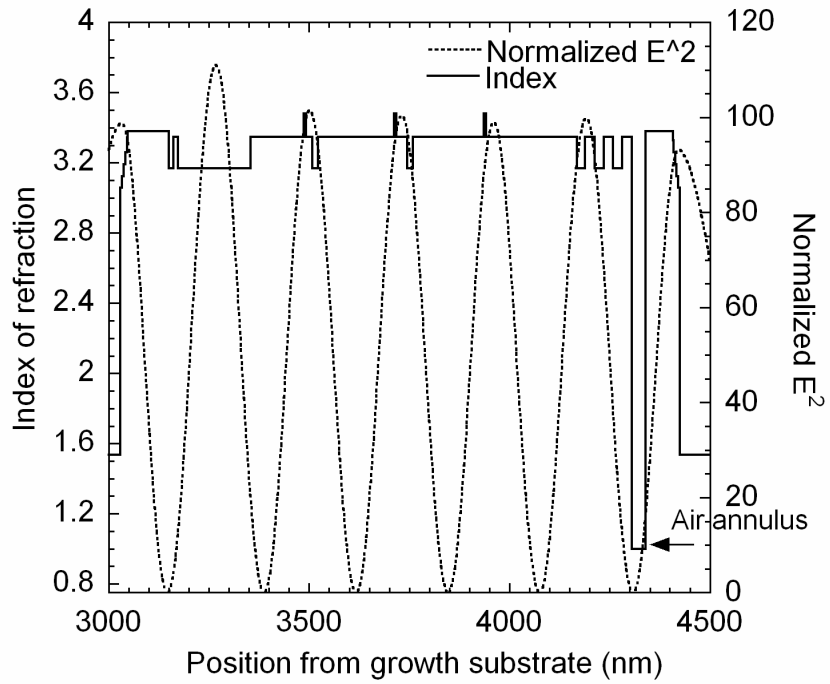

Figure 4.22. Standing wave plot superimposed on design structure plot for a VCSEL operating at 1530 nm and using the 1480 nm PL peak active region. Note the overlap of the standing wave with the air-gap aperture.

It is clearly not possible to use one air-gap annulus design for modal confinement in every VCSEL of the CWDM array. Ideally, a different etch depth for of each wavelength laser in the array would be used. Unfortunately, because the annuli are etched in the AlGaAs DBR surface prior to bonding, there is no way to control exactly how the mirror wafer will align to the active regions when the wafers are bonded together. Thus, a way to ensure that each wavelength laser has an air-gap annulus aperture guide with the right V-parameter was needed. The solution is to etch four different annulus depths in repeating columns on the wafer surface. In this way each row of annuli contains all four etch depths. This concept is shown in Figure 4.23. The key is to keep

the pitch of the rows and the repeating column pattern significantly smaller than the 250-μm pitch of the different laser regions and the 1-mm pitch of the integrated active regions. Then, at least one correct air-gap annulus aperture will be available for each laser in the array.

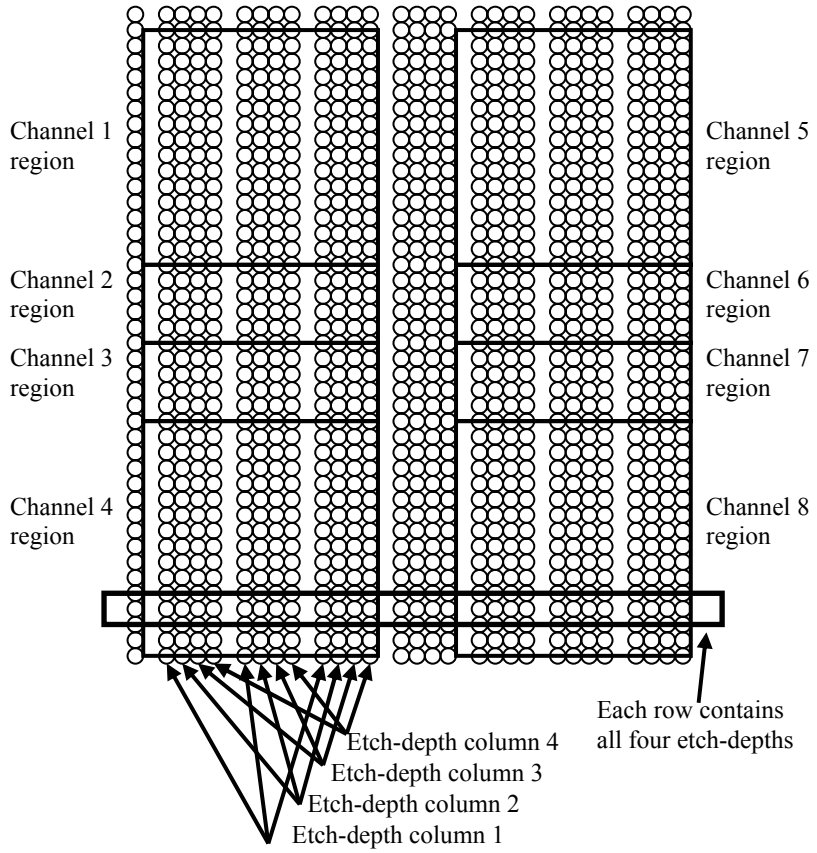

Figure 4.23. Schematic showing the technique to ensure the correct index guide design (four available) is available for each VCSEL wavelength region in the final structure. The circles represent air-gap annuli etched in the GaAs DBR wafer surface and bonded to the two VCSEL active regions already integrated by nonplanar wafer bonding.

The Vertical program was used to determine the correct etch depth for each column of annuli so that each of the eight VCSELs had at least one air-gap

aperture that would give a V-parameter of about 3.5. For accuracy, the four etch depths required are calculated after the epitaxial material is grown and the precise structure thicknesses have been predicted using Vertical. Table 4.6 is the design table used in the CWDM arrays fabricated for this work. Based on the simulations, etch depths of 32, 38, 44, and 50 nm were selected to provide the required modal confinement for each VCSEL element in the array.

Nominal Wavelengths (nm)									
Index depth (nm)		1610	1590	1570	1550	1530	1510	1490	1470
R1	32	2.99	2.75	2.51	2.28	2.21	1.95	1.73	1.54
R2	38	3.64	3.39	3.14	2.89	2.93	2.57	2.32	2.1
R3	44	4.3	4.05	3.79	3.55	3.52	3.24	2.97	2.73
R4	50	4.99	4.74	4.48	4.23	4.24	3.94	3.67	3.41

Table 4.6. V-parameters calculated for CWDM VCSEL array elements for the four etch depth annuli selected. The shaded areas are the anticipated depths required for stable, single-mode operation.

Thus, with the use of four different depths of 8-μm annuli, all eight channels of the CWDM VCSEL array can be designed to operate single mode.

4.4 Summary

A detailed design for an eight-channel CWDM VCSEL array has been presented. The array spans from 1470 to 1610 nm with 20-nm wavelength spacing. To support the wide wavelength span of the VCSEL array, fully-oxidized DBRs were designed for the top and bottom mirror of the VCSEL.

The array uses two optically-pumped active regions integrated by nonplanar wafer bonding. The active regions are designed with carrier-blocking layers located between the three periodically spaced quantum wells. The PL peaks of the two active regions are at 1480 and 1560 nm and each active region supports four wavelength channels spanning 60 nm. Superlattice layers are used to trim the active-region thickness to compensate for growth errors and to form the multi-wavelength regions. Modal confinement in the device is achieved by an air-gap annulus aperture etched into the top DBR and located at the wafer bonded interface. The array geometry leads to a total chip size of 1 mm by 1.25 mm. Channels groups 1-4 (1470 – 1530 nm) and 5-8 (1550 – 1610 nm) are spatially separated by 500 μm with an inter-channel spacing of 250 μm.

This CWDM array design has many distinct advantages over other approaches. Through the use of two active regions to span the wide wavelength range, more uniform gain can be maintained across all wavelength channels and for a wider temperature range. The wafer bonding approach gives unprecedented access to the active region, from both sides. This access allows for the proper tuning of all the wavelengths in the WDM array. This is of critical importance for sources designed for use in WDM applications.

With the application of nonplanar wafer bonding, the design presented here is a true single-chip solution. All the laser positions are lithographically defined, easing the future simultaneous fiber coupling of the array elements.

The use of optical pumping has been used to demonstrate the design approach, but much of this design is compatible with electrical pumping [9, 18]. In separate demonstrations, Reference 18 has shown excellent quality long-wavelength electrically pumped, intra-cavity contacted VCSELs fabricated with wafer bonding. Reference 9 has demonstrated high-quality short-wavelength intra-cavity contacted VCSELs with fully-oxidized top and bottom DBRs.

The next chapter will discuss the fabrication of the array design presented here.

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Chapter 5

Device Processing

In previous chapters the nonplanar wafer bonding integration technology was presented and the design of the CWDM VCSEL array has been developed. In this chapter the key process technologies will be discussed and the steps involved in building the overall CWDM chip will be outlined in detail. The exact process steps will be reserved for Appendices A and B.

The ultimate goal of the processing work is to build an optically-pumped, 2-dimensional, coarse WDM VCSEL array. The array is to span 140 nm from 1470 to 1610 nm with eight wavelength channels and precise 20-nm wavelength spacing. The process used was developed to be as simple as possible while still meeting the requirements of the project.

Several fabrication techniques were developed for this work. An InP substrate polishing technique was developed for the backside processed

nonplanar wafer bonding approach. Wafer handling techniques to process 100-μm thick substrates were developed, and an epitaxial surface protection technique was developed to prevent surface damage during backside polishing and wafer thinning. Ultrasonic etching was used to enhance the uniformity and reproducibility of transport-limited wet-chemical etches. For the nonplanar pressure block nonplanar wafer bonding technique, the overall nonplanar wafer bonding process was simplified over the backside processed approach. A technique to align the nonplanar pressure block to the epitaxial wafer was needed and was developed. This technique required the development of a new type of wafer bonding fixture.

In this chapter, critical process technologies will be developed and presented in the approximate order they occur in the actual process. Each section will reference the corresponding detailed process follower in Appendices A and B based on the cross references given in the general process flow shown in Table 5.1. Though the entire process will be presented, the processing aspects novel to this work will be emphasized. These process steps include: the active region and mirror wafer characterization steps, the backside processed and nonplanar pressure block nonplanar wafer bonding process used to integrate the active regions on the bottom AlGaAs DBR, the WDM thickness adjustment etches, formation of the air-gap annulus aperture waveguide structures on the

top AlGaAs DBR surface, and the etching and oxidation steps required to form the fully oxidized mirrors.

Appendix A is the process for a WDM VCSEL array with traditional AlGaAs DBRs fabricated by backside processed nonplanar wafer bonding (see Section 2.2.2 for the laser results). Appendix B is the process for the CWDM VCSEL array with fully oxidized DBRs and nonplanar wafer bonding with a nonplanar pressure block as designed in Chapter 4. The process descriptions in this chapter closely follow the process follower in Appendix B.

Number	Description	Appendix A&B Item Number
1	Characterize material	
2	Nonplanar wafer bond to laterally integrate InP-based active regions onto bottom 6-period AlGaAs DBR material	A-3-17, B-3-18
3	Etch WDM adjustment layers	A-18, B-19
4	Etch air-gap annuli into top mirror surface prior to wafer bonding	A-2, B-2
5	Bond top 5.5-period AlGaAs DBR material to InP-based active regions already integrated on bottom DBR	A-19, B-22
6	Remove GaAs substrate on top DBR side of wafer stack	A-21, B-23,25
7	Polish remaining bottom DBR GaAs substrate to optically pump through	A-20, B-24
8	Etch structure and oxidize DBRs	B-26,27
9	Deposit metal optical-pumping targets	A-22, B-29
10	Deposit 1540-nm AR coatings on both sides of sample	B-30

Table 5.1. Basic process flow table and Appendix A and B cross-reference.

The standard sample size throughout this work was 1 cm by 1 cm, unless otherwise noted. This size is used because of the size limitation imposed by the

wafer bonder furnace diameter. In addition, it is a convenient size to handle and conserves valuable epitaxial material by allowing up to 12 process runs from each 50-mm wafer.

5.1 General Etching Design

The CWDM VCSEL array design and epitaxial structure was designed with process simplification in mind. The compositions in the active-region layers were chosen to simultaneously maximize device performance and ease fabrication. To this end, the InGaAsP material system was chosen for the barriers, quantum wells, and superlattice layers. By using a 1.22-Q InGaAsP composition for all barrier and superlattice layers, it was ensured that these layers could be wet-chemical etched with high selectivity over InP layers [1]. This selectivity is important because selective etching was to be used to remove controlled number of superlattice layers for VCSEL array wavelength control and to etch off entire active-region structures during nonplanar wafer bonding. As the band gap of the InGaAsP layers is made larger, the selectivity of the etch process is reduced because the material behaves more like InP when etched. 1.22-Q InGaAsP is a good compromise between ease of processing and carrier confinement in the quantum wells.

By using the same InGaAsP composition for the barriers and the superlattice layers, only one type of etch process needed to be developed. This

etch is a H_2SO_4:H_2O_2:H_2O (1:1:10) solution that has been cooled down to room temperature after mixing. The etch exhibits 21:1 selectivity over InP and etches 1.22 Q at a rate of about 0.057 μm per minute. The selectivity of this etch is important because 1.22-Q InGaAsP regions as thick as 450 nm are to be etched while stopping on a 15-nm-thick InP carrier-blocking layer. In addition, the InP can be selectively etched with respect to the InGaAsP using an HCl:H_2O (3:1) etch or an even more selective, though slower, H_3PO_4:HCl (3:1) etch [1]. The InP etch rate in H_3PO_4:HCl (3:1) is about 700 nm per minute. By diluting the H_3PO_4:HCl to 9:1, the etch rate drops by a factor of 3. Because the active-region structure (shown in Table 4.4) is essentially just alternating layers of InP and 1.22-Q InGaAsP, the entire structure can be etched using alternating H_2SO_4:H_2O_2:H_2O and HCl:H_3PO_4 etches and etching can be stopped on any layer. The selectivity of the etch process simplifies the etch timing considerably. Typically, minimum required etch times were lengthened by 10% to ensure the entire layer was removed.

In addition to simplified selective wet-chemical etching, the use of an InGaAsP-based active region allowed the active-region structure to be etched using Methane:Hydrogen:Argon (MHA) reactive ion etching (RIE). This etching will be described in a following section.

All processing was done using standard contact lithography and this process will not be discussed in detail. The smallest feature sizes where the air-

gap annuli with an 8-μm center circle. To ensure that the circle was the proper size, vacuum contact was used and the exposure and develop times were carefully selected.

5.2 Wafer Cleaning

Cleanliness of the wafer surface is critical and must be maintained during the course of processing the VCSEL array. In order to maintain the sample cleanliness, a specific surfactant cleaning technique was used. This technique made use of the chemical Tergitol, a surfactant, to remove particles from the wafer surface and prevent particles from adhering.

Particles appear during the material characterization steps when the wafers are cleaved and transported outside the clean room for PL and reflectivity measurements. Particles also appear after the InP substrate remove steps due to undercut of other InP epitaxial layers exposed at the edge of the sample. The undercut causes thin epitaxial layers to protrude from the edges of the sample. If care is not taken, these thin layers can flake from the edge of the sample and bond to the wafer surface. The bonding forces are often so strong that they cannot be removed. To prevent the pieces from flaking off during subsequent processing, they are intentionally removed with the aid of the Tergitol solution. The solution keeps the particles from adhering to the wafer and allows the flakes

to be rinsed away. Particulate generation is particularly common after the InP substrate removal step of nonplanar wafer bonding. The epitaxial material spanning the 200-μm wide bending accommodation regions is only about 1-μm thick. Such thin material can break off prior to intentionally being removed by the etch-back step. If it breaks off during photolithography, it can be problematic. To prevent this, the membranes can be intentionally removed using the Tergitol cleaning technique.

The technique specifically uses a combination of airbrush cleaning and nylon swab cleaning. About 5 drops of the Tergitol chemical are dissolved in one liter of deionized (DI) water. This solution can then be airbrush sprayed onto the sample. The mild pressure removes unwanted particles, and the Tergitol prevents them from sticking before being washed away. With the aid of a nylon brush wetted with Tergitol, more stubborn particles can be removed. After cleaning, the sample is thoroughly rinsed in running water to remove the Tergitol solution.

The Tergitol cleaning technique is used for all cleaning steps before and after wafer bonding, and whenever the sample has been removed from the clean room. It is also used after photolithography and immediately prior to the patterned wet-chemical etches used in forming the steps for nonplanar wafer bonding and the etch-back steps as well as the WDM superlattice adjustment etches. Doing so prevents unwanted particles from masking the surface to be

etched and allows the etched areas to remain clean and flat - a requirement for all subsequent wafer bonding steps.

5.3 Wafer Characterization

Prior to beginning any device processing, basic material characterization steps must be completed. The two main purposes of these steps are to ensure the material meets the device requirements (PL and thickness), and to determine the precise material thicknesses to complete the Vertical device simulation. The precise thickness of the active region and the mirrors allows the prediction of the final lasing wavelength of the completed VCSEL structure. This is particularly important for WDM devices that must operate at specific wavelengths. With an accurate VCSEL simulation based on the measured thickness of the grown material, the proper number of superlattice thickness adjustment layers can be removed from the active region prior to bonding. In this way, the operating wavelengths of the CWDM VCSEL array can be brought into the range allowed by the application specifications.

5.3.1 PL Characterization

The first step in the material characterization process is the testing of the photoluminescence across the entire 50-mm active-region wafer. In order to accomplish this task, an automated PL measurement system was built. The

system, shown in figures 5.1 and 5.2, uses a microscope to deliver 780-nm and 980-nm diode laser pump light to the wafer and collect the generated photoemission from the wafer. The photoemission is then delivered to a grating based spectrometer and the spectrally resolved photoemission intensity is measured. The two diode pump lasers are free-space coupled into the system and one laser is used at a time. The 980-nm pump laser was used exclusively for this work. The pump light can be delivered to the sample through one of three different microscope objectives and pump spot-sizes of 3, 5, and 15 μm are achieved. The spectrometer uses a 512 element InGaAs detector array to detect the light diffracted off the grating, thus allowing for rapid spectral measurements as short as 40 ms. The spectrometer can be configured to use any of three available gratings that are mounted on a turret inside the machine. By selecting the appropriate grating, each PL measurement can give data over a 125-, 250-, or 500-nm wavelength span. The wafer itself is mounted on a motorized two-axis stage that can move with 1-μm accuracy. With the system, about 1500 PL measurements can be made per hour, allowing a full 50-mm wafer to be PL mapped with 2000 data points in about 80 minutes. The entire system is controlled by a LabVIEW program.

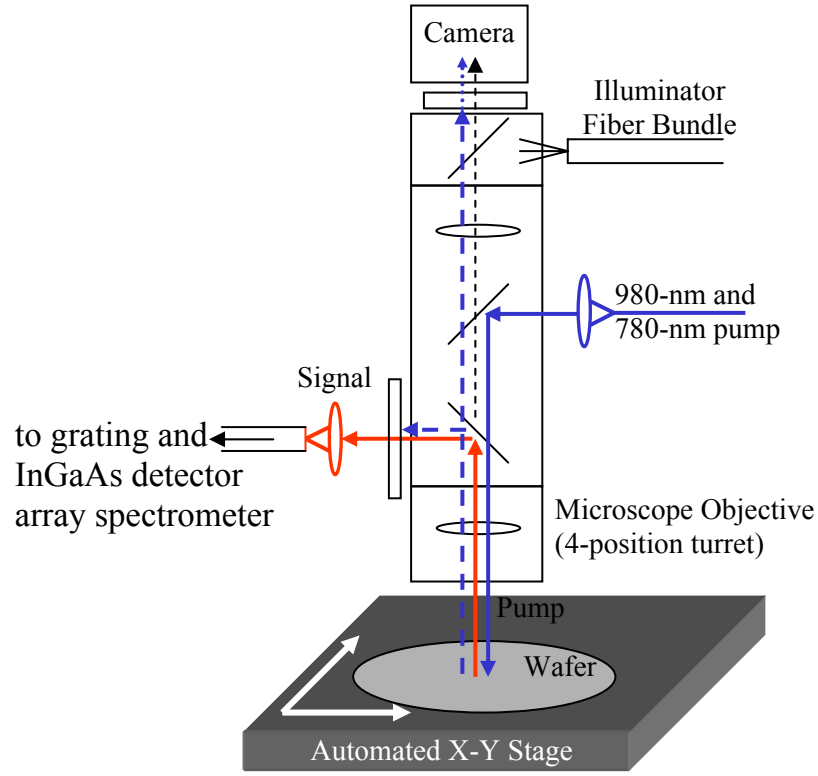

Figure 5.1. Schematic of PL collection system

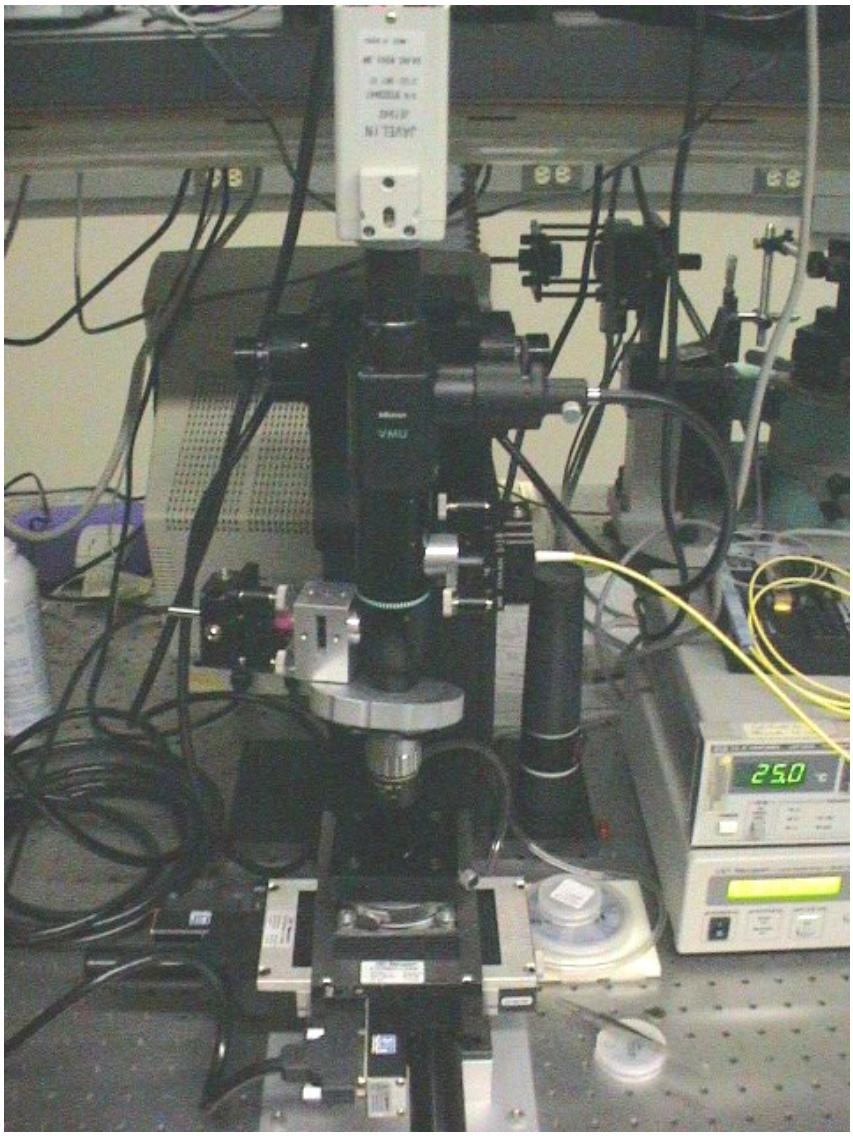

Figure 5.2. Photo of PL collection system.

Using the PL measurement system built, the active-region wafers from the material supplier were characterized. The critical wafer parameter is the peak wavelength of the PL and the uniformity of the peak wavelength across the wafer surface. Because two active regions are grown in a stack, only the top active region can be fully characterized in this way. It is assumed the PL

uniformity of the top active region will be similar to that of the bottom active region. The result of the wafer map is shown in Figure 5.3. Here, the edge data has been removed. It is clear from the figure that the majority of the 50-mm diameter wafer has its peak PL at 1560 +/- 15 nm. To test the shape and intensity of the PL, individual data points near the center of the wafer were measured. Figure 5.4 shows the PL from the center of the wafer. The bump in the PL spectrum near 1475 is from the bottom active region. Figure 5.5 shows the PL spectrum measured after the top active region was etched off a small region of the center of the wafer. The process used to remove the top active region will be discussed in the nonplanar wafer bonding section. With PL values of 1557 nm and 1475 nm at the center of the wafer, both active regions were very close to their target wavelengths of 1560 nm and 1480 nm.

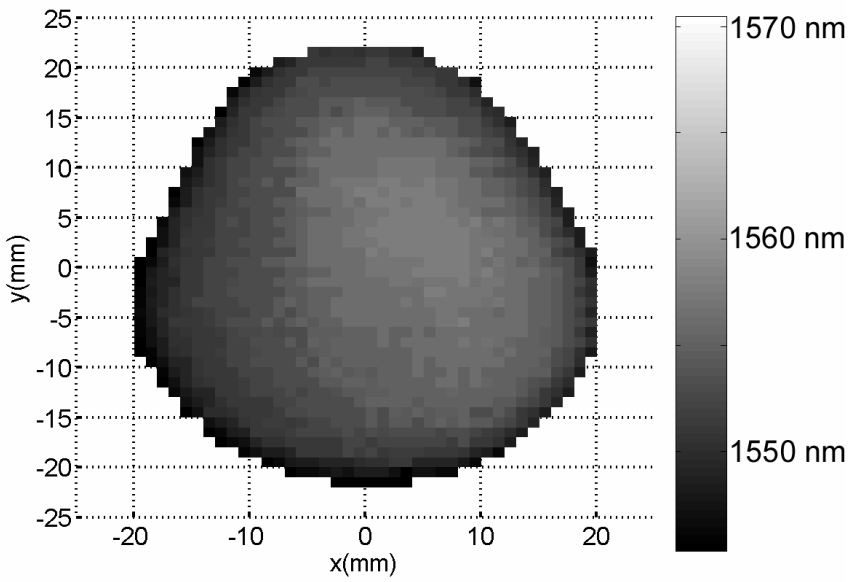

Figure 5.3. PL peak wavelength map from 50-mm double active-region stack wafer (number 0306266-C).

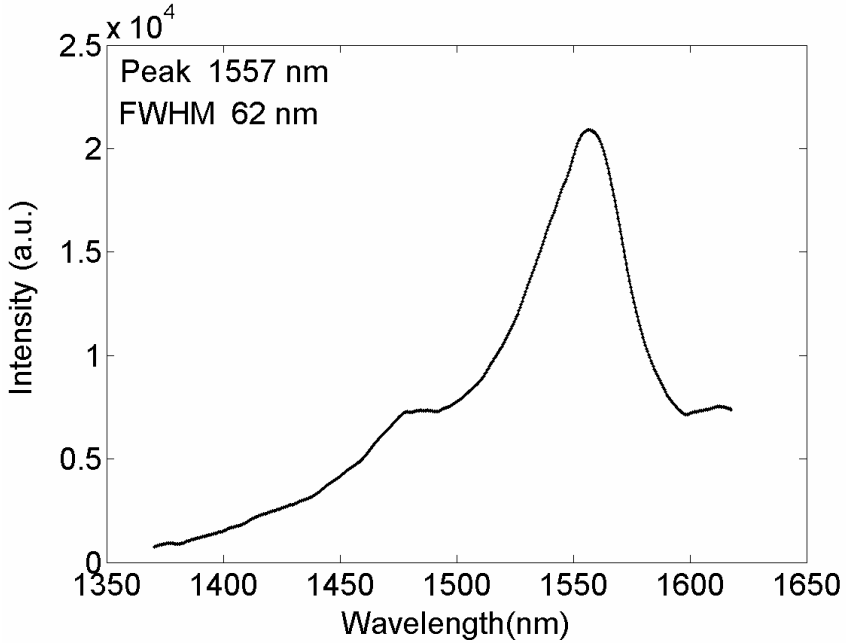

Figure 5.4. PL spectrum of the top active region. Measured from the center of the double active-region stack wafer. The peak near 1620 nm is from the InGaAs etch-stop layer located below the active region.

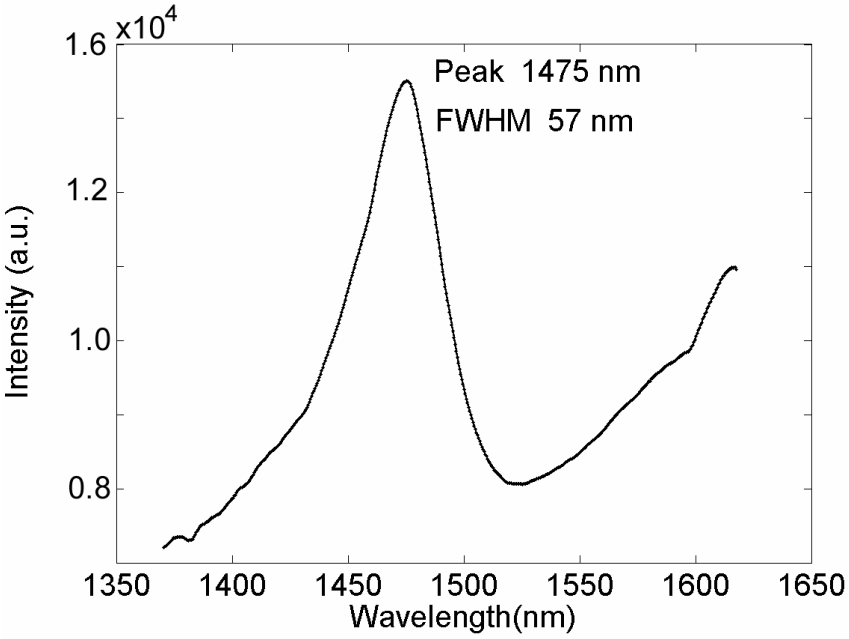

Figure 5.5. PL spectrum of the bottom active region. Measured from the center of the double active-region stack wafer by etching off the top active region. The peak near 1620 nm is from the InGaAs etch-stop layer located below the active region.

5.3.2 Thickness Characterization

After checking the PL position and uniformity of the active region, the next step is to measure the thickness of the InP-based active region and the GaAs-based mirror material. This concept was discussed at length in Chapter 4, and section 4.1.2 discusses the reflectivity measurements conducted on the as-grown DBR material and section 4.2.2 discusses the cavity length measurements conducted on the active-region material. Once these measurements have been made, the simulated reflectivity is fit to the measured reflectivity using Vertical and assuming all layers are off by the same percentage. As discussed in section 4.2.2, the fit of the active region determines how many total superlattice layers need to be removed from each side of the active region. Using Vertical, the optimum number of fine-pitch topside and course-pitch backside superlattice layers to remove can be determined. The goal is to keep the electric-field standing wave centered on the quantum wells despite the growth-rate error. It is also possible for the growth rate to drift during the growth of the stack so each of the two active regions must be individually measured. Table 4.4 gives the detailed epitaxial structure.

The active-region characterization process begins by cleaving two small pieces (4x4 mm) from the center of the wafer. Because the standard processed

sample size in this project was always 1 cm by 1 cm, cleaving the wafer is required and removing the two 4 by 4 mm pieces from the center of the wafer is simple. Each of the pieces has the epitaxial material of both active regions in a stack on the sample surface. In order to measure each active region's thickness, each must be transferred to a separate glass slide for reflectivity measurements. The first sample is mounted directly to the glass slide using wax (MWH135 from South Bay Technology - SBT) so that the top grown active region is now facing down toward the glass. After mounting, the substrate is wet-chemical etched using an $HCl:H_2O$ (3:1) etch. The etch takes about an hour to remove the entire 385-μm thick substrate. The etch stops on the 200-nm thick InGaAs etch-stop layer. The InGaAs layer is removed using a 40-sec etch in $H_2SO_4:H_2O_2:H_2O$ (1:1:10). The bottom grown active region, which is now on top, is completely removed using alternating H_3PO_4:HCl and $H_2SO_4:H_2O_2:H_2O$ etches. The last 20-nm thick InGaAs etch-stop layer separating the two active regions is removed and all that remains wax bonded to the glass slide is the top-grown active region. Similar processing is used to mount the bottom-grown active-region epitaxial material to a glass slide, except in this case the top-grown active region is removed first.

Once both active regions are mounted to glass slides, their reflectivity profile is measured as discussed in section 4.2.2. The reflectivity spectrums from the active-region wafer used in the final CWDM VCSEL array of this

work are shown in Figures 5.6 and 5.7. Both active regions were slightly long. The top, 1560 nm PL active region was 1.08% long (17 nm) and the bottom 1480 PL active region was 1.33% long (20 nm). Based on these values, it was determined that one additional coarse superlattice layer would be removed from each active region after the nonplanar wafer bond step (for at total of two each of the fine- and coarse-pitch superlattice layers). The removal sequence will be discussed in a following section on nonplanar wafer bonding.

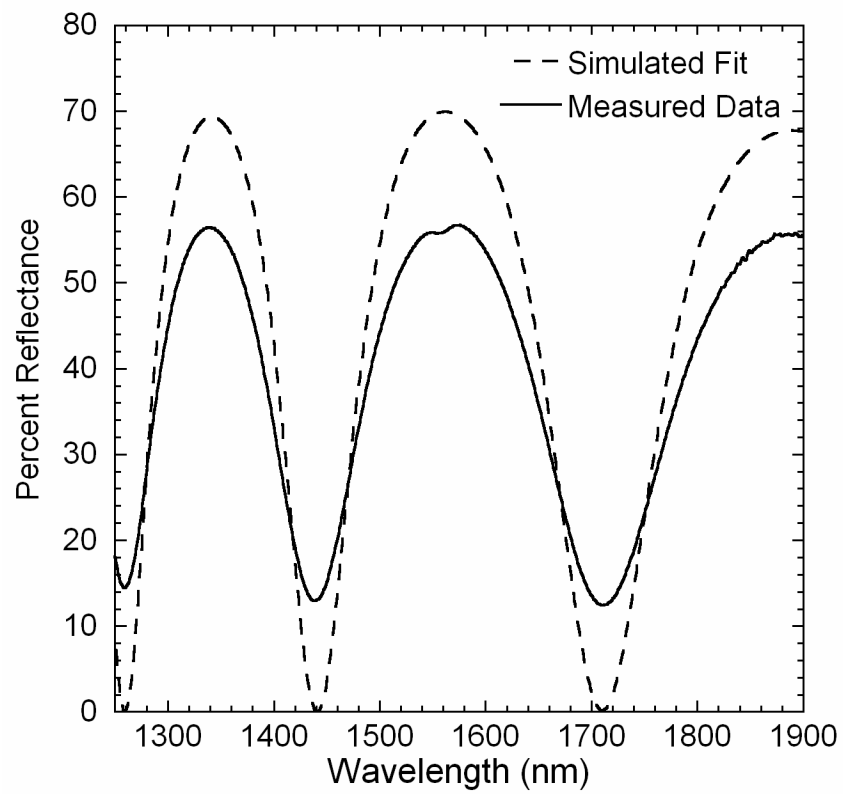

Figure 5.6. Top active region measured and simulated reflectivity spectrum. The fit shows the structure to be 1.08% long.

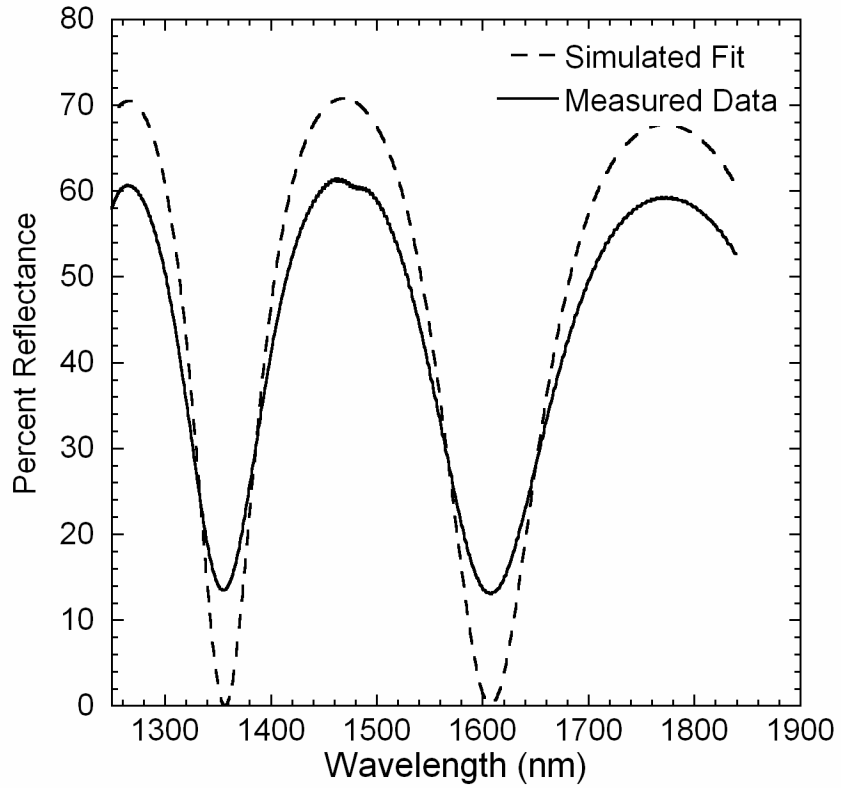

Figure 5.7. Bottom active region measured and simulated reflectivity spectrum. The fit shows the structure to be 1.33% long.

Section 4.1.2 discusses the reflectivity measurements conducted on the as-grown DBR material to determine the grown rate error. Because the DBR is broad band and has a nearly flat phase response, the VCSEL array operating wavelengths are not strongly dependent on this measurement. Thus, although the top and bottom mirrors were measured to be 9 and 16-nm short (0.6 and 1%), respectively, these errors have only a minor impact on the lasing wavelength of the device. The actual wafer pieces to be bonded to the active region are measured and fitted as shown in section 4.1.2.

5.4 Backside-Processed Nonplanar Wafer Bonding Process

This section describes the process steps to complete the nonplanar wafer bonding by backside processing. Chapter 2 discusses this technique in detail and should be referred to. Though two nonplanar wafer bonding techniques were developed, they share many features in common. The etching of the steps on the front of the wafer to expose the different active regions is the same, as is the etch-back process required to leave only the desired epitaxial layers after bonding the active regions to the bottom AlGaAs DBR material. The key difference is in the absence of backside processing in the nonplanar pressure block approach, and the absence of the alignment of the wafer to the pressure block required in the backside processed approach. The two approaches are different enough that they will be described separately and the nonplanar pressure block approach will be described in a later section. The nonplanar pressure block approach was selected for the final VCSEL array.

5.4.1 Etching the Thickness Adjustment Layers

The first step in the nonplanar wafer bonding process for CWDM VCSEL arrays is the removal of the proper number of top active-region superlattice thickness adjustment layers required for growth-rate error correction. In this case, as was discussed in section 4.2.2 and 5.3.2, because the growth is only slightly long, only two of the fine-pitch superlattice adjustment layers on the top of the wafer

surface need to be removed. This is done with a combination of a 10-second H_3PO_4:HCl (3:1) etch, followed by a DI water rinse and a 10-second H_2SO_4:H_2O_2:H_2O (1:1:10) etch, DI water rinse and N_2 dry. Now the top active region has had one side of its growth-rate error correction layers etched.

5.4.2 Forming the Etch-Step

The next step is to step-etch the surface of the sample to expose a different active region on the surface of each step level. This is done using photo lithography to mask stripes of the wafer surface, followed by etching the wafer using alternating H_3PO_4:HCl (3:1) and H_2SO_4:H_2O_2:H_2O (1:1:10) etches until the InGaAs etch stop layer that divides the two active regions is reached. Once this layer is reached, it too is removed to reveal the top surface of the bottom active region in the area that was not masked by photoresist. Now, with the bottom active region exposed and the top active region still protected by the photoresist, the two top fine-pitch superlattice layers of the bottom active region can be removed. A wafer cross-section is shown in Figure 5.8. Figure 5.9 is photo of the wafer surface and shows the alignment target used. The horizontal groove leading from the edge of the raised top active-region stripe in the figure is to allow fluid to escape from around the target during wafer bonding.

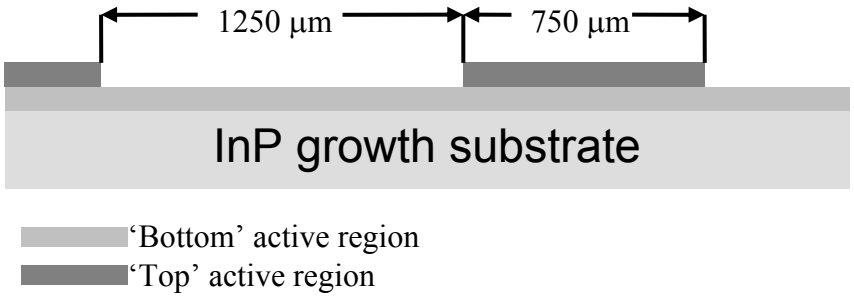

Figure 5.8. Cross-section schematic of the wafer surface after the step-etch process and etching the top superlattice layers on each active region.

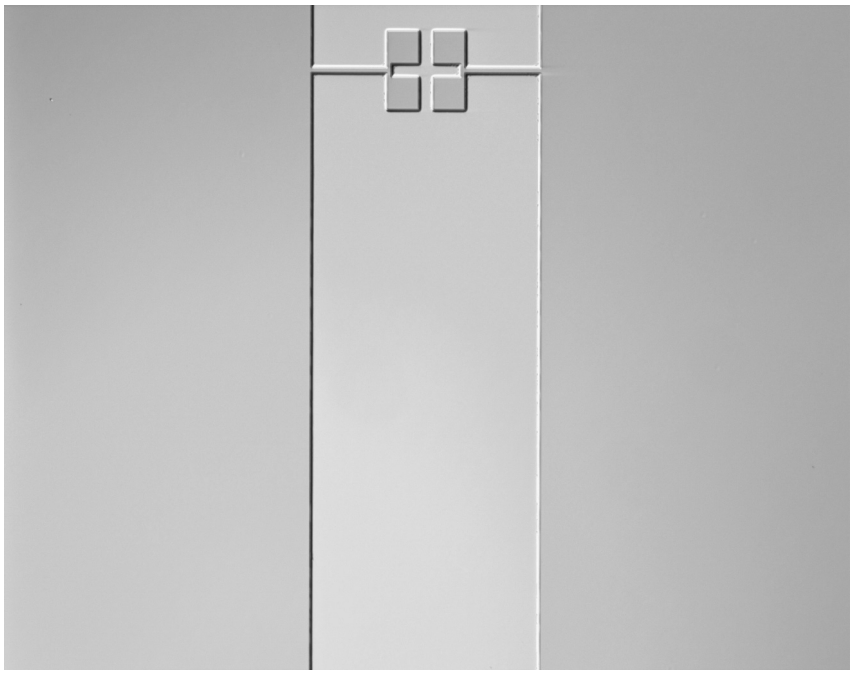

Figure 5.9. Photograph of small area of the sample surface after step etching. The center, raised region, is the top active region. The cross is an alignment target.

5.4.3 Polishing the InP Active-Region Wafer

In order to process the backside of the InP active-region wafer, the wafer must be thinned and polished to a thickness of 100 μm. A Bromine:Methanol chemical-mechanical polish was developed based on Reference 2. Techniques

were developed to improve wafer flatness, protect the epitaxial surface from scratches, and handle the substrate without breakage during and after the thinning and polishing process. Because the sample is hand polished, care is taken to maintain the flatness of the sample. This flatness is critical in wafer bonding to ensure uniform pressure during bonding. Also because the wafer is thinned to 100 μm, care is taken to keep the wafer from breaking during the backside processing steps. With several backside lapping and polishing steps, great care is also taken to prevent the sample surface from becoming scratched during handling.

First, the sample is Tergitol cleaned and coated with PMGI. PMGI was used to coat the epitaxial surface in order to protect the material from scratches and particle contamination. It is well suited for this because it has a glass transition temperature (above about 180 °C) that is higher than that of the MWH135 wax (about 135 °C) used later in the process, and PMGI does not dissolve in the acetone, as the wax does. The surface of the sample is coated with PMGI and the PMGI is planarized by baking the sample at 300 °C for several minutes.

Once the sample surface has been coated with PMGI, it is mounted epitaxial layer side down along with four other dummy InP pieces to a carefully planarized and prepared lapping block. A hand fixture is used for lapping and it is important the lapping block be planarized to the hand lapping fixture so that

each of the five pieces will be the same thickness with minimal wedge shape after lapping. These samples are used later to help maintain the wafer flatness during polishing. Mounting is accomplished using a vacuum mounting fixture on a heated hot plate. Slow cooling is used to ensure a uniform wax thickness below the five samples, an important condition for the wax layer. Excess wax is removed from the lapping block surface prior to lapping. The five pieces of InP are lapped to about 150 μm thick with about 225 μm of material removed. The thickness is not critical so long as the wafer is not thinned past about 125 μm so that at least 25 μm of material can be removed to reach the target thickness of 100 μm. The subsequent polishing step is capable of removing material quickly, but enough material must be removed by polishing to remove all lapping damage. Also, the less polishing time required, the flatter the final sample surface.

After thinning the sample and the four dummy InP pieces, they are carefully removed from the lapping block and cleaned using acetone and isopropyl alcohol (IPA). This cleaning step removes the wax, but leaves the PMGI protective layer over the InP epitaxial layers. Once cleaned, the five thinned pieces are vacuum mounted to glass cover-slips using MWH135 with the lapped surfaces facing away from the glass. The excess wax is removed from the pieces using an acetone spin clean. The five samples and their cover-slips are now vacuum mounted to a 3-inch-diameter glass polishing puck with

the real sample in the middle of the puck and the lapped InP substrate sides facing outward. The wax used to mount the glass cover slips to the glass puck is MWH070 and it has a low, 70 °C, melting point. The low temperature wax was used to prevent the higher temperature wax from melting during mounting and causing wafer movement. It was also necessary because it is more difficult to heat the surface of the 5-mm thick glass puck to melt the high temperature wax. Once mounted, the excess MWH070 wax is removed using heated WaxStrip (also from SBT) in a heated, ultrasound bath. WaxStrip is used to remove the MWH070 wax because MWH070 does not dissolve in acetone. Figure 5.10 shows the configuration of samples on the lapping puck.

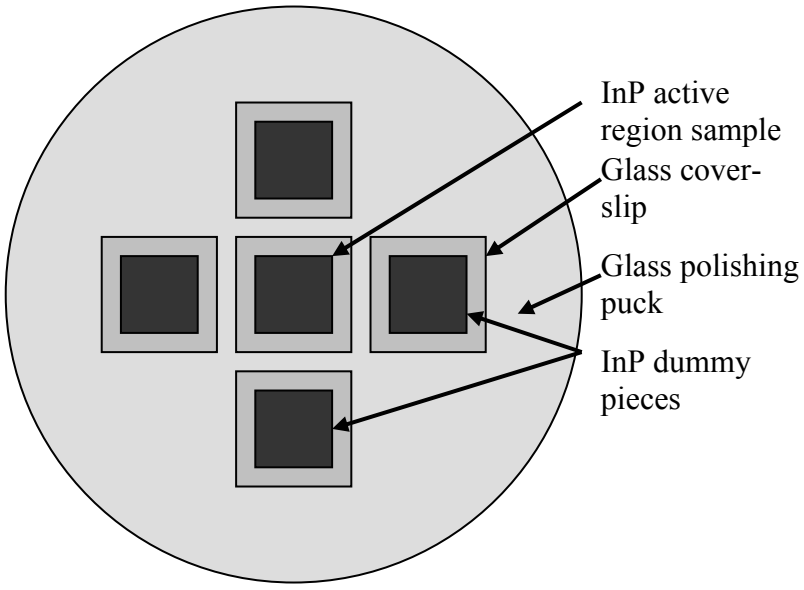

Figure 5.10. Top view of InP active-region sample and dummy pieces mounted to polishing puck.

Once the sample is mounted to the glass polishing puck it is ready to be polished. The polish used is a 1% Bromine:Methanol solution applied continuously to an 8-inch-diameter silk cloth rotating at about 3 Hertz. The material removal rate is about 20 μm per minute. Figure 5.11 shows the design of the Teflon polishing fixture developed to hold the polishing puck during the process. Once the desired amount of material has been removed (based on the estimated removal rate) the polish is slowed by applying a 0.1% Bromine:Methanol solution to the silk cloth for 15 seconds, followed by applying straight methanol to the cloth to slow the etch to a stop. The sample is quickly rinsed to remove any bromine that might remain in contact with the sample. By slowing the etch rate gradually, the evidence of physical material removal is diminished and the sample surface becomes smoother. Measurements show that the center 8-mm by 8-mm area of the polished sample has a post-polishing thickness uniformity of +/- 2 μm.

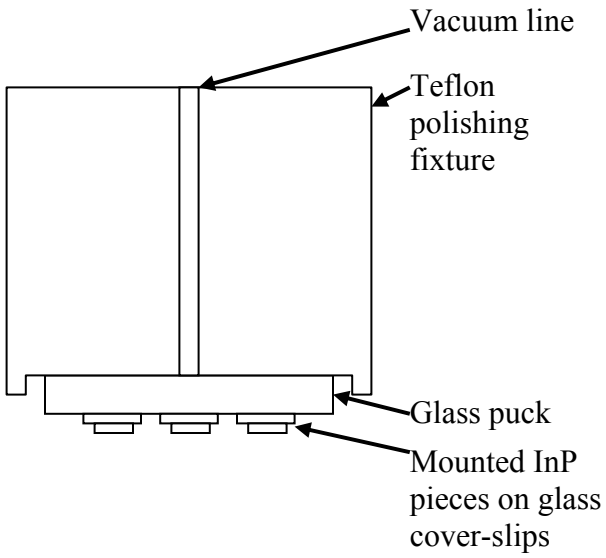

Figure 5.11. Side-view schematic of hand-held Teflon polishing fixture.

After the chemical-mechanical polish, the polished InP sample and dummy pieces are removed from the polishing puck but are left attached to the glass cover slips. The excess low temperature wax is removed using WaxStrip in a heated ultrasound bath. Once the samples are clean, a chemical finish etch is used. This finish etch is a two minute dip in 0.1% Bromine:Methanol and it aids in removing subsurface damage from the polishing process. This solution was selected because more aggressive 1% solutions leave spike defects, likely due to wax residue entering the solution from the exposed area between the sample and the glass cover-slip to which it is mounted. Figures 5.12 and 5.13 show photographs of the polished wafer surface at about 500x magnification (50x objective lens, 10x camera magnification). The finish-etch removes visible mechanical polishing lines. The wafer can be scene to have a wavy surface.

Though the impact of the finish etch is difficult to see from these pictures, its overall effect after subsequent processing is important and will be discussed in the next section. It is important that the glassware and tweezers used for this step be clean and free of wax. Contamination leads to spike etch defects in the polished surface.

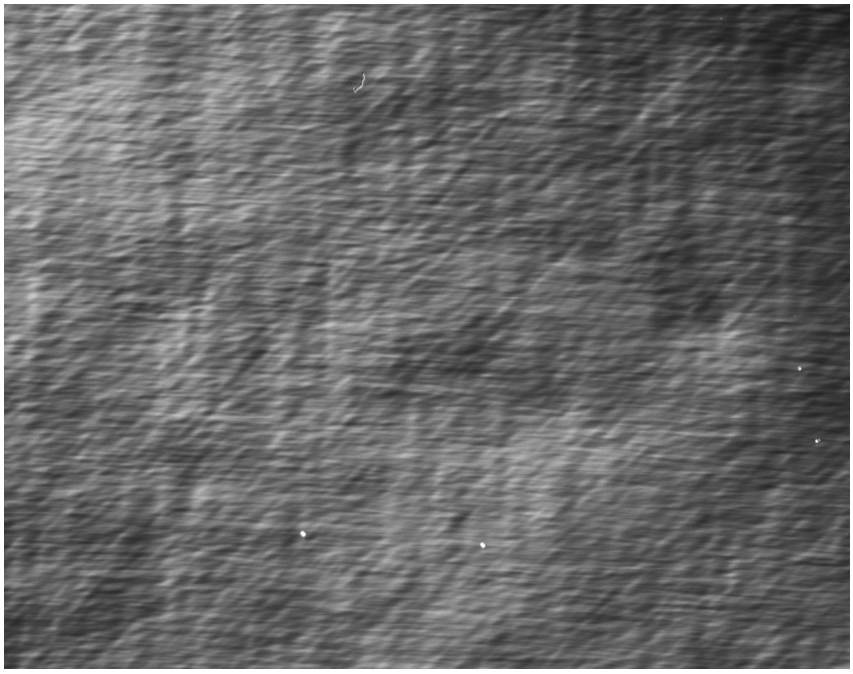

Figure 5.12. Photograph of wafer surface after chemical-mechanical polish (about 500x magnification).

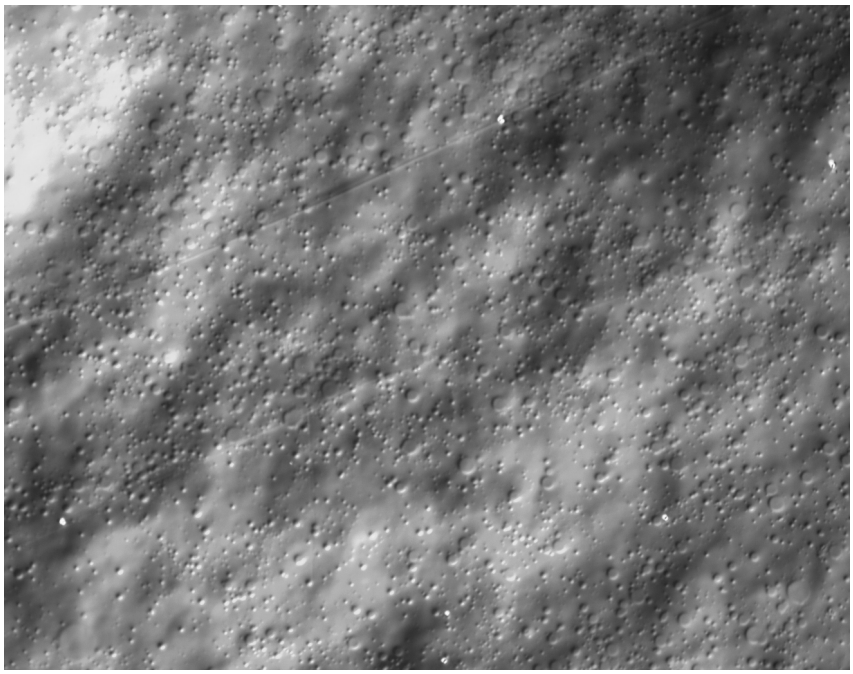

Figure 5.13. Photograph of wafer surface after final chemical polish (about 500x magnification).

5.4.4 Backside Etch Process

After the sample has been polished, it is patterned with the complementary backside etch discussed in Chapter 2. The sample is still attached to the glass-cover slip and is now about 100-μm thick. Infrared alignment is used to align the new backside pattern to the front-side pattern. The depth of the backside etch is critical. It must be nearly identical (less that about 5% error based on experience) for the substrate to bend correctly to promote uniform bonding. The difficulty arises from the non-uniformity of the H_3PO_4:HCl (3:1) etch used to remove the InP material from the newly polished substrate. Regardless of the polish, the etch rate is difficult to control and is very sensitive to the amount of agitation. Because the etch forms phosphine gas bubbles at the surface of the

wafer, the flow of the etchant across the sample varies with proximity to the edge of the wafer and the edge of the photoresist pattern. This bubble flow changes the etch rate and causes non-uniformity. To prevent the bubbles, vigorous agitation can be used, but the non-repeatability of manual agitation leads to varying etch rates from sample to sample and the fluid dynamics across the sample leads to etch depth variability across the sample. Figure 5.14 shows a patterned, factory polished InP wafer after a total of 3 minutes of etching with H_3PO_4:HCl (3:1) using no agitation and holding the sample flat. The etch rate is about 0.7 to 0.8 μm per minute, depending in the distance from the mask pattern and sample edge. The etch waviness is clearly visible. In addition, a circular structure is visible in the upper left formed by etch masking from a gas bubble formed during etching.

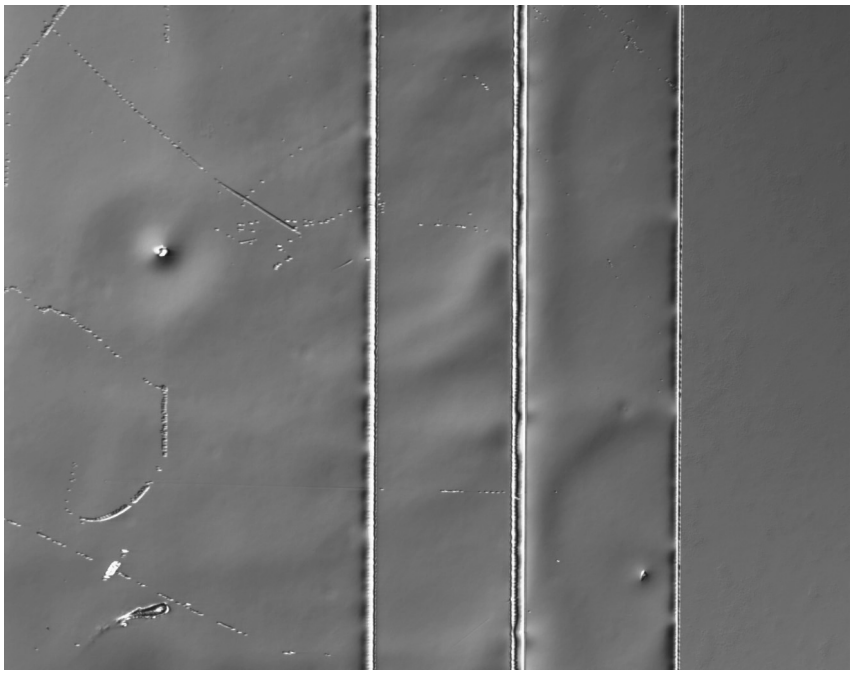

Figure 5.14. Photograph of the surface of a factory polished wafer after patterning and etching twice with H_3PO_4:HCl (3:1) for a total of 3 minutes. The etch pattern is actually a step etch and the approximate depth of the regions from left to right is 3, 2, 1, and 0 μm. The area size shown is about a 2 mm square.

To improve upon this uniformity, ultrasonic etching was used to create reproducible and uniform agitation across the sample surface. Figure 5.15 shows the result of the etching with low-power ultrasound. The etch was 3 minutes long and the same H_3PO_4:HCl (3:1) solution etches InP at a rate of 1.25 μm per minute. Though some structure is visible in the etch pattern, the waviness is gone and the etch rate was no longer dependent on the amount of stirring (additional ultrasound energy did not change the etch rate). This etch was selected for the backside processing to allow the etch depth to be controlled to match the front-side step heights for uniform nonplanar wafer bonding.

Figure 5.15. Photograph of a 3.75-μm deep etch with H3PO4:HCl (3:1) in ultrasound. The etch rate was 1.25 μm per minute. The area size shown is about a 2-mm square.

Using the developed H_3PO_4:HCl (3:1) ultrasonic etch, the manually polished sample surface can be controllably etched. The etch process reveals the true quality of a substrate polish by exposing subsurface damage caused during wafer polishing. Figure 5.16 shows the result of the patterned backside ultrasonic H_3PO_4:HCl (3:1) etch after manual polishing if the final chemical finish etch is not used. The line from left to right in the center of the sample separates the top polished and etched region from the bottom polished and masked region. The etched area has large defect areas and is not smooth. Figure 5.17 shows the same H_3PO_4:HCl (3:1) ultrasonic etch on a manual polished sample that has undergone a finish etch. Though the surface is not smooth, significant additional etch defects are not present.

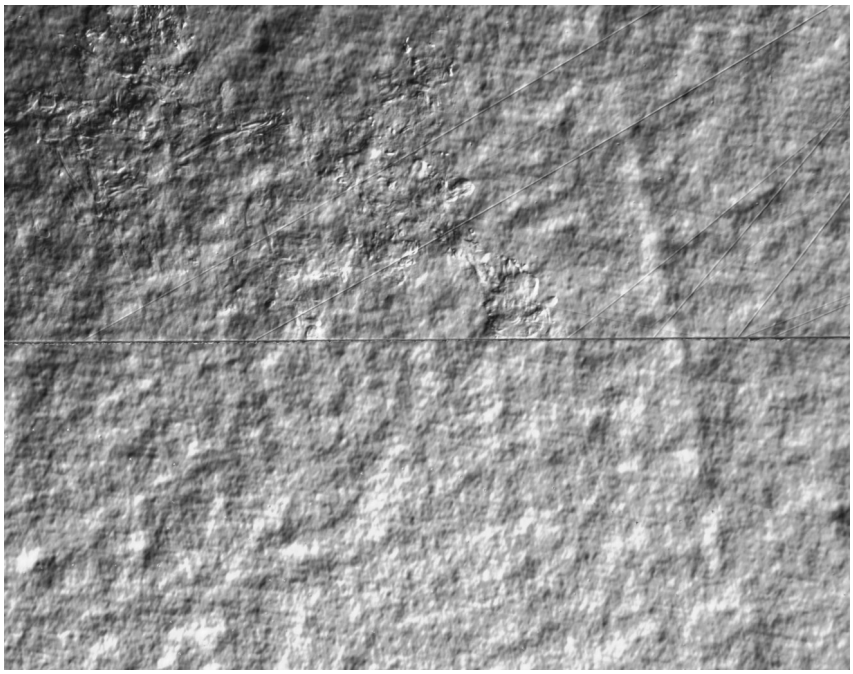

Figure 5.16. H3PO4:HCl (3:1) etched, manually polished sample when chemical finish-etch is skipped. The top half of the picture is the etched region and has large rough areas superimposed on the texture of the polished surface (about 500x magnification).

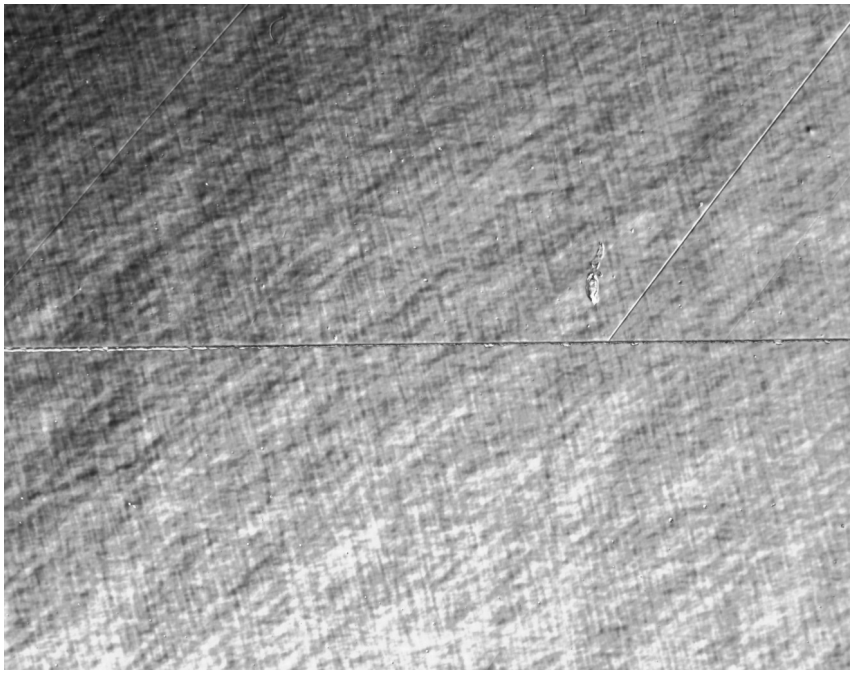

Figure 5.17. H3PO4:HCl (3:1) etched, manually polished sample when chemical finish-etch is used. The top half of the picture is the etched region and few additional rough areas superimposed on the texture of the polished surface (about 500x magnification).

Once the backside of the sample has been etched (about 1 minute to match the 1.2-μm-thick step height on the front of sample), the sample is carefully demounted from the glass cover slip by soaking the sample in acetone. Once the sample is separated from the cover slip, the PMGI protective coating is removed by hot 1165 (NMP) stripper. Having kept the sample surface clean during the previous processing steps, the PMGI is removed and the sample is ready to undergo wafer bonding to the AlGaAs bottom DBR of the VCSEL structure.

5.4.5 Nonplanar Wafer Bonding Step

The wafer bonding procedure for backside processed nonplanar wafer bonding is identical to traditional planar wafer bonding, except that the InP sample is cleaned for particulates prior to the backside processing steps. Also, because the sample surface is not flat and bending accommodation regions exist, the use of channel etches on the wafer surface for fluid escape is not necessary. Reference 3 provides a good background for the wafer bonding approach used here, though minor changes do exist. This section will review the procedure that was used throughout this work.

The samples are cleaned using the Tergitol surfactant cleaning technique described in Section 5.2. The clean removes particle contamination from the wafer surface. Following the particle clean, the wafers are subjected to an oxygen plasma descum etch to remove organic contamination, and then etched in buffered hydrofluoric (HF) acid to remove surface oxides.

Having cleaned the epitaxial layer surfaces of the AlGaAs bottom DBR wafer piece and the step-etched InP active-region wafer piece, the samples are prepared for wafer bonding by using a one-minute NH_4OH dip to modify the wafer surfaces to be hydrophilic, a requirement for successful semiconductor direct wafer bonding. The samples are removed from the NH_4OH and transferred to methanol while maintaining a surface tension bubble of NH_4OH over the wafer surface to protect it from air oxidation and further contamination. The methanol is used to rinse the NH_4OH from the wafer surface. The samples are then transferred from the methanol and placed adjacent to each other on a clean room grade absorbent cloth. A surface tension bubble of methanol is maintained on each sample. The methanol layer serves two purposes; it keeps air from reaching the wafer surfaces, and it aids in aligning the wafer surfaces together for bonding. When the InP piece is flipped over onto the GaAs piece, so that their epitaxially grown layers are in contact, the surface tension of the methanol layers pulls the 1-cm-square samples into alignment with each other

and holds them together. This aids in handling the wafers and transferring them to the wafer bonding fixture.

For this work, a new modified wafer bonding fixture was used. The fixture is made of densified and purified graphite. The fixture made use of a removable sleeve to keep the wafers in alignment with each other and aid in placement of the wafers and the pressure application dome. By removing the sleeve, the fixture surface can be polished to a mirror flat finish before use; a requirement for reproducible and uniform pressure application. Figure 5.18 shows an exploded schematic view of the graphite wafer bonding fixture. Pressure is applied by tightening the graphite nuts. The torque on these nuts translates to a fixed amount of force on the wafer pieces. The force, in Newton units, is given by 343 times the torque in lb-in. The torque used is 0.45 lb-in for a pressure of about 1.54 MPa on the 1-cm-square sample.

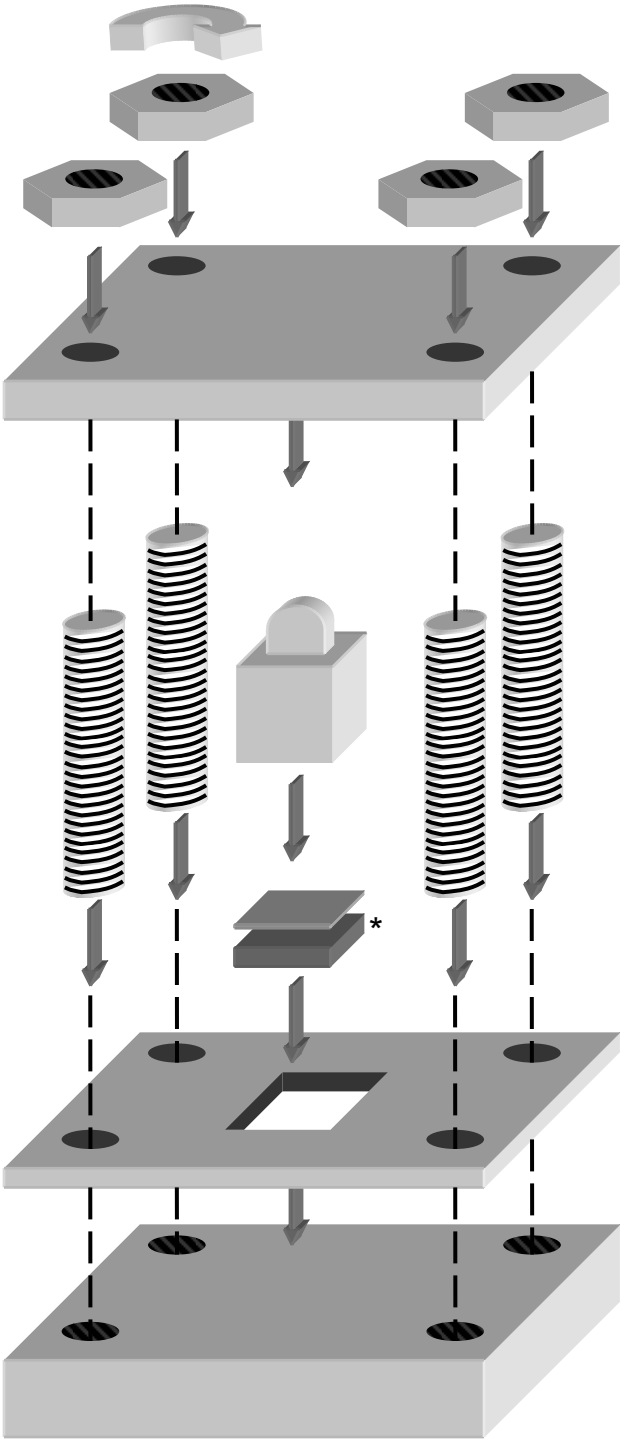

Figure 5.18. Exploded schematic view of graphite wafer bonding fixture used for traditional planar wafer bonding and backside processed nonplanar wafer bonding. The InP and GaAs wafer pieces to be bonded are shown in the center, marked with a asterisk (*).

Once the wafer pieces are loaded into the graphite fixture and pressure is applied, the fixture is loaded into a rapid temperature-ramp tube furnace. The tube is evacuated and refilled with flowing nitrogen. The nitrogen flow rate is 2 standard cubic liters per minute and the tube furnace diameter is 2 inches. The temperature in the furnace is ramped at 85 per minute to 600 °C and is held constant. After 30 minutes the temperature is ramped to 300 °C at 10 °C per minute and allowed to freefall to room temperature. Typically the fixture is removed from the furnace below 100 °C. After removal from the furnace, the samples, are now atomically bonded to each other and can be removed as a single piece from the graphite fixture.

Nonplanar wafer bonding attaches the step-etched InP wafer surface to the AlGaAs DBR surface. The backside processed step-pattern promotes the bending of the wafer when pressure is applied. Figure 5.19 shows a profilometer scan of the backside of the InP wafer after the nonplanar wafer bond and before the InP substrate is removed. The deformation of the bending accommodation regions is visible in the scan. As the wafer bends in these regions, the top surfaces of the backside step levels are brought into line with each other. The original backside and front side step heights were about 12000 Angstroms.

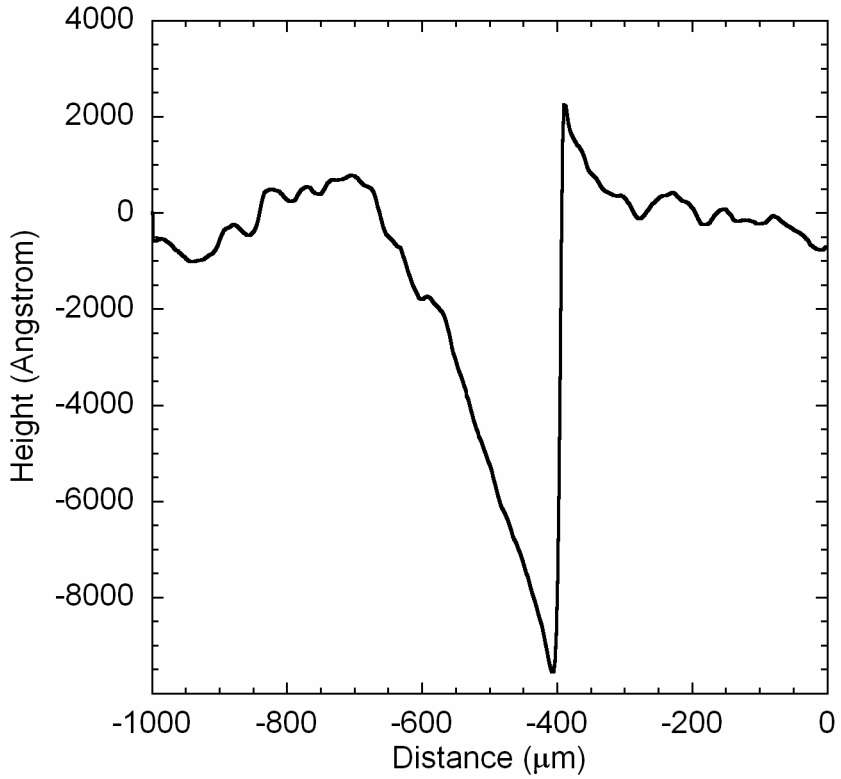

Figure 5.19. Profilometer scan across the backside etched steps of the nonplanar wafer bonded InP substrate. The bending accommodation region is visible as the different step levels are brought into line on each side of the region.

5.4.6 InP Substrate Removal

After nonplanar wafer bonding is complete, the InP substrate is removed. This is accomplished using an etch solution of HCl:H_2O (3:1) and takes about 20 minutes. The etch stops on the 200-nm-thick InGaAs etch-stop layer that was grown first on the wafer prior to growing the active-region stack. This etch-stop layer is removed using a minimum 40 second long H_2SO_4:H_2O_2:H_20 (1:1:10) etch. The InGaAs layer was designed to be thicker than the minimum required to aid in lifting off (via undercutting) debris that can attach itself to the surface

of the wafer during the InP substrate removal. The Tergitol cleaning description in section 5.2 discusses this debris removal in more detail.

5.4.7 Etch Back of the Excess Epitaxial Layers

After removing the InP substrate and the InGaAs etch-stop layer, the nonplanar wafer bonding process in nearly complete. All that remains is the removal of the first, bottom-grown, active region as shown in Figure 2.6(b). Because nonplanar wafer bonding has inverted the step-etched active regions, the bottom-grown active region is now above the top-grown active region. This excess active region can be removed in a fashion exactly analogous to section 5.4.2 were the top step level was formed. This etch-back step is common to both types of nonplanar wafer bonding developed in this work. The region of the wafer that is only one active region thick (referred to as the bottom active region prior to wafer bonding) is masked with photoresist. Then, alternating H_3PO_4:HCl (3:1) and H_2SO_4:H_2O_2:H_2O (1:1:10) etches are used until the InGaAs etch-stop layer that divides the two active regions is reached. Once this layer is reached, it too is removed to reveal the surface of what was referred to as the top active region in the stack prior to wafer bonding. Because the protective photoresist strip is only 750 μm wide, the bending accommodation regions that divide the two regions are also etched away in this process. What remains after this etch-back step are just two stripes of active-region epitaxial

material laterally integrated on the AlGaAs DBR transfer substrate as shown in Figure 5.20.

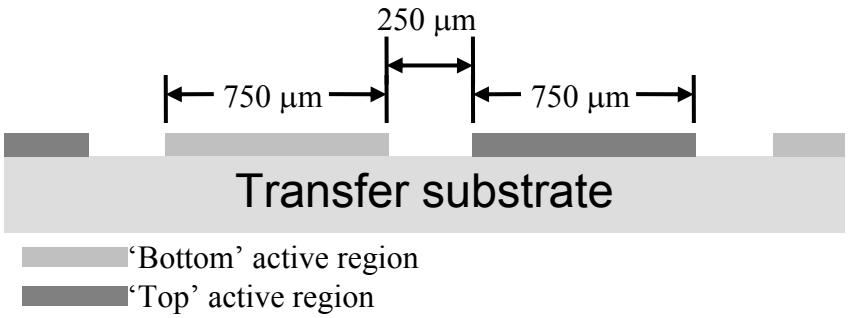

Figure 5.20. Schematic of GaAs wafer surface after nonplanar wafer bonding and etch-back process. Both active regions, originally grown in a stack on an InP wafer, are now laterally integrated on the GaAs wafer surface.

5.4.8 Superlattice Adjustment Etch

The final step in the integration of the two active regions is the removal of the required number of coarse thickness-adjustment layers. As discussed in section 5.3.2, the active regions were grown more than 1% longer than the target growth rate. Thus, it is necessary to remove one extra (two total) coarse superlattice adjustment layers to bring the VCSEL resonance back into the specified wavelength window. These two layers are simultaneously removed from both active-region areas by etching the entire surface of the newly integrated active regions for 10 seconds in H_3PO_4:HCl (3:1), followed by a 10-second etch in H_2SO_4:H_2O_2:H_2O (1:1:10). With this final etch process, two active regions of different design and of the proper thickness are now laterally integrated on the bottom AlGaAs DBR wafer surface.

5.5 Nonplanar Pressure Block Nonplanar Wafer Bonding Process

Nonplanar wafer bonding with a nonplanar pressure block requires almost no backside processing, other than wafer thinning. This is made possible by using a separate pressure block with a nonplanar surface as shown in Figure 2.10(c). The alignment of this pressure block requires an aligned wafer bonding technique. To manage this alignment in this research work, a novel passive alignment approach was developed. This approach wastes active-region wafer material and is not necessary with proper access to an industrial wafer bonder with wafer alignment capabilities.

Many of the steps involved in this approach are the same as the backside processed approach. The epitaxial layer side of the InP active region is still etched to create the step-shaped profile, and the sample is still thinned. There are, however, no further backside processing steps, such as mounting to glass cover slips, polishing and ultrasonic etching. Two additional steps required include the deposition of a SiN_x coating on the surface of the nonplanar pressure block to prevent it from sticking to the backside of the InP active region during the bond step, and lapping the backside of the InP sample after wafer bonding to

remove SiN_x that is transferred due to contact with the nonplanar pressure block during bonding.

The process developed in this section was used to fabrication the CWDM VCSEL array of this work. Appendix B provides specific process details for the steps described here.

5.5.1 Forming the Etch-Step and the Nonplanar Pressure Block

The formation of the etch-step process used in the backside processed approach is modified to allow for the simultaneous fabrication of the nonplanar pressure block. By fabricating the nonplanar active-region wafer to be bonded and the nonplanar pressure block in the same step, it is assured that they can be passively aligned to each other during nonplanar wafer bonding. It is also assured the step heights on the nonplanar pressure block will be identical to those on the surface of the step-etched active-region sample to be bonded.

Figure 5.21 shows the approach selected. The concept uses a 1-cm-wide and 2-cm-long piece of the InP active-region wafer to simultaneously fabricate the step-etched active-region surface and the nonplanar pressure block. One half of the sample is to become the step-etched active-region piece to be bonded. The other half is to become the nonplanar pressure block piece. By fabricating the pieces from the same cleaved piece of active-region material, it is ensured that they will both be exactly the same width. Furthermore, a single mask step

is used to place the ridges for the nonplanar pressure block and the etch-protection stripes of the step-etched active region. Thus, by patterning the two sections at the same time, the precise position of the final etched steps can be maintained with respect to each other and the edge of the sample.

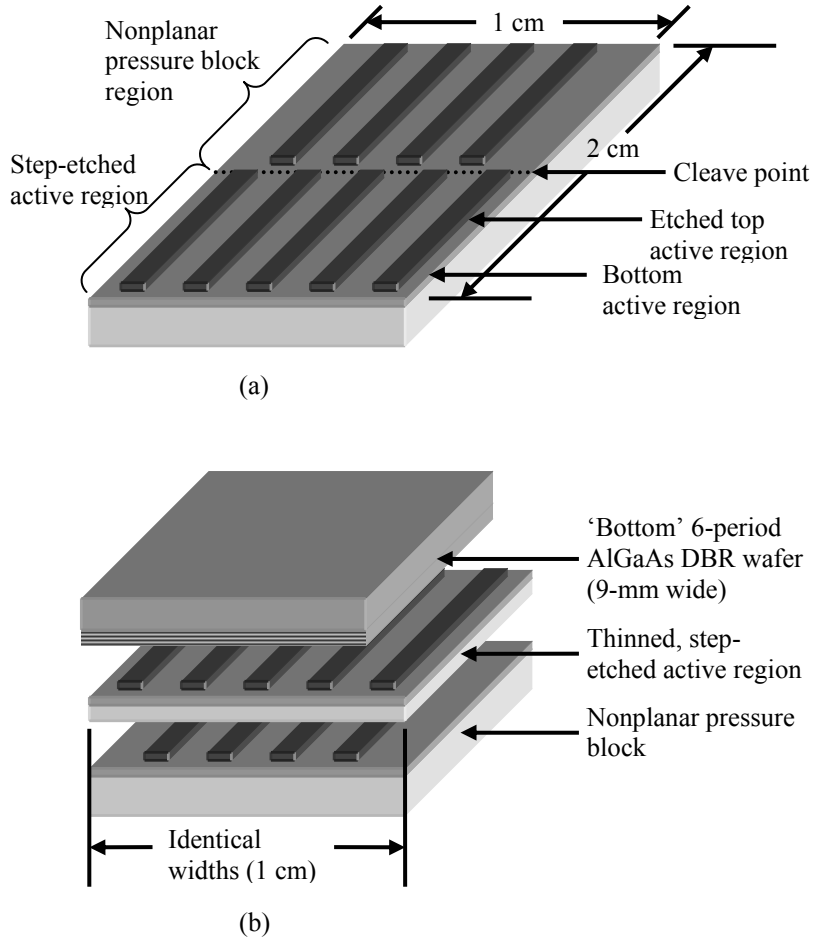

Figure 5.21. (a) Schematic of the etched InP active-region piece before cleaving apart the step-etched active-region half and the nonplanar pressure block half. (b) Schematic showing the nonplanar pressure block and the step-etched active-region piece. Both are identical in width

and the ridges are aligned on each piece as needed for nonplanar wafer bonding. Both pieces are wider than the AlGaAs DBR piece that the active regions will be integrated on.

Figure 5.22 shows a photograph of the wafer surface after patterning and etching the steps. The offset of the steps on the nonplanar pressure block side and the step-etched active-region surface side can be clearly seen. With both pieces having the exact same width and the correct relative positions of the steps with respect to the sample edges and each other, the steps of the active region and the nonplanar pressure block will be automatically aligned to each other by simply aligning the edges of the cleaved samples.

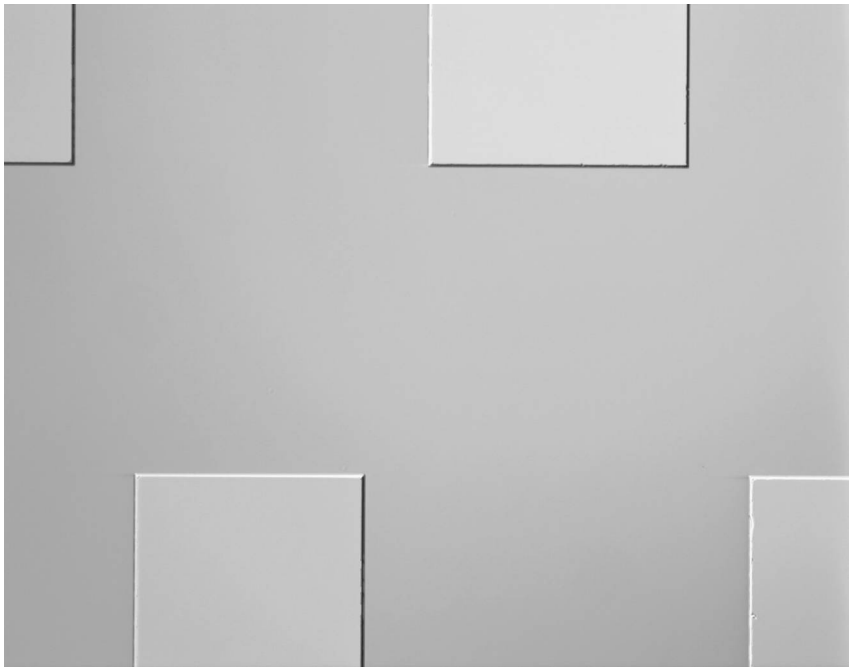

Figure 5.22. Photograph of wafer surface showing the separation between the area that will become the step-etched active-region surface (bottom) and the nonplanar pressure block surface (top). The two pieces will be cleaved apart along a horizontal path through the center of the photograph.

To align the edges of the cleaved active region and the nonplanar pressure block, a new graphite wafer bonding fixture was developed, as shown in Figure 5.23. The new fixture has a separate block that can apply pressure on the edges of the wafers pieces to force their edges to align to each other. As long as the GaAs DBR wafer piece is not as wide as the step-etched active-region piece and the nonplanar pressure block piece, it will not interfere with their alignment via the applied side pressure. The side pressure application block assembly can be removed to allow the fixture surface to be polished flat between bonds.

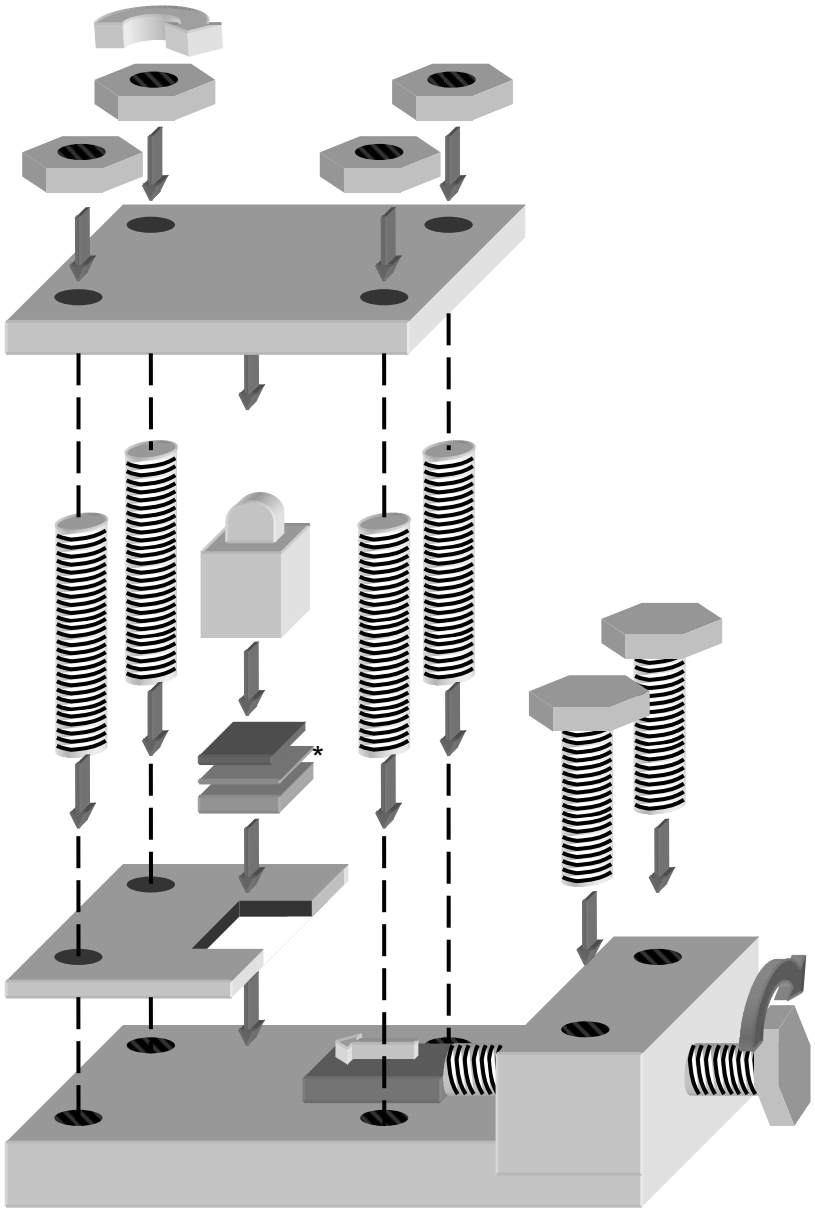

Figure 5.23. Exploded schematic view of the graphite nonplanar pressure block nonplanar wafer bonding fixture. Rotating the screw on the lower right pinches the samples (*) from the side and aligns their edges.

The etching of the nonplanar pressure block piece and the step-etched active-region piece is identical the procedure used in the backside processed nonplanar wafer bonding approach. After etching, the two pieces are separated by cleaving and the step-etched active-region piece is coated with PMGI and lapped to a 100 μm thickness. The nonplanar pressure block is coated with 100 nm of SiN_x.

5.5.2 Wafer Bonding

The bonding process used is identical to that described in section 5.4.5 except that the new fixture is used with a small amount of side pressure. The side pressure (gentle finger tightness only) is applied prior to applying the top bonding pressure (1.7 MPa for this work), and is released after the top pressure is applied. Figure 5.24 is a plot of a Dektak profilometer scan of the back of the InP substrate after the nonplanar wafer bond. The bending of the InP substrate caused by the nonplanar pressure block is clearly visible and creates a series of ridges on the previously flat sample. After the bond, the back of the InP active-region sample is lapped to remove about 25 μm of material. This is necessary for the InP substrate removal process because SiN_x from the nonplanar pressure block becomes impregnated in the back of the InP active-region sample and, unless removed, interferes with the substrate removal.

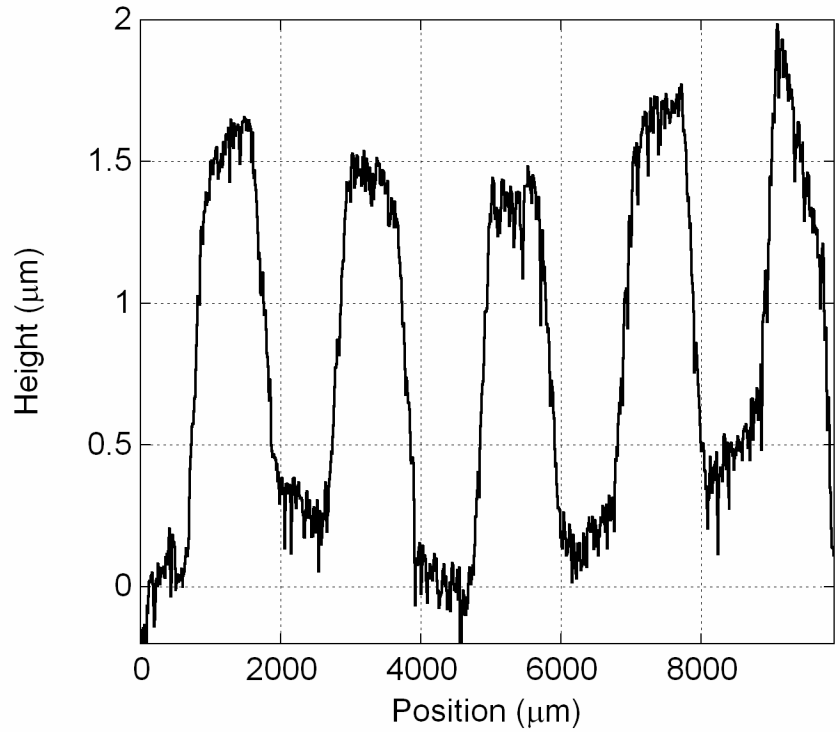

Figure 5.24. Plot of the profilometer scan of the backside of the thinned InP substrate after nonplanar wafer bonding, but before the InP substrate lapping and removal step.

All other steps after this post bond lapping step are identical to the backside processed approach, and when completed, two active regions of different design and of the proper thickness are laterally integrated on the bottom AlGaAs DBR wafer surface.

5.6 Superlattice Etching for WDM Arrays

With both active regions of the CWDM VCSEL array now laterally integrated on the AlGaAs bottom DBR, the superlattice layers responsible for creating the multi-wavelength sections on each active region, as described in section 4.2.2,

are etched [4]. The purpose of this etch is to create multiple thickness regions on each active region so that the final laser array will operate at multiple wavelengths determined by the thickness of the active region in each area. Figure 4.17 shows the concept of superlattice etching for multi-wavelength arrays and Figure 4.19 shows the final array configuration. In this section the technique used to etch the regions is presented.

The superlattice layers are 1.22-Q InGaAsP and InP (each 23.2 nm thick) (see Table 4.4). These layers are selectively etched, as are other layers in the active-region structure, with alternating H_3PO_4:HCl (3:1) and H_2SO_4:H_2O_2:H_2O (1:1:10) etches. The final goal is to have a repeating pattern of four different thickness regions on each active region. Thus, three superlattice layers must be removed. To minimize the number of mask steps required, a binary masking and etching approach is used. Doing so, the four step levels can be created with two mask levels. Figure 5.25 shows the general approach. Figure 5.26 shows the actual surface of the active region after the process and the position of the eight wavelength channels.

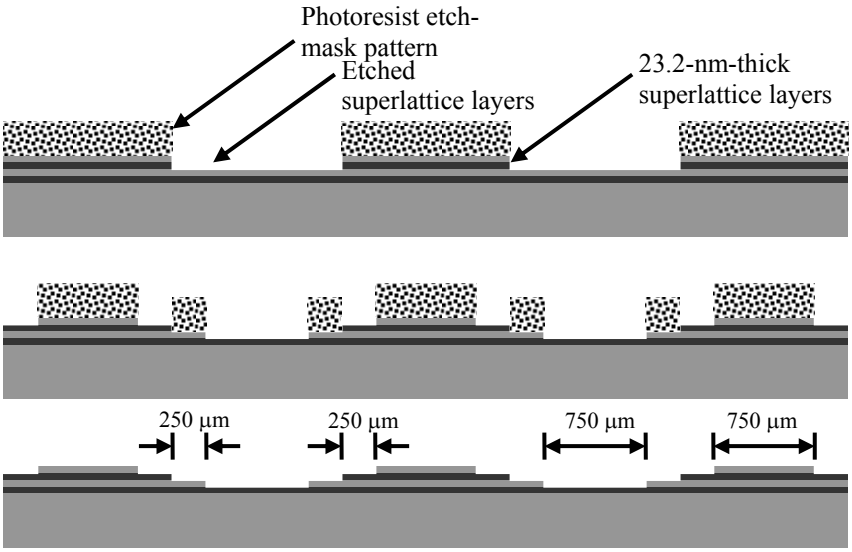

Figure 5.25. Schematic of superlattice wavelength adjustment process for multi-wavelength VCSEL array fabrication. Schematic is a side view of a stripe of active-region material integrated on the AlGaAs DBR (not shown). Two mask and etch steps are used to generate the four step levels.

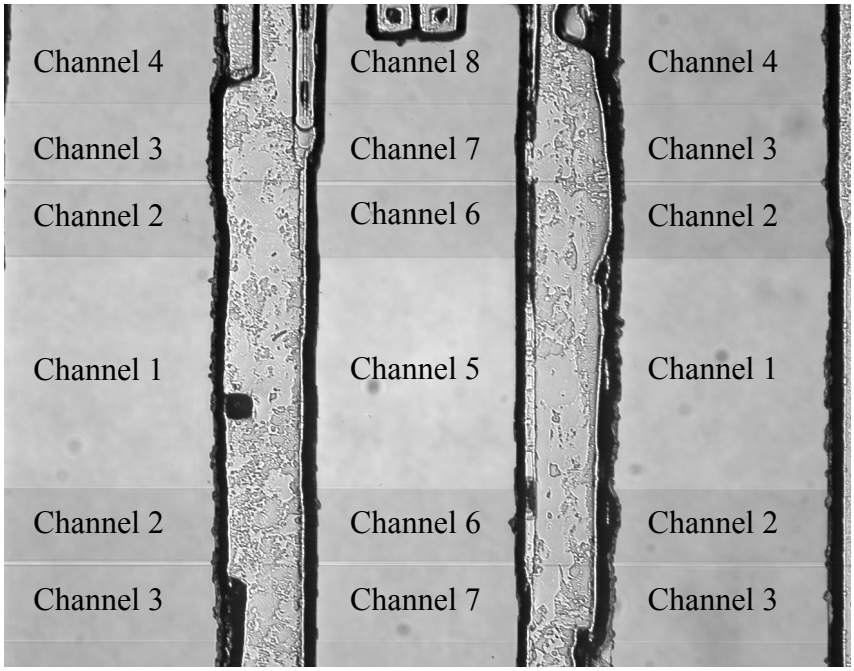

Figure 5.26. Annotated top view photograph of the two active regions integrated on the AlGaAs bottom DBR. The four multi-wavelength regions per active region have been etched.

During the processing used to fabricate the final CWDM VCSEL array, the photoresist used in the first masking step was not properly removed before patterning the second etch-mask. Thus, the channel-7 and channel-3 regions were roughened by the final etch. This error led to a reduction in device yield in the final devices. The roughening of the channel-7 region was detrimental to Channel 8 as well. As Figure 5.26 shows, Channel 8 is located adjacent to the alignment target areas. These areas tend to have reduced bond yield due to contamination that can occur due to the undercut these regions experience. With surface roughness in the channel-7 areas, and reduced bond area in the channel-8 areas, the top DBR mirror did not adhere well to Channel 8 and very few working channel-8 devices were available, as will be discussed more in Chapter 6.

5.7 Etching the Air-Gap Annuli

As described in Section 4.3, air-gap annuli are used in this work for mode confinement in the optically-pumped VCSEL structures. The annuli are etched into the surface of the top, 5.5-period, AlGaAs DBR epitaxial layers prior to wafer bonding the two integrated active regions. Table 4.6 shows the target depths of the four 8-μm inner diameter annuli. These depths are 32, 38, 44, and 50 nm. As shown in Figure 4.20, the outer diameter was chosen to be 24 μm so

as not to interfere with the lasing mode of the device. Figure 4.23 shows the final desired geometry for the four different depth annuli. In this section the processing required to attain the desired depths and geometry is described.

5.7.1 Controlled Etching

In order to etch the shallow annuli, a controlled wet-chemical etch was needed. The etch solution selected was H_3PO_4:H_2O_2:H_2O (2:1:60). This etch is easy to mix and has a reproducible etch rate of about 1 nm per second. Prior to etching the real sample however, a test sample is etched with the actual mixed etchant to verify the rate.

The annuli to be etched represent a small fraction of the wafer surface and the majority of the patterned surface is covered with photoresist. Photoresist is hydrophobic and hence will tend to allow for the formation and trapping of air bubbles in small features during wet chemical etches. Thus, care must be taken to prevent air voids from forming over the small features to be etched. Such voids will prevent etching and create unpredictable results, with many of the features not etching. To prevent these air voids, one of two things must be done. Either the photoresist must be made hydrophilic (by an O_2 plasma descum prior to etching), or the clear pattern in the photoresist must extend all the way to the edge of the sample so the etchant can be drawn along

the pattern and displace any air that might otherwise be trapped. This latter approach was used in this work.

The pattern used was a column of annuli with each annulus in the column connected to its neighbor by a 10-μm-wide channel. The neighboring annuli and columns are on a 50-μm pitch. Each column depth repeats across the sample every 250 μm. The sample is patterned using a 1-μm thick photoresist with vacuum-contact lithography. The vacuum-contact mode was used to maintain precise the 8-μm inner annuli diameter. The epitaxial surface of the DBR is first patterned and etched to create the column of 50-nm-deep annuli. Then the photoresist etch mask is stripped with acetone and the sample is patterned and etched again to create the column of 44-nm-deep annuli. This process is repeated until all four columns of differing depth annuli have been etched in the surface. The columns are all aligned to each other so the finished annuli are spaced in a 2-D array on 50-μm centers. One empty column remains after the processing is complete. Figure 5.27 shows the etched DBR surface after all the annuli have been etched. With this technique, each row has annuli with all four of the etch depths.

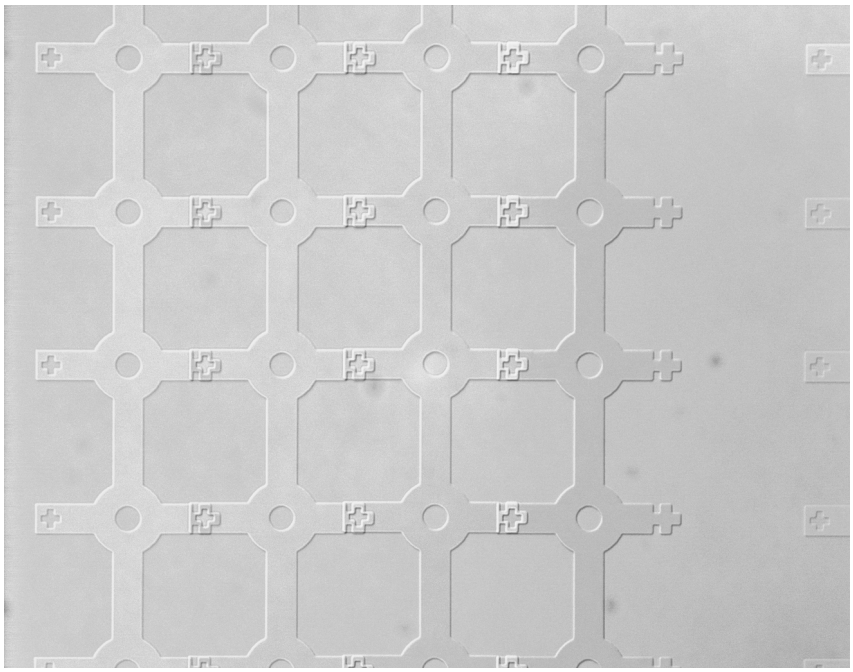

Figure 5.27. Photograph of the epitaxial surface of the top DBR of the VCSEL prior to wafer bonding and after etching the annuli. The annuli are separated from each other by 50 μm. Each of the four columns is a different etch depth so each row has four different depth annuli in it.

5.8 Finishing the Epitaxial Structure Assembly Process

The final wafer bond of the process is used to integrate the top AlGaAs DBR with the two laterally integrated active regions and the bottom AlGaAs DBR. The surface of the laterally integrated active regions on the bottom DBR is not flat in the traditional sense, but includes the step height variation due to the superlattice adjustment etches and the overall differences in the active-region thicknesses. The largest height difference is about 157 nm and this is the difference between the thicknesses of the active-region material in the Channel-1 and the Channel-8 areas of the integrated substrate. The height differences

between adjacent regions on the wafer surface are only about 23 nm and this is the more critical dimension that must be considered.

5.8.1 Second Wafer Bond

Despite the thickness variations on the sample, traditional planar wafer bonding was used to bond the top DBR, with its patterned air-gap annuli, to the pair of laterally integrated active regions on the bottom DBR surface. The process is identical to that of Section 5.4.5. The bond pressure used is 1.54 MPa.

5.8.2 GaAs Substrate Removal and GaAs Substrate Polishing

Following the wafer bond step, one of the GaAs substrates is removed using a citric acid and peroxide based etch, and the other is polished using a chemical-mechanical polish. The GaAs substrate to be removed is the one associated with the top DBR. The substrate associated with the bottom DBR requires polishing so the optical pump light can enter the VCSEL during testing.

The GaAs substrate to be removed was about 400-μm thick, and the process begins by wax mounting the sample to a lapping block and hand lapping the substrate to remove about 370 μm of material. A course grit lapping paper is sufficient for this step. The sample is then remounted to expose the bottom DBR's GaAs substrate for polishing. This substrate is lapped to remove 25 μm with a 9-μm grit lapping paper. The lapping fixture and the mounted sample are

carefully cleaned to remove any 9-μm grit material and the sample is lapped again to remove another 25 μm using a 3-μm grit lapping paper.

After lapping the bottom GaAs substrate with the 3-μm grit lapping paper, the mounted sample is carefully cleaned to remove any trace of the 3-μm grit. The sample is then hand polished on a silk cloth using 0.5-μm grit alumina powder mixed with standard household bleach. About one minute of polishing on the silk cloth with the alumina and bleach mixture is sufficient to give the bottom GaAs substrate a mirror finish.

Following the lapping and polishing steps, the sample is prepared for the GaAs substrate removal process. The double wafer bonded sample is demounted from the lapping block and wax mounted to a glass cover-slip with the remaining top GaAs substrate material (un-polished side) exposed. The excess mounting wax is removed using a spin clean with an acetone spray. Tergitol cleaning is also used to ensure no wax residue remains exposed. Any exposed wax interferes with the substrate removal etch.

The GaAs substrate-removal etch process uses a citric acid and hydrogen peroxide solution. The citric acid is mixed by dissolving 60 grams of citric-monohydrate in 60 ml of H_2O. The citric acid solution is then mixed with 25 ml of hydrogen peroxide (H_2O_2). The solution is held at a constant 25 °C on hot plate and a stir bar is used for constant agitation. The mounted sample is placed in the solution facing away from the stir bar and the GaAs substrate is etched at

a rate of about 0.6 μm per minute. The total substrate removal time is about 60 minutes. The Citric:Peroxide etch stops on the AlAs etch-stop layer grown at the bottom of the top, 5.5-period, AlGaAs DBR. After the etch reaches this layer, the sample is removed from the solution and dipped into $HCl:H_2O$ (1:3) for one minute to remove the AlAs layer, and $HF:H_2O$ (1:10) for 20 seconds to remove any remaining oxidized AlAs. Oxidized AlAs debris is typical on the sample and a Tergitol swab cleaning of the sample surface can be used to remove any remaining residue. Following the GaAs substrate removal process, the VCSEL epitaxial structure is complete. Figure 5.28 is a photograph of a section of the top surface of the completed multi-wavelength VCSEL sample. The bubbles in the bonded area are a result of the fact that some small air voids form when the top DBR conforms to the superlattice steps during the final wafer-bonding step. Figure 5.29 shows a cross-section schematic of a single channel of the completed VCSEL epitaxial structure.

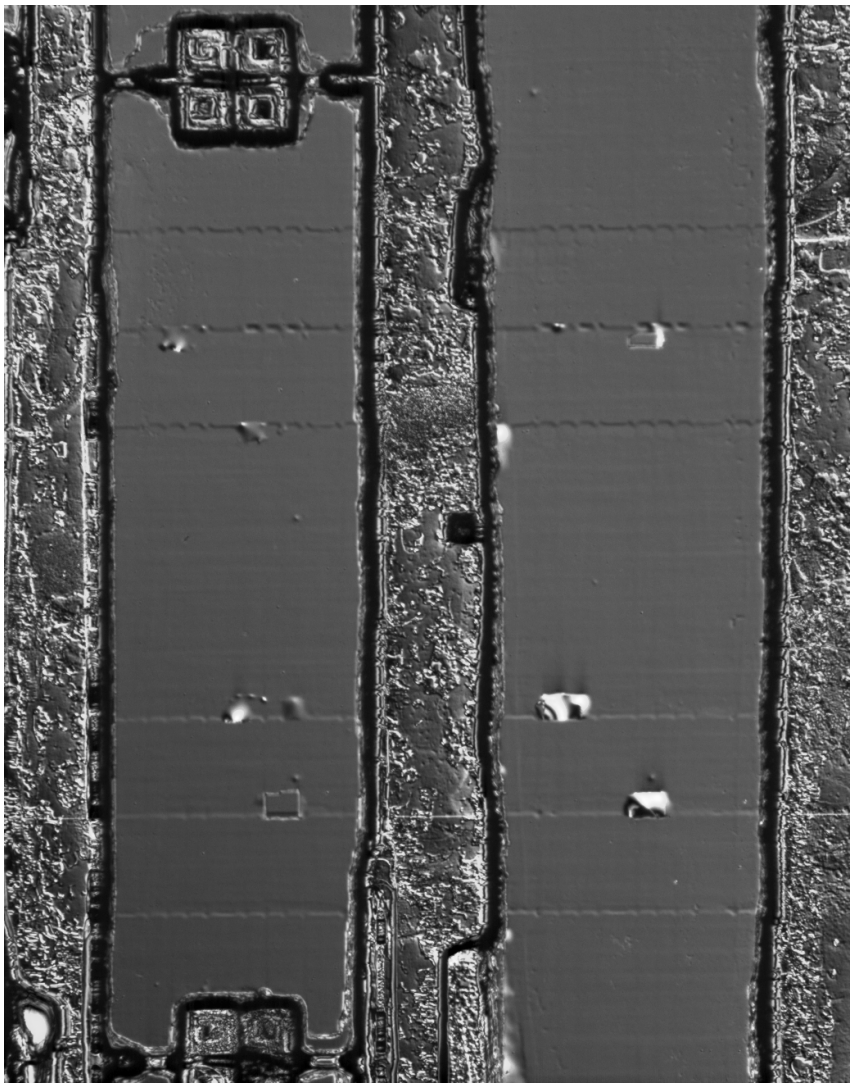

Figure 5.28. Photograph of a section of the top surface of the completed multi-wavelength VCSEL sample. Nemarski mode is used to enhance the surface contrast and accentuate height differences.

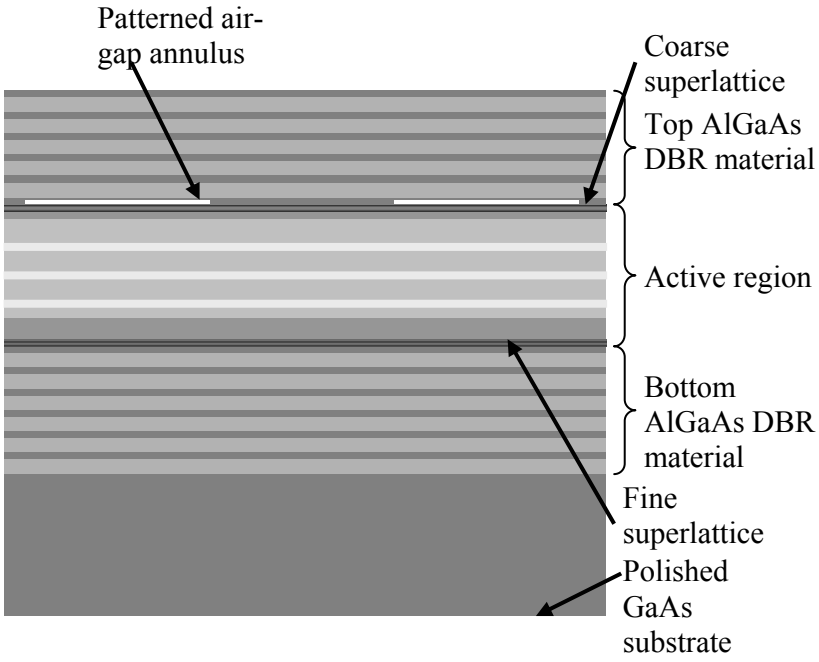

Figure 5.29. Cross-section schematic of the completed VCSEL device epitaxial structure after two wafer bond steps. The patterned air-gap annulus for mode confinement and the polished GaAs substrate are also shown.

5.9 Oxidation of the DBR Material

Following the successful integration of the dual active regions with the dual AlGaAs DBR material, the final process step required to create a resonant VCSEL cavity is the formation of the fully oxidized DBRs from the AlGaAs DBR material. Section 4.1 discusses in detail the design and fabrication issues involved with using this mirror technology in optically-pumped long-wavelength VCSELs. In this section the actual process steps required to create the finished mirrors structures from the integrated VCSEL epitaxial structure will be discussed.

5.9.1 Etching the Oxidation Holes

The final VCSEL structure makes use of a variety of materials including 1.22-Q InGaAsP, InGaAsP quantum wells, InP, GaAs, AlAs, and graded AlAs to GaAs transitions. In order to access the top and bottom DBR AlAs layers for oxidation, an etch process was required that could reliably and uniformly penetrate the entire VCSEL structure via a 10-μm-wide etched trench extending across the wafer surface. The trench is positioned between the buried VCSEL air-gap apertures using infrared alignment. The ideal etch is likely an inductively coupled plasma (ICP) etch suited for etching all the materials in the structure. At the time of this work, ICP etching was not available for use. Thus, a hybrid etching approach was developed to etch the entire structure.

The first etch developed was designed to etch the AlGaAs DBR material but not etch the InP and InGaAsP material. This is an RIE process based on chlorine and BCl_3. This etch was developed while at Gore Photonics to maximize etch rate, and sidewall smoothness and straightness when used with a photoresist and SiN_x etch mask. The etch uses 19.5 standard cubic centimeters per second (sccm) of BCl_3, 1.5 sccm of Cl_2 at 15 mT pressure and 75 W of power. The etch rate is about 0.4 μm per minute through the DBR material and negligible through the InP material (about one tenth the AlGaAs rate). To ensure the entire top DBR would be penetrated the etch time for the 5.5-period

DBR (about 2-μm thick) was set to 6 minutes. The etch mask process included a 250-nm SiN_x mask and a 3-μm photoresist mask. After patterning a 10-μm wide trench pattern on the sample (see Section 4.1.4), the SiN_x was etched using a 4-minute, 300-mT, 100-W CF_4 etch. Then, the sample surface was rinsed with an $NH_4OH:H_2O$ (1:20) solution for one minute and nitrogen dried. The $NH_4OH:H_2O$ solution removes surface oxides from the GaAs area and prevents micro-masking during the RIE. Immediately after the oxide clean, the sample was loaded for the 6-minute Cl_2 and BCl_3 RIE.

After the completion of the timed $Cl_2:BCl_3$ RIE, the sample is removed from the etch-chamber load lock and immediately rinsed in deionized water. This water rinse is essential to remove chlorine based etch byproducts. Without the water rinse, the byproducts will react vigorously with the AlAs layers in the structure. If this happens, the wet thermal oxidation step in the process will produce material delamination and non-uniform lateral oxidation fronts. With the proper water rinse, the sample can safely remain etched for days prior to controlled wet-thermal oxidation of the AlAs.

After the first RIE, the photoresist mask is stripped from the sample using heated 1165 (NMP) and the sample is solvent cleaned. It is now ready for an MHA InGaAsP etch. The details of this etch process are in the Appendix B. The RIE uses Methane:Hydrogen:Argon flow rates of 4:20:10 sccm at 75 mT with a -450 V electrode bias. The etch chemistry deposits organic material as it

etches and the sample must be in-situ O_2 plasma cleaned after the etch process. The InGaAsP active-region etch rate was measured to be about 80 nm per minute. The etch rate of GaAs material was measured to be about 40 nm per minute and the AlAs etch rate was undetectable. Thus, a long over-etch of the active region results in the complete penetration of the InGaAsP active region and the first GaAs layer of the bottom AlGaAs DBR. The etch process will come to a stop on the AlAs layer of the bottom DBR. Because this AlAs layer could be used as etch stop layer, the etch time for the MHA etch was set to 22 minutes to ensure the AlAs layer was reached in all areas of the sample. The MHA etch process was followed by an 11-minute in-situ O_2 plasma clean (20 sccm, 125 mT, -300 V).

Following the MHA RIE, the VCSEL sample was dipped in buffered HF for 15 seconds to remove the AlAs layer exposed at the bottom of the 10-μm wide trench. The buffered HF etch stops on low aluminum content AlGaAs layers and hence, does not penetrate further down than the one AlAs layer and part of the next linear AlGaAs composition grade.

The SiN_x used in this work was plasma deposited and had an etch rate of 37 nm per minute in the buffered HF. The etch rate in the MHA RIE was negligible. The SiN_x sputter rate in the Cl_2:BCl_3 RIE used for this work was measured to be 12 nm per minute. Thus, a 250-nm SiN_x layer can withstand 20 minutes of Cl_2:BCl_3 etching after the 15 second buffered HF sample dip. This is

sufficient for the final 8-minute Cl_2:BCl_3 RIE used to penetrate through the rest of the bottom AlGaAs DBR material. Figure 5.30 shows the etch process flow required to penetrate the structure.

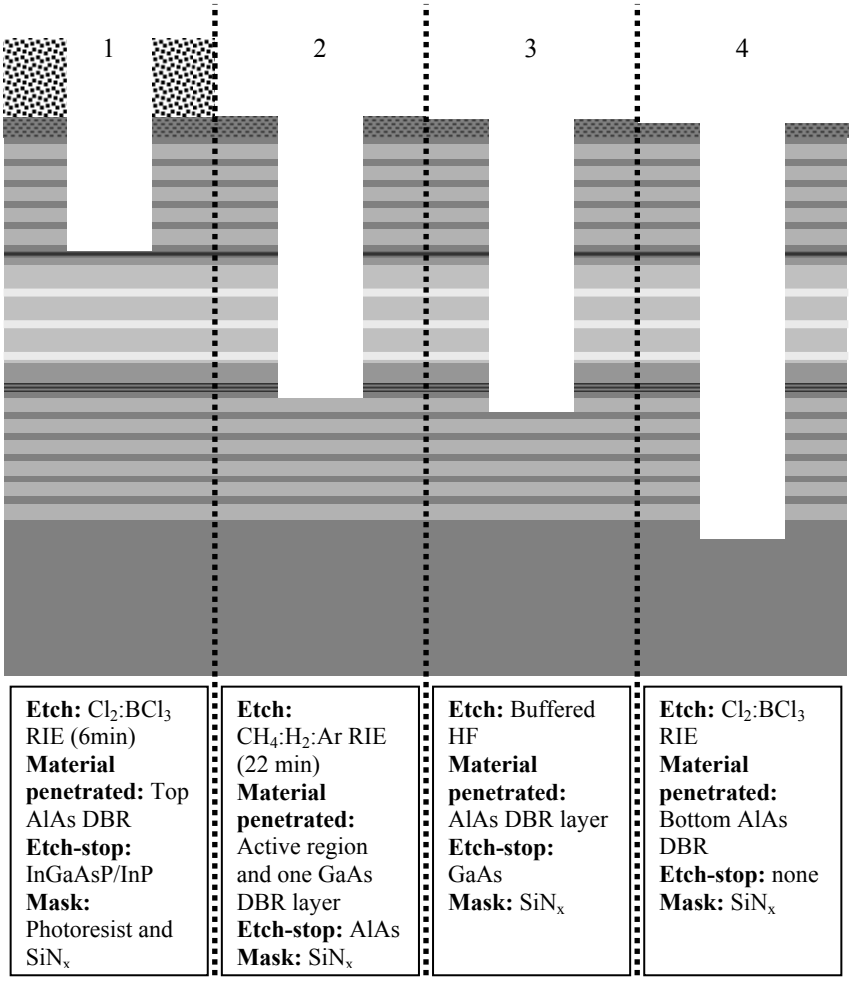

Figure 5.30. Process-flow schematic showing the etching of the VCSEL structure's oxidation trench.

5.9.2 Oxidizing the DBR

Following the final Cl_2:BCl_3 RIE, the entire VCSEL structure has been etched and all the AlAs layers of the DBR material have been exposed and are ready for oxidation. The oxidation geometry is discussed in Section 4.1.4 and Figure 4.14 shows the oxidation trench positions with respect to the buried VCSEL air-gap annulus apertures. The geometry is designed to completely oxidize all the VCSEL AlAs DBR layers and offset the final union of the oxidation fronts away the central axis of the VCSEL aperture. Here the actual oxidation will be discussed.

The oxidation process has been previously developed elsewhere and was used as a process tool for this work. The purpose of the oxidation step is to convert all the AlAs to AlO_x with it's correspondingly lower index of refraction. The etched oxidation trenches are 10-μm wide and are spaced 100-μm apart. The oxidation fronts need to extend laterally 45 μm for the entire DBR to be laterally oxidized. Figure 5.31 shows a cross-section view of an etched VCSEL device. The SiNx mask used during the etching of the oxidation trenches is keep over the top of the sample to protect the GaAs wafer surface and prevent any roughening that may occur.

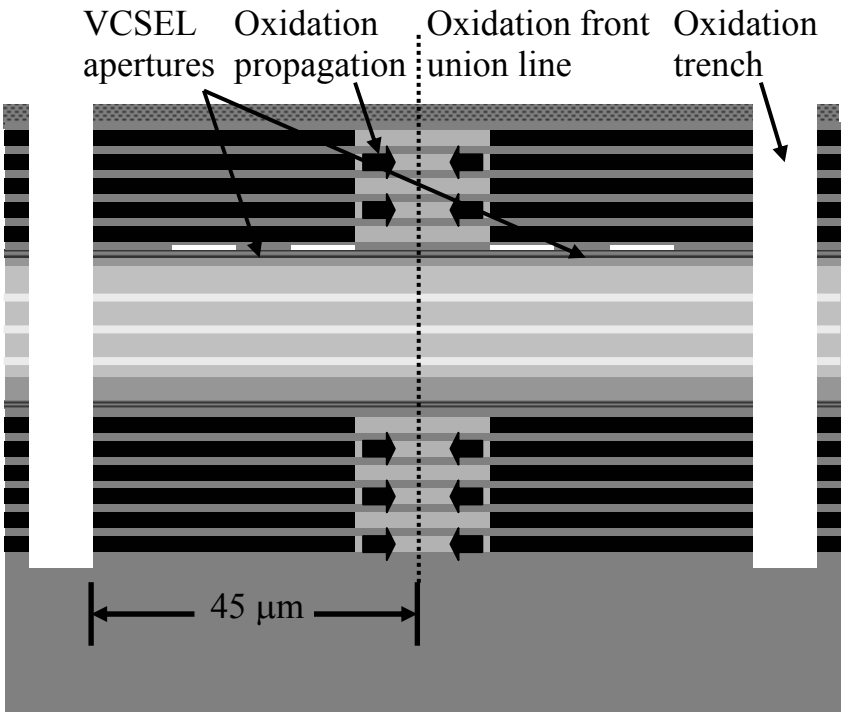

Figure 5.31. Cross-section Schematic showing lateral oxidation of AlAs from etched oxidation trenches.

Oxidation calibrations were conducted to determine the oxidation rate. At a furnace temperature of 400 °C the oxidation rate of the mirror layers was measured to be about 1.6 μm per minute. At 430 °C the rate was about 3.3 μm per minute. Cleaved cross-sections of oxidized DBR test material that had been double bonded and oxidized were investigated and all layers in the mirror were verified to oxidize at the same rate, indicating that any stress that might be associated with the bonded interface does not affect the oxidation rate of the adjacent layers. Mirror reflectivity measurements from samples oxidized at both 400 and 430 °C indicated the oxidation temperature had no impact on the quality

of the mirror stop-band shape. Thus, a 430 °C oxidation temperature was selected. The gas flow rate in the 2-inch diameter tube furnace was 1000 sccm, and the nitrogen carrier gas was bubbled through water heated to 80 °C.

Because all the AlGaAs DBR material grown for this work used AlAs layers for oxidation, the oxidation rate was stable between samples from different wafers. Thus, no final oxidation rate calibration was needed. A single small cleaved piece of the wafer surface was used prior to oxidizing the whole sample to ensure that the furnace was operating correctly. Once the furnace was checked, the sample was oxidized for a total of 14 minutes. This oxidation time provides a small amount of over-oxidation to ensure the entire layer is converted. A timed sample load and unload step was used because removing the furnace cap affects the temperature of the furnace and the overall oxidation rate. The load sequence is shown in Table 5.2.

Step	**Time (min:sec)**	**Description**
1	-0:05	Start timer
2	0:00	Remove furnace cap
3	0:10	Hook oxidation boat
4	$0{:}10^{+}$	Begin slowly withdrawing boat
5	0:20	Finish withdrawing boat
6	0:20	Exchanging sample(s) on boat
7	$0{:}40^{-}$	Finish exchanging samples on boat
8	0:45	Beginning inserting boat
9	0:55	Finish inserting boat
10	1:00	Replace furnace cap

Table 5.2. Oxidation furnace load/unload sequence.

5.10 Anti-Reflection Coatings and Metallization of the Pump Targets

After fully oxidizing the VCSEL mirror structure, the VCSEL resonant structure is complete. To enhance the performance of the devices and ease testing, a few steps remain. First the protective SiN_x top layer is removed and replaced with an e-beam deposited SiO anti-reflection coating. This coating reduces the total reflectivity of the top VCSEL mirror by eliminating the semiconductor-air interface reflection. The index of the layer is about 1.75 and is designed to be one-quarter wavelength thick at a wavelength of 1540 nm (220 nm). The same anti-reflection coating is deposited on the backside of the VCSEL structure to prevent reflections from the polished backside of the sample from interfering with the laser operation.

Testing of the optically-pumped VCSELs requires aligning the focused pump laser spot on the VCSEL aperture. This process is greatly simplified if visual pump targets are placed on the sample. The pump targets can be located with the aid of a microscope integrated with the optical pump measurement system. The pump target shape chosen was a 40-μm-diameter circular opening in a metal pattern centered on each VCSEL aperture. The metal used was a Ti:Au e-beam deposited film. Figure 5.32 shows a photograph of the pump

targets deposited on the VCSEL chip. The pump target pattern also includes numbered serialization labels to aid in data collection and testing.

The pump targets are aligned to the buried VCSEL apertures using infrared alignment. The serialization labels are aligned over the column of missing air-gap annuli that was intentionally left blank during the processing of the top DBR surface prior to wafer bonding. In addition, the most shallow etched air-gap annuli are located directly above the serialization labels and the deepest etched air-gap annuli are located directly below the serialization label. These regions are labeled R1 through R4 in the figure, with R1 indicating the position of the shallow-etched annuli and hence the weakest index guide.

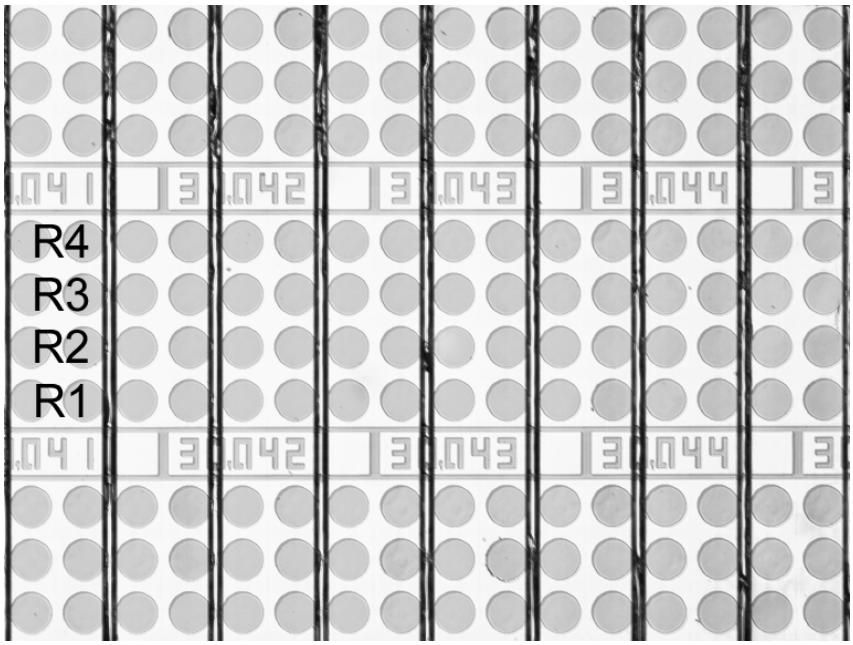

Figure 5.32. Photograph of the metal pump targets and serialization labels on the completed VCSEL chip surface. The rows of different strength index guides are marked by R1 through R4 (weakest to strongest).

5.11 Process Challenges

The successful fabrication of the CWDM VCSEL array required many challenges to be overcome. These process challenges were primarily concerned with the development and application of nonplanar wafer bonding. Such challenges were overcome to achieve the results of this work.

As has been alluded to before, wafer bonding requires very smooth surfaces in order to achieve a successful bond. In the wafer bonding steps of this work, the wafer surface underwent multiple wet-chemical etching steps prior to the bond steps. These etch steps were used to form the stepped wafer surface of the nonplanar wafer bond, and were used to form the multiple wavelength regions prior to the second wafer bond step. During wet-chemical etching, it is possible for debri, already present on the surface to be etched, to mask the surface. This masking will leave raised, under-etched regions on the wafer surface. These under-etched regions will prevent large areas of the wafers from contacting each other during the bond and can result in large unbonded regions.

To prevent the occurrence of these raised regions, the Tergitol cleaning technique previously described was developed. With the implementation of this cleaning technique, wafer bond areas in excess of 80% were consistently attained for both the backside processed and the nonplanar pressure block nonplanar wafer bonding processes.

Another critical challenge overcome in this work was the formation of proper step heights to promote the bending of the wafer during nonplanar wafer bonding. As was presented in Chapter 2, nonplanar wafer bonding requires the overall thickness of the wafer stack in the wafer bonding fixture be nearly identical at each lateral point. This is the reason for the backside processed steps or the use of the nonplanar pressure block. These two structures compensate for the heights of the steps levels on the surface of the epitaxially-grown wafer and promote the bending of the growth substrate when pressure is applied. Problems can arise when the heights of the backside etch or the nonplanar pressure block steps are not the same as the step levels on the epitaxially-grown side of the substrate.

Some lateral variability in the wafer thickness can be accommodated as is evident in the second wafer bond step of the VCSEL array fabrication. During this step, the surface is not flat due to the etched superlattice wavelength adjustment layers. Based on the development work conducted for nonplanar wafer bonding, it is estimated that the thickness variation between the epitaxially step levels and the heights of the backside etch or the nonplanar pressure block surface steps should be less than 5%. This is based only on antidotal evidence and is likely dependent on the specifics of the nonplanar bonding geometry. Never-the-less, it is important that the steps formed for the backside etch or the

nonplanar pressure block closely match the step-level heights on the surface of the epitaxially-grown wafer.

5.11 Process Summary

The finished process produces a completed sample with as many as 80 8-channel CWDM VCSEL array chips per sample. Figure 5.33 is a photograph of a finished CWDM VCSEL array from the wafer surface.

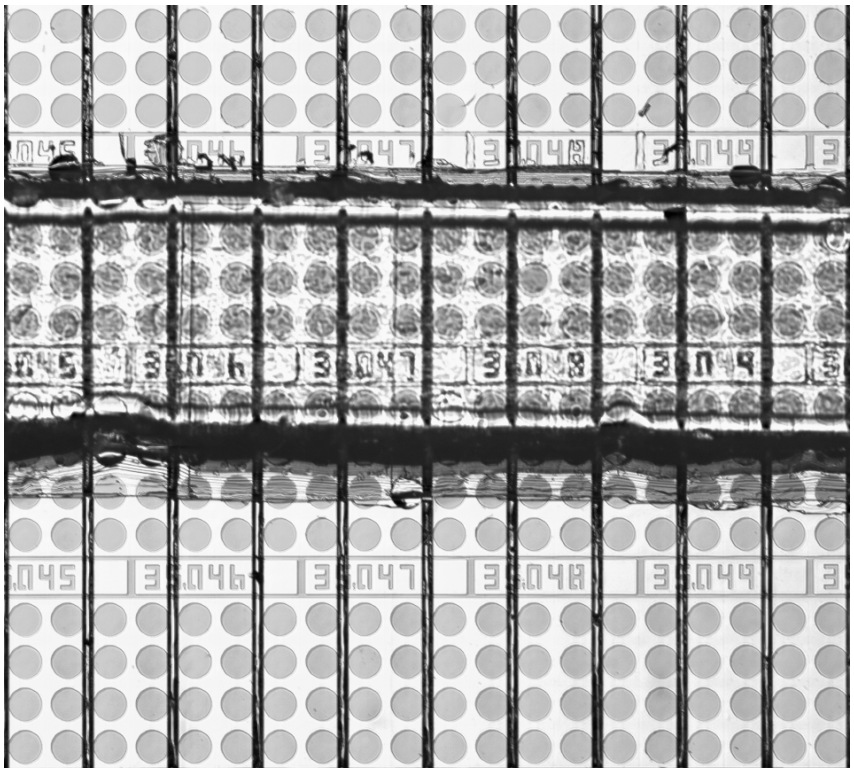

Figure 5.33. Photograph of completed CWDM VCSEL array. The material in the center is the etched bending accommodation region and the smooth areas on the top and bottom of the photo are the VCSEL regions.

CHAPTER 5: DEVICE PROCESSING

Many process challenges were overcome to fabricate the finished devices. Air-brush surfactant (Tergitol) cleaning steps were developed to maintain the sample cleanliness throughout the process. Two nonplanar wafer bonding techniques were developed, including InP substrate polishing and techniques to protect the epitaxial wafer surface during backside process steps. Novel wafer bonding fixtures were developed to allow for alignment between the step-etched active-region wafer and the nonplanar pressure block piece. In order to access the top and bottom AlGaAs DBR for oxidation, a four-step etch approach was developed. To optically pump the device, the backside of the sample was polished and anti-reflection coated at 1540 nm.

The final process resulted in a complete CWDM VCSEL array chip. The array uses two different VCSEL active regions and top and bottom fully-oxidized DBRs. The wavelength span of the array is the widest ever made in a long-wavelength VCSEL and covers 140 nm.

Due to a poor photoresist strip step during the etching of the WDM superlattice adjustment etch steps, many of the Channel-3 and Channel-7 regions were roughened. This resulted in lower device yields in these areas and the loss of most of the Channel-8 devices. Despite this problem, an area yield estimated at 80% was attained and all 8-channels on the chip operated. In addition, at least one completely functioning array was tested. The test results from this array are presented next, in Chapter 6.

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Chapter 6

WDM Array Testing, Results, and Analysis

In chapters 2 through 5 of this work, the completed design and fabrication of an optically-pumped, 2-D, CWDM VCSEL array was presented. To achieve an ultra wide wavelength span of 140 nm, the CWDM VCSEL array makes use of the novel lateral heterogeneous integration technique of nonplanar wafer bonding, and fully oxidized DBRs. Mode control is accomplished with a buried air-gap aperture.

In this chapter the completed CWDM VCSEL array is tested continuous wave (CW) from room temperature to the maximum lasing temperature of the array (90 °C). The emission properties of elements across the multi-wavelength array are compared and conclusions are drawn. The general optically-pumped VCSEL emission properties related to mode control and light output linearity

are discussed and explained as is the thermal impedance properties of the VSCEL design. Before the 2-D optically-pumped arrays could be tested, a measurement system capable of controlled optical pumping of the devices was required. Thus, a new semi-automated test and measurement system was developed for this task, and is presented and discussed.

The eight-channel CWDM VCSEL array results shown here cover the widest wavelength span ever reported in a long-wavelength VCSEL. The array spans 140-nm from 1470 to 1610 nm. All wavelength channels in the array operate to at least 65 °C and are single mode with only +/- 1 dB of output power variability. These arrays represent a significant step toward the development of a single-chip source for CWDM applications. The fundamental technology is not limited to 140 nm, but is capable of fabricating VCSEL arrays covering several hundred nanometers.

6.1 Experimental Setup for Testing Optically-Pumped VCSELs

The testing of optically-pumped VCSELs poses challenges different than those of electrically-pumped VCSELs. This is particularly true for multi-wavelength optically-pumped VCSEL arrays. The devices in this work are optically pumped from the backside of the sample, and different wavelength regions

existed within close proximity (250 μm) on the same chip. In addition, the device aperture diameter is only 8 μm. These single-mode devices need to be tested over a wide temperature range (about 20 – 90 °C) without exciting unwanted higher-order modes by optically pumping the device off-axis. The complexity of the testing required the development of a specialized measurement setup. The setup was built to be robust, allowing rapid stage temperature changes with minimal position drift, and was completely computer controlled for semi-automatic operation.

With eight different wavelengths per chip, and testing across a broad temperature range, a large amount of light-out vs. light-in test data was generated. To aid in the analysis of this data, a Matlab program was written to automatically extract and tabulate the basic parameters from the light-out vs. light-in VCSEL data. This VCSEL light-out vs. light-in test data can be analyzed in two different ways. It can be analyzed as a function of the total pump power incident on the bottom of the VCSEL chip, or it can be analyzed as a function of the pump power actually absorbed by the chip. This difference will be discussed in more detail later in this section.

This section will discuss the test and measurement system built, and the general data analysis method used. Measurement results will be presented in Section 6.3.

6.1.1 The Optical Pumping Test System

In order to properly characterize optically-pumped, index-confined, multi-wavelength VCSEL arrays, a capable test and measurement system is required. Such a test system must be capable of delivering a focused pump laser beam to the VCSEL aperture with precise and accurate placement. The alignment process must be fast and reproducible and must consider all three relevant axis of alignment (orthogonal x-, y-, and z-axis). The system must be capable of maintaining the pump/VCSEL alignment for extended periods of time and be capable of changing the sample temperature from room temperature to 90 °C without requiring substantial realignment of the pump to the VCSEL. The alignment precision in the plane of the sample must be sub-micron to prevent pumping the VCSEL off-axis. The measured data from the device under test (DUT) must be collected and saved in a format usable by other analysis programs.

In order to find and test the proper device on the sample, the optical pumping measurement system must be integrated with a microscope. In addition, the system must be capable of easily switching between a photodetector and a fiber probe. The photodetector should be capable of simultaneously measuring the VCSEL emission near 1540 nm and the excess 980 nm pump light that leaks through the top of the VCSEL.

CHAPTER 6: WDM ARRAY TESTING, RESULTS, AND ANALYSIS

To meet all the test requirements listed for this project, a semi-automated test system was built. Figure 6.1 shows a photograph of the overall system, and Figure 6.2 is a photograph of the test system measurement stage. The system has several key features designed to simplify the testing of devices and improve the quality of the test data. The system delivers the pump light to the bottom of the sample and has a top-side microscope capable of viewing the pump light leaking through the VCSEL, thus allowing the operator to roughly align the VCSEL to the pump beam. Figure 6.3 shows a picture captured from the computer screen during the rough manual alignment process. The microscope uses a camera to avoid eye-safety issues. The entire measurement setup is controlled via a single LabVIEW program. The program control includes an automated 3-axis VCSEL/pump alignment routine, full stage motion and temperature control, all data collection and storage, and pump laser power control. Figure 6.4 shows screen capture of the program front control panel in one mode of operation (automated VCSEL/pump alignment mode).

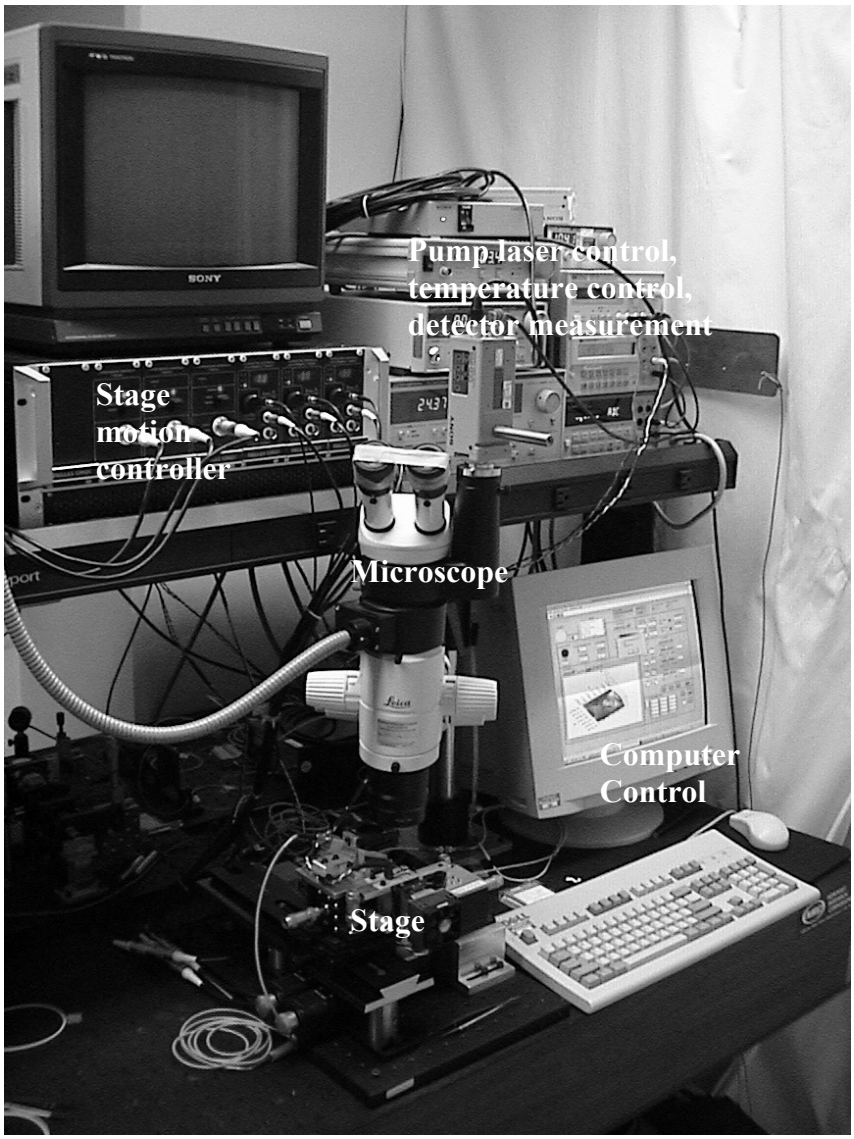

Figure 6.1. Photograph of overall optical-pumping test system.

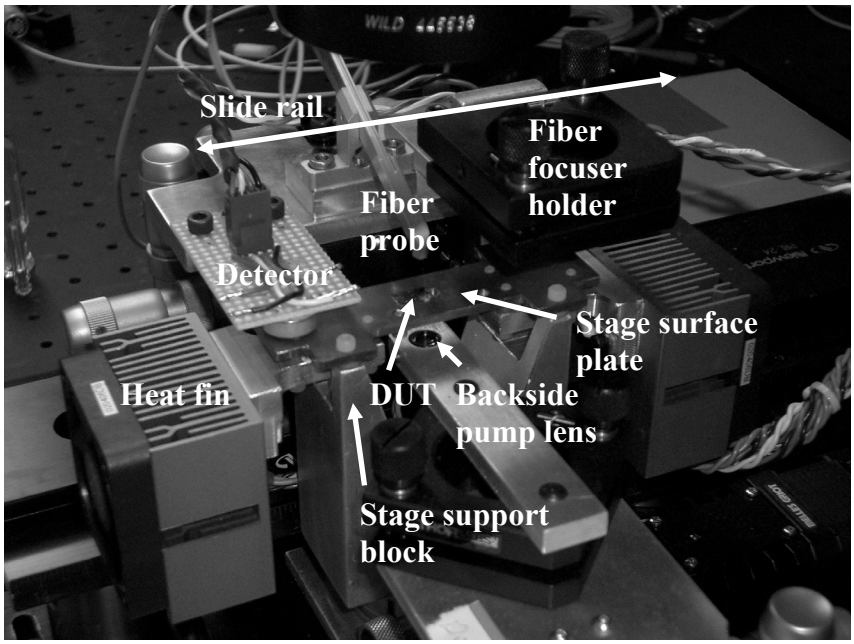

Figure 6.2. Photograph of optical-pumping test system measurement stage.

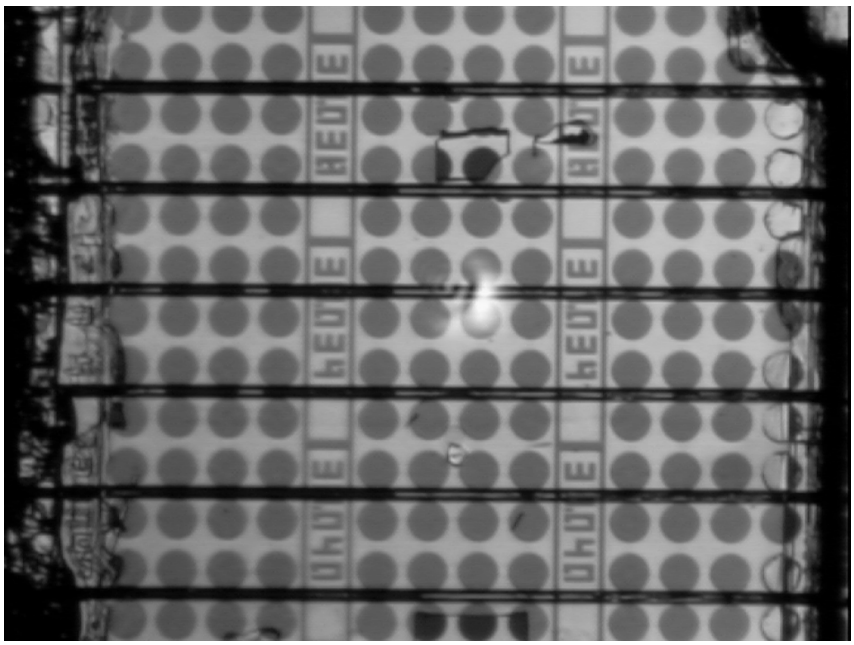

Figure 6.3. Photograph of manual alignment image viewed by operator. The pump laser light passing through the VCSEL allows the VCSEL and pump beam to be coarsely aligned prior to running the program-controlled fine-alignment routine.

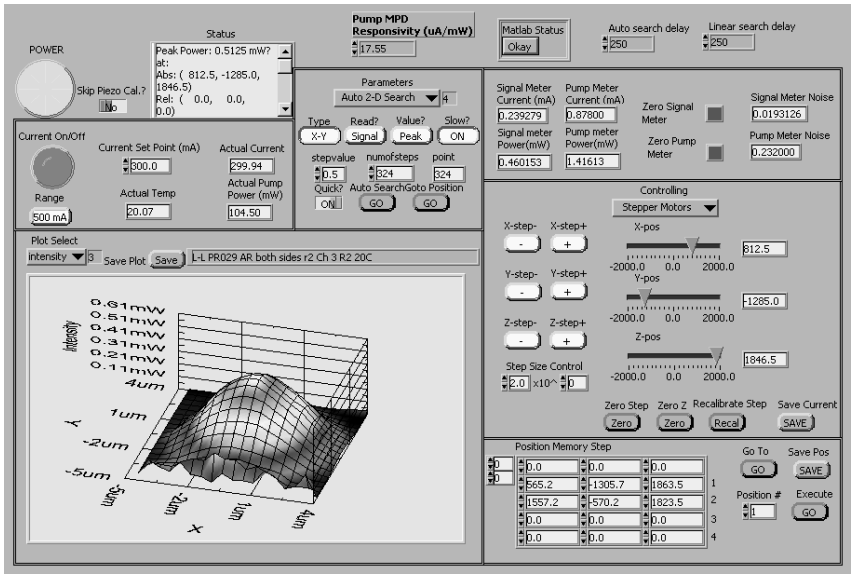

Figure 6.4. Photograph of the test system's graphical user interface during automated VCSEL/pump alignment.

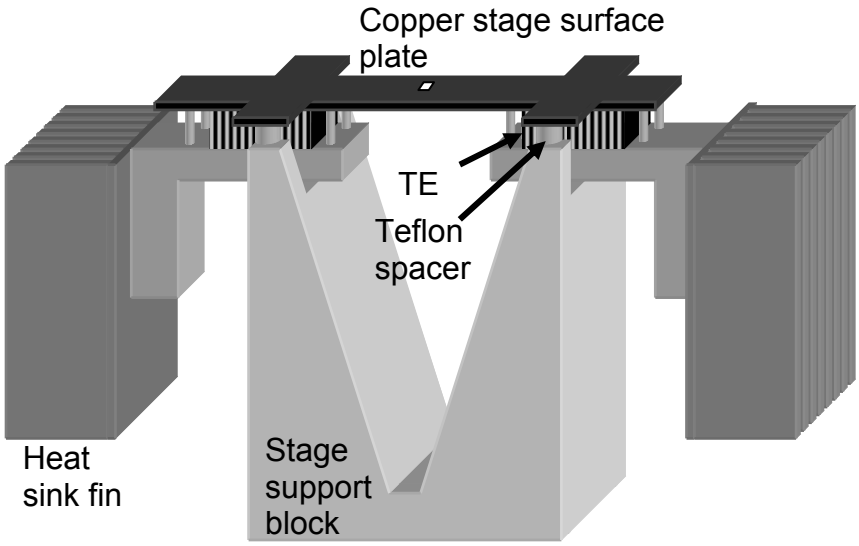

Figure 6.5. Schematic representation of the measurement stage developed for optical pumping.

Figure 6.5 shows a schematic drawing of the system measurement stage. The measurement stage design is critical because it has a profound impact on the thermal properties of the stage, and the reproducibility of the measurements.

The stage was designed to decouple thermal changes in the test temperature and the heat sink temperature from the positioning of the DUT. This decoupling was accomplished by mounting the stage surface plate with thermally insulating Teflon spacers to the stage support block and using separate heat fins for dumping heat to, and absorbing heat from, the room. This arrangement is in stark contrast to the configuration used by many measurement stages, where the stage support block is also used as the thermal heat sink. In these traditional configurations, as the stage temperature is changed using the integrated thermal-electric coolers (TECs), heat from the stage is pumped in and out of the stage support block. This heat causes the stage support block to change temperature and expand and contract, shifting the position of the stage surface plate and the DUT. In optically-pumped testing, this position shift is not acceptable and the newly developed configuration does not pump heat in and out of the stage support block. Instead, heat passes through to heat fins mounted via TECs to the stage surface plate, and their expansion and contraction has no impact on the sample position. To minimize the effects of changes in the temperature of the stage surface plate itself, the DUT is placed in the middle of the plate, equidistant from the four Teflon mounting bolts. Thus stage surface plate expansion and contraction has a minimal impact on the centered sample position. To avoid unnecessary vibration, the heat sink fins have fans that are automatically operated only if the fin temperature becomes too high for effective

heat sinking (~50 °C). In practice, the fans only operate when the stage temperature is reduced more than 50 °C per minute.

The DUT is optically pumped from the bottom of the stage surface plate via a 4 mm square hole in the plate. The focused pump laser light is delivered via an optical fiber and a fiber focuser that is held below the stage surface plate in an opening in the stage support block. The lens position only needs adjustment during initial setup and is angled so the spot on the DUT is circular and so the position of the spot on the DUT will not shift as the DUT and the stage surface plate is moved up and down (z-axis). This configuration greatly simplifies testing because it allows the pump to be focused on the DUT by changing the DUT z-axis position with stepper motor accuracy and precision without concerns about the pump spot "walking off" the VCSEL aperture as the DUT height is changed.

The detector used is a two-color detector and is made of a germanium detector placed behind a silicon detector. In this configuration, the front silicon detector is used to measure the amount of 980-nm pump light present while the longer wavelength VCSEL emission passes through to the germanium detector. The responsivity of the Ge detector to emission near 1540 nm is 0.52 A/W, and the responsivity of the Si detector to 980-nm emission is 0.62 A/W. A small amount of 980-nm light leaks through the Si detector and is detected by the Ge detector. With the amount of 980-nm pump light present known, however, this

leakage is accounted for in the analysis software and its effect is removed. Even without this correction, only a few micro-amps of unwanted photo-generated current occur.

The pump laser is a fiber pigtailed, packaged, and TEC temperature controlled EDFA pump laser. The pump light is delivered to the VCSEL via a focusing lens. Back-reflection from the VCSEL substrate can interfere with the operation of the pump laser so an in-line fiber attenuator is used to drop the round trip back-reflection an additional 10 dB to minimize the impact. The pump laser current determines the intensity of the light delivered to the VCSEL and is controlled by the main program. Prior to testing a VCSEL wafer, the pump laser output power is characterized and stored by the program. The stored 980-nm pump power vs. current information is used later to determine the amount of pump light actually absorbed by the sample during light-out vs. light-in testing.

Typical measurement procedures involve moving the measurement detector out of the way of the camera every time a new region of the wafer is to be tested. In addition, to measure the VCSEL spectrum, a fiber probe is required directly above the VCSEL in place of the photodetector. To facilitate rapid testing, the photodetector, the fiber probe, and a lensed fiber focuser (for future high-efficiency emission collection), were all mounted to a slide rail so they could quickly be moved in and out off the VCSEL emission path. Thus,

switching measurement modes takes only a few seconds. The rail can also be used to move all the measurement devices away from the DUT for microscope viewing and to remove the sample from the stage.

The stage motion is controlled by piezoelectric actuators and stepper motors. Piezoelectric motion control was required to achieve the sub-micron in-plane positioning precision required to ensure that the pump beam is precisely aligned to the VCSEL aperture. If this alignment is off-axis, then gain in the VCSEL does not overlap well with the VCSEL lasing mode and the VCSEL lasing threshold appears to increase. In addition, at pump levels well beyond those needed to reach lasing threshold, if the pump drifts off-axis, the shift in position of the optically-generated carriers can promote improved efficiency of higher order lasing modes and affect the side-mode suppression ratio (SMSR) of the VCSEL emission spectrum. Modal properties of the VCSEL will be discussed in more detail in Section 6.2.

To align the VCSEL and the pump beam, the stepper motors (1-μm precision) are manually controlled through the program to position the pump beam on the VCSEL of interest (see Figure 6.3). Once the coarse, manual alignment is done, the program can be used to automatically search for the optimum alignment position. This accomplished through automated stepping of the stage position while simultaneously measuring VCSEL emission power (essentially a form of raster scanning). The test system typically takes about 3

measurements per second. The program then moves the stage to the position of peak VCSEL output power. Figure 6.6 shows the output data from the completed automated scan, as plotted in Matlab. The central peak in the figure is the position of the VCSEL aperture, and the round mesa surrounding it is the spontaneous emission from the VCSEL active region as it appears when blocked by the circular gold optical-pumping target. The smaller peak to the right in the figure is located in a region of the VCSEL were the pump power is sufficient to induce lasing, but it does not correspond to the VCSEL aperture.

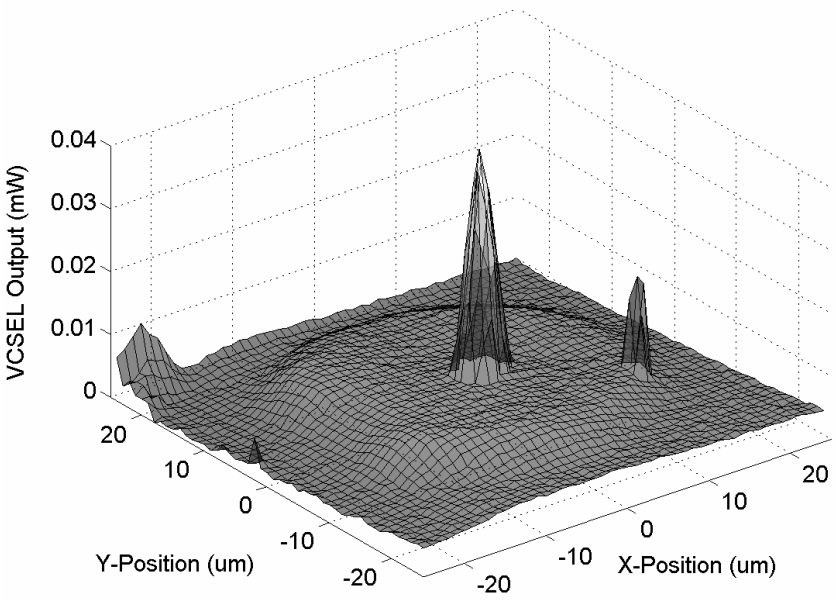

Figure 6.6. Measurement system automated VCSEL/pump alignment routine output, as plotted in Matlab. The central peak indicates the position of the VCSEL aperture.

Once the VCSEL aperture has been located, manual control of the piezoelectric stage motion is used to optimize the VCSEL/pump alignment. To ease this process, a special motion control zoom-and-pan feature was

implemented. This feature allows the operator to incrementally increase the motion precision of the piezoelectric control by zooming in and out using the program panel. The operator can then move with the set precision and pan the pump beam around the sample until the VCSEL output power is peaked, indicating optimized VCSEL/pump alignment. This zoom-and-pan motion control technique is analogous to trying to select a pixel in a digital photograph by clicking the mouse to zoom in and out and panning by using the screen scrollbars.

With the VCSEL/pump alignment complete, the DUT height is adjusted to place the VCSEL aperture at the beam waist of the focused pump laser beam. This is accomplished using an automated routine that sweeps the DUT height and measures the VCSEL output power. The peak VCSEL output power (when the device is operated near threshold), is taken to coincide with the highest pump light density and hence the narrowest beam waist of the pump. The program then places the VCSEL aperture at the pump beam waist. Figure 6.7 shows the plotted output of such a scan. After the z-height has been optimized, the in-plane position optimization is typically checked to ensure the VCSEL/pump alignment has not changed.

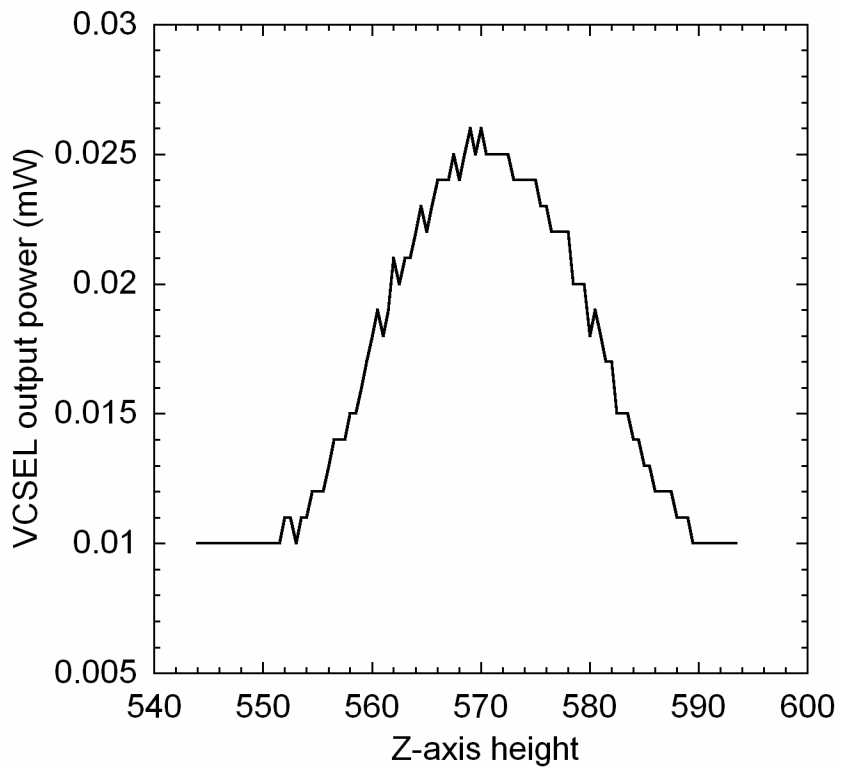

Figure 6.7. Plot of VCSEL output power near lasing threshold as a function of the height of the stage. The VCSEL output power changes as the pump power density changes. The peak occurs at the beam waist of the focused pump spot.

Once all three-axis of VCSEL/pump alignment is complete, the light-out vs. light-in properties and the emission spectrum (at various currents) of the device can be measured at the specific stage temperature. The spectrum is measured by aligning the fiber probe to the VCSEL using the microscope video image and bringing the fiber into an Optical Spectrum Analyzer (OSA). The light-out vs. light-in properties are automatically measured by the control program using the two-color photodetector, two program-controlled multimeters, and by automatically sweeping the current to the pump laser. The data generated by this light-out vs. light-in measurement is shown in Figure 6.8.

The data is stored by the program in a table format. The next two sections will describe the ways in which this data can be analyzed to determine the required light-out vs. light-in properties.

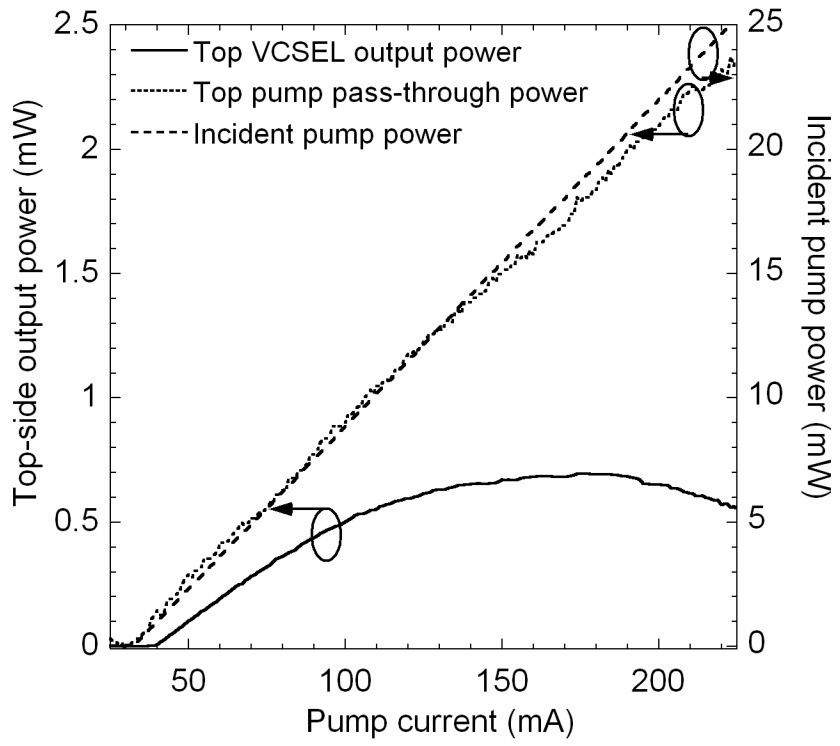

Figure 6.8. Plot of light vs. current data generated by the automated measurement routine of the test system.

The stability and reproducibility of the measurement system allows devices to be accurately located, tested, and if need be, relocated and retested with the same results. This system made it possible to take the large amount of date required to fully characterize the CW properties of the optically-pumped CWDM VCSEL arrays of this work.

6.1.2 Absorbed Vs. Incident Pump Power

The data in Figure 6.8 does not explicitly give the light-out vs. light-in properties of the VCSEL. However, by knowing the pump power incident on the sample vs. the pump current and the VCSEL power emitted vs. the pump current, the VCSEL light-out vs. the Pump light-incident can be determined. With the additional knowledge of the intensity of the pump light leaking out the top of the VCSEL, the actual pump light absorbed in the sample can be estimated. This estimation is simple in the case of VCSEL active regions with high single-pass pump absorption efficiencies, as is the case in this work. Chapter 4 gives the single-pass absorption efficiencies of these designs near 80% based on the thickness of the pump absorbing layers (neglecting superlattice absorption). With high single-pass absorption in the active region, multiple passes and reflections of the pump light can be neglected without a loss of accuracy. Figure 6.9 shows the reflection of the pump at the top and bottom air-semiconductor interfaces. If the semiconductor has no antireflection coatings and if scattering is neglected, the pump power intensity P_4 is less than 1% of the P_{in} intensity as given by Equation 6.1 (R_1=R_2=0.31, L_1=80%) and only 1.2% of the pump power at P_1. Thus, it can be assumed that any pump power that enters the VCSEL substrate (P_1) and does not leave the top of the VCSEL is absorbed by the active region. If R_1 and R_2 are known, it is also

simple to estimate the actual single pass absorption of the active region based on Equation 6.2.

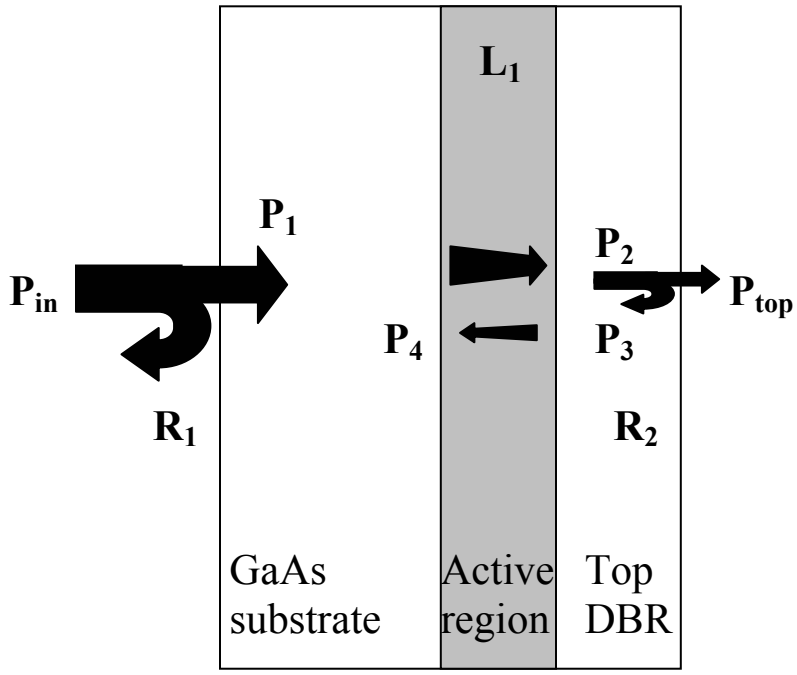

Figure 6.9. Schematic showing relevant pump reflections and losses.

$$(6.1)\ \frac{P_4}{P_{in}} = R_2 \cdot (1 - R_1) \cdot (1 - L_1)^2$$

$$(6.2)\ L_1 = 1 - \frac{P_{out}}{P_{in} \cdot (1 - R_1) \cdot (1 - R_2)}$$

With such straightforward relationships between the pump power incident on the bottom of the sample, the pump power exiting the top of the sample, and the pump power absorbed in the active region, it is more instructive to analyze the VCSEL measurement data with respect to the estimated pump

power absorbed in the active region than with respect to the pump power incident on the active-region substrate. This method of analyzing the VCSEL results will be used throughout this chapter.

For an accurate estimate of the actual pump power absorbed in the VCSEL active region, it is still necessary to have the R_1 and R_2 reflectivities at the pump wavelength of 980 nm. Chapter 5 described the processing of the VCSEL array and the back-side substrate polish that was used. Chapter 5 also described the 1540-nm antireflection coating that was used on the top and bottom of the sample. The topside of the sample is epitaxially grown and selectively chemical etched and is considered to have a nearly perfect surface quality. Thus, its reflectivity at 980 nm is modeled using Vertical and estimated to be 21%. The bottom side is manually polished and has more scattering loss associated with it. In order to estimate the backside reflectivity at 980 nm, the VCSEL array was tested prior to the antireflection coatings and a perfect 31% backside reflectivity was assumed (all scattering loss was neglected). The sample was antireflection coated and measured again. The two data sets were compared and the new backside reflectivity was fit until the data sets matched. This technique, though far from perfect, estimated the backside reflectivity at a new value of 28%. No accounting is made for the imperfect polish on the backside.

Based on this technique, actual device testing from the completed CWDM VCSEL array estimates the single pass pump absorption at about 83 % and the total pump power absorbed at about 87 %. These values neglect the backside reflection and again, do not account for scattering loss.

6.1.3 Automated Analysis Routine

Having developed a capable test system and an understanding of the relationship between the measured pump power and the pump power actually absorbed in the active region, all that remained in the test development process was the development of an automated data analysis program. To this end, a Matlab script was created to automatically interpret the data generated by the test system and calculate the relevant light-out vs. light-in parameters with respect to the total absorbed pump power.

Figure 6.10 shows the output of the script. The script automatically generates linear fits to the data above and below threshold and uses the intercept to find the precise threshold value. The script accounts for the sample reflectivities at 980 nm and calculates the relevant parameters with respect to the absorbed pump power. The data generated by the script is output to the screen and a data file. The parameters extracted include: single-pass pump absorption, total pump absorption, threshold pump power, differential efficiency, peak

VCSEL output power, and pump power at the peak VCSEL output power. The results of the CWDM VCSEL array testing will be presented in section 6.3.

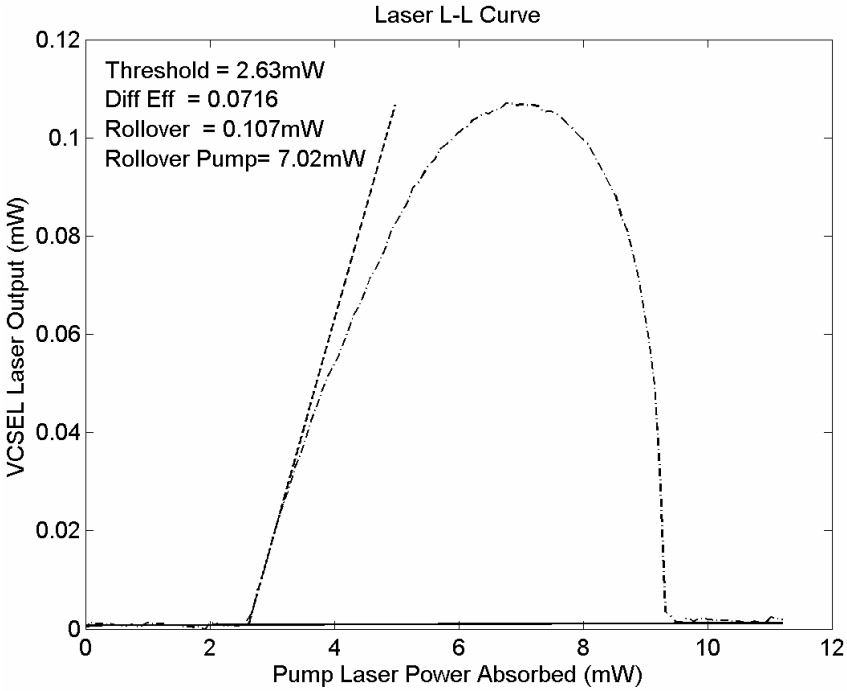

Figure 6.10. Matlab script output plot showing the automatically generated fits for the above and below threshold data.

6.2 Index Guiding For Optically-Pumped, Single-Mode, VCSELs

Controlling the single-mode lasing spectrum of optically-pumped VCSELs for CWDM applications is critically important. Chapter 4 discusses the design of an air-gap annulus for modal confinement in the structure. In this section, the strength of the index guide and its effect on the spectral quality is discussed. In addition, the strength of the index guide was found to have a dramatic effect on

the shape of the light-out vs. light-in data from the measured devices. This effect is discussed and a plausible explanation and solution is presented.

6.2.1 Weakly Confined VCSEL Hysteresis

Generally, a weaker strength index guide is desirable to create a VCSEL waveguide capable of only supporting a single lasing mode. Fundamentally, as the index guide becomes weaker, the mode becomes larger and the overlap with the gain profile of the active region is reduced. In the optically-pumped VCSELs of this work, this effect was very pronounced and led to undesirable hysteresis in the VCSEL operation.

Figure 6.11 shows the results of light-out vs. light-in (or pump current) testing for a device with an estimated V-parameter strength of 2.1. With this V-parameter, as discussed in Section 4.3, only a single transverse mode is supported. Such a single-mode waveguide would normally be desirable for applications requiring single-mode sources. Unfortunately, as is visible in Figure 6.11, the device has a sharp turn-on behavior that is not suitable for direct-modulation operation. The VCSEL does operate with most power in a single longitudinal and transverse mode as shown in Figure 6.12 (two polarization modes exist in this device).

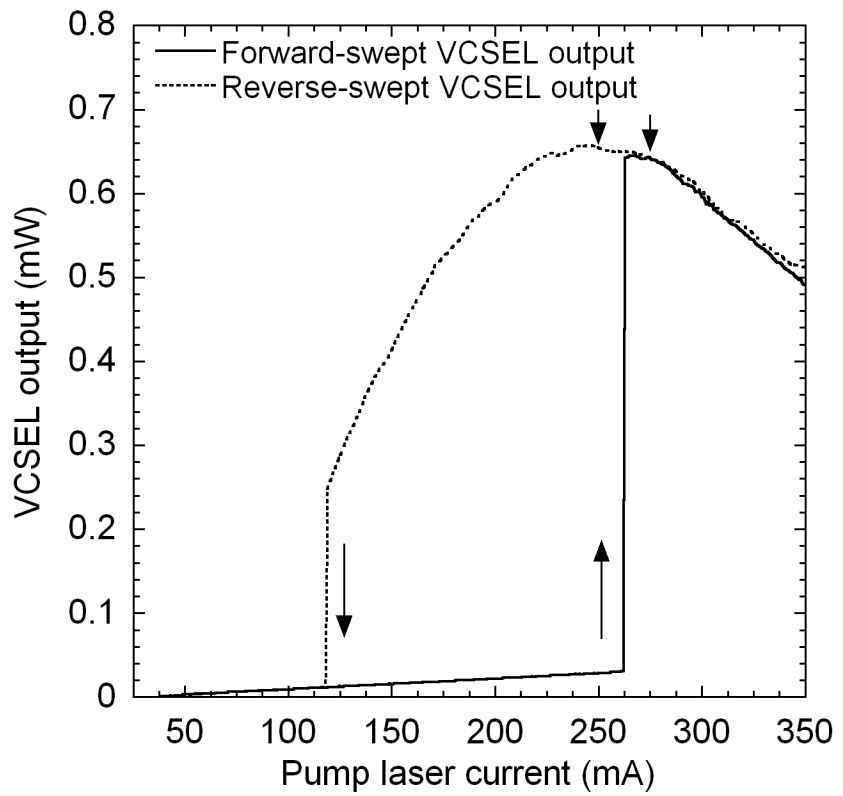

Figure 6.11. Light-out vs. pump current for a channel-1 device (about 1470 nm) with an index guide strength of about 2.1. Note the difference in the forward-swept and reverse-swept pump input.

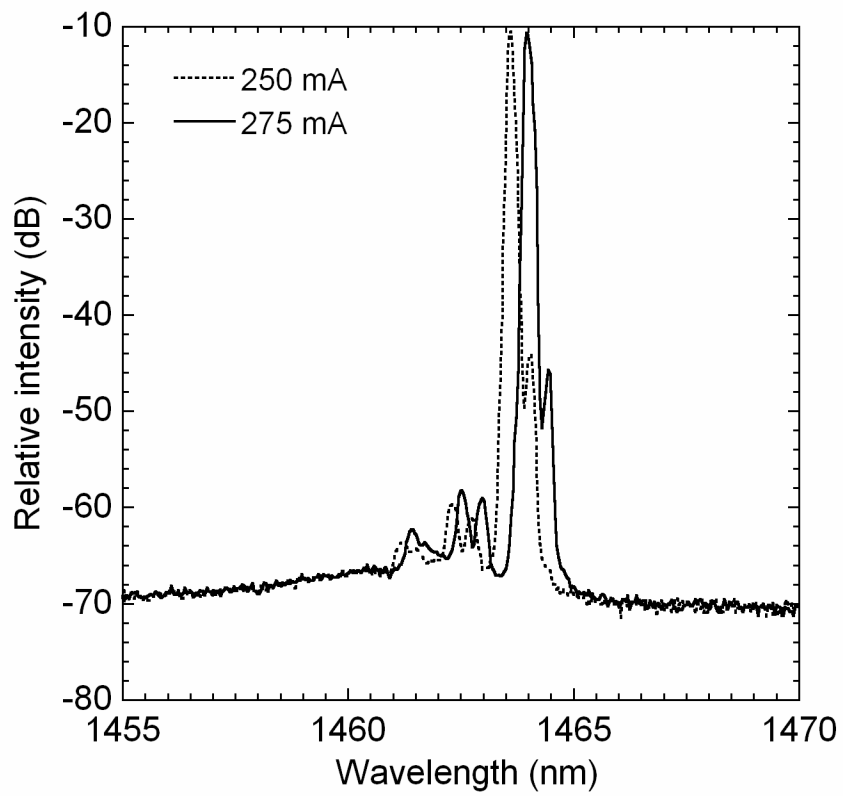

Figure 6.12. Spectra from the same channel-1 device in Figure 6.11 at two different input drive currents corresponding to two different pump input powers. The two currents correspond to the arrow positions shown in Figure 6.11.

As was discussed, Figure 6.11 shows the light-out plot from a VCSEL with a V-parameter of 2.1. Two traces are shown; the solid line corresponds to sweeping the current to the pump laser, and hence the pump input power to the VCSEL, from low to high, and the dashed line corresponds to the VCSEL output when the pump light is swept from high to low. There is a drastic difference in the VCSEL performance under forward and reverse swept conditions. This result is reproducible and occurs for all the optically-pumped

VCSELs with index guide strengths lower than about 2.5. Unpublished results from Gore Photonics also verify this result.

The explanation for this behavior is simple and related to the overlap between the gain and the lasing mode. If fiber theory is used to analyze the VCSEL mode behavior, the electric field distribution of the fundamental lasing mode in the VCSEL waveguide can be approximated by a Gaussian distribution. The radius of the field mode can be approximated by Equation 6.3 (very accurate for 1.2<V<2.4) [1]. For a V-parameter of 2.1 and a waveguide radius (a) of 4 μm, the field radius (w) is about 4.9 μm. Considering the fact that the beam waist diameter of the 980-nm pump laser (r) is 2.5 μm, it is clear that the lasing mode does not overlap well with the gain from the optically-generated carriers in the active region. In fact, using Equation 6.4 [1], the overlap factor of the mode with respect to the pump beam is only 0.41.

(6.3) $$w/a \approx 0.65 + 1.619 \cdot V^{-3/2} + 2.879 \cdot V^{-6}$$

(6.4) $$\Gamma = 1 - \exp\left(-\frac{2 \cdot r^2}{w^2}\right)$$

With poor overlap of the fundamental guided mode with the pump spot, the tails of the guided mode will experience loss from the area of the active

region with a radius larger then the radius of the pumped region. The outer, un-pumped areas will not reach transparency until enough carriers diffuse from the central pumped region. Thus, until the VCSEL is pumped hard enough to cause a sufficient number of carriers to spill out of the central pumped region, the under-pumped active-region areas will continue to act as absorbing regions and create too much internal loss for the VCSEL lasing mode to reach threshold. When sufficient carriers spill from the central pumped region to the outer regions, the internal loss of the device drops, and the lasing mode is allowed to turn-on. At this point, the internal loss is now lower, and the VCSEL immediately consumes the excess carriers that had been accumulating in the central portion of the active region and begins to operate on a differential efficiency slope defined by the new internal loss value. This behavior explains the sharp VCSEL turn-on under forward-swept pump operation.

Once the VCSEL has turned on and is operating with a new internal loss value, the tails of the large diameter lasing mode become responsible for continuing to pump to transparency the active-region material not pumped by the external pump laser. If the VCSEL is now operated in the reverse swept direction, the VCSEL lasing mode will continue to lose power by pumping the active-region material that overlaps with the mode tails. Because the lasing mode is capable of pumping these regions and maintaining device transparency, the VCSEL continues to operate above threshold well below the pump current

level associated with the sharp turn-on of the forward-swept condition. This behavior explains the operation of the VCSEL under reverse-swept pump operation.

This VCSEL behavior leads to hysteresis in the VCSEL output and is a result of the poor overlap between the pump spot size and the lasing-mode diameter. This poor overlap results in the un-pumped active-region material acting as an absorber until pumped to transparency by either carrier diffusion (forward swept) or the lasing mode of the VCSEL (reverse swept).

6.2.2 Index Guide Strength and Modal Behavior

The previous section described the undesirable performance of VCSELs with weak index-guide apertures. Section 4.3 described the design of the CWDM VCSEL array to provide 4 index guide strengths per VCSEL wavelength. Thus, for testing purposes, the key is to select the VCSEL with index guide strong enough to avoid the sharp turn-on behavior, but weak enough to suppress higher order lasing modes. Fortunately, the small spot size of the pump laser aides in this task because it naturally provides improved spatial gain-mode overlap for the fundamental lasing mode and thus helps to suppress higher order modes. This is particularly true a low pump powers. At high pump power, enough gain is available that the mode suppression ratio is degraded if the waveguide is too strong and the higher order modes too well confined. In subsequent sections,

devices results will be presented. The results presented are from devices selected to balance the need for single-mode operation and the need for well behaved light output characteristics. This is accomplished by selecting the device with the proper amount of modal confinement.

Figure 6.13 shows the light-out vs. the absorbed pump light for three different strength index guides for wavelength channel 2 of the array. A fourth, weaker guided VCSEL was available (V=1.54), but the mode-gain overlap was too weak to reach lasing threshold (as described in Section 6.2.1). The estimated V-parameters for the R2, R3, and R4 devices are given in Section 4.3 and are 2.32, 2.97, and 3.41. As is evident form the Figure, the R2 waveguide is too weak to provide sufficient special mode-gain overlap and the characteristic sharp turn-on is visible. R3 and R4 do, however, provide sufficient confinement and are good candidates for selection for further testing.

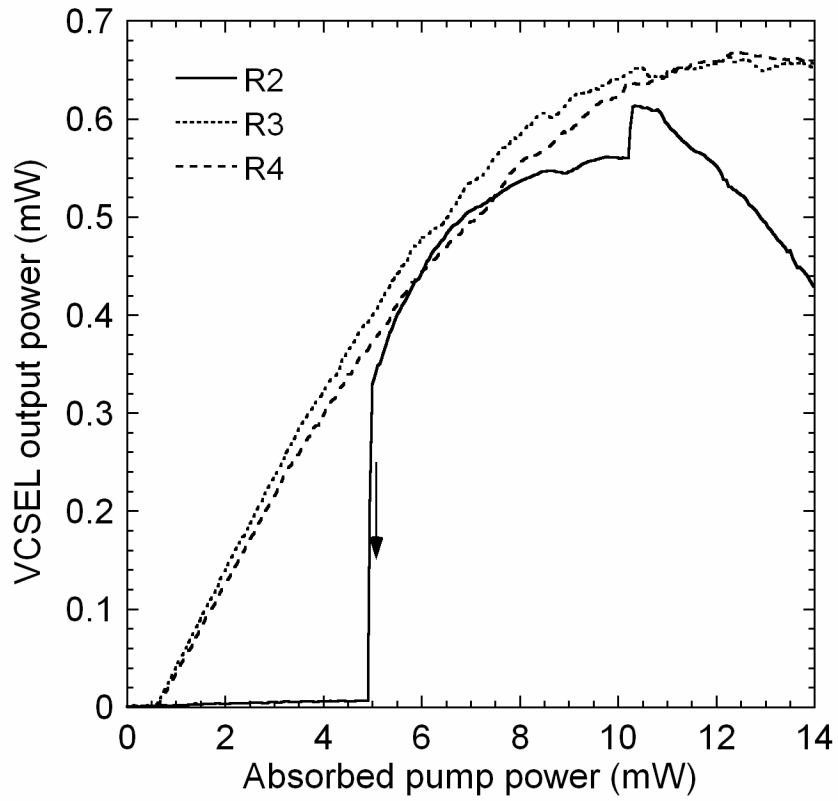

Figure 6.13. VCSEL light output traces for three different waveguide confinement strengths (R2<R3<R4).

After evaluating the light output power characteristics of the VCSEL wavelength channel, it is necessary to select the proper modal structure. Figure 6.14 shows the light output spectrum of the same R2, R3, and R4 confined VCSELs at 10 mW of absorbed pump power (about 0.6-mW VCSEL output power). As is evident from the figure, R2 is indeed a single-mode device. However, R3 and R4 however show multiple modes as is expected from the strength of their modal confinement. Fortunately, R3 is sufficiently single mode for the application, and at slightly lower pump powers maintains about 30 dB of SMSR. R4 shows poor SMSR through most of its operation range. As stated

earlier, the SMSR of R3 is enhanced due to the preferential pumping of the fundamental mode, through the use of a small pump laser spot size.

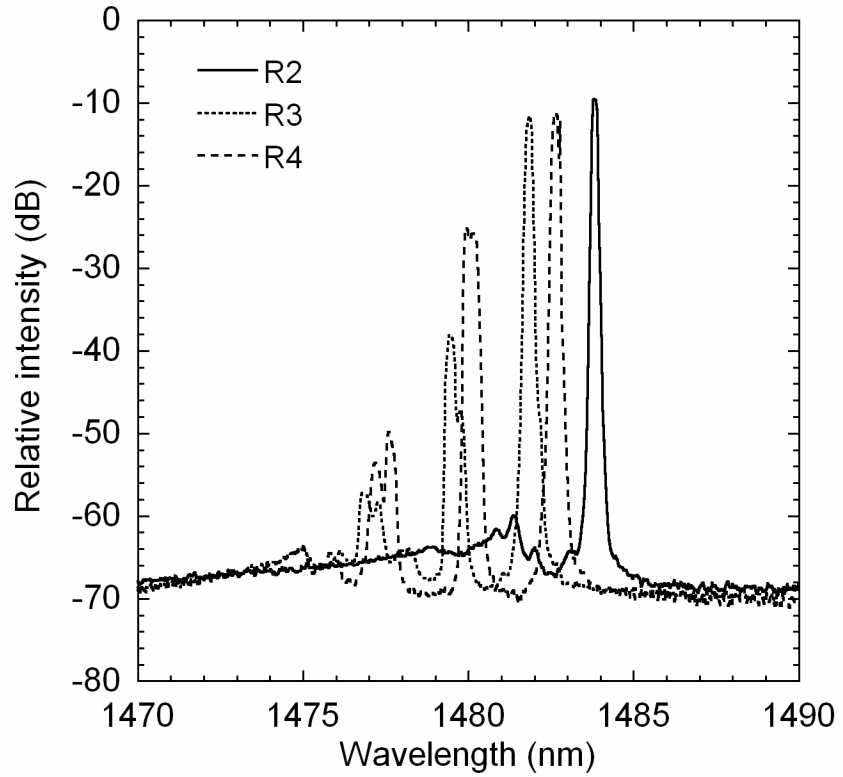

Figure 6.14. Emission spectra from VCSELs with three different strength modal confinement factors (R2<R3<R4).

Based on testing such as this, devices with modal confinement sufficiently strong for well behaved light-out vs. light-in characteristics, yet low enough for adequate SMSR, were selected. The results of testing these devices are presented in the following sections.

6.3 WDM Array Results

CWDM VCSEL arrays were designed, fabricated, and tested as described in the previous sections. The completed device arrays spanned 140 nm from 1470 to 1610 nm and all wavelength channels operated single mode and up to at least 65 °C. In this section, the CW test results from the completed array are presented. These test results include spectra and light-out vs. light-in testing. The test results will be discussed in the Section 6.5. All the test data is presented from a single array and is not an ensemble of the best devices from around the wafer. That being said however, because many densely packed devices are present on each array (as many as 600 per array) some selection was done within the array to find devices with the appropriate performance attributes. An example of this selection is choosing VCSELs with the appropriate modal confinement as described in Section 6.2.

6.3.1 Spectra

Figure 6.15 shows the superimposed lasing spectra from all eight channels of the array at 20 °C. The spectra were all recorded at the same absorbed pump power of 14 mW for each device. These VCSELs all use an index guide etch depth in row R2 (38 nm deep etch) (see Table 4.6) and most have model confinement factors too weak for well-behaved light-out vs. light-in characteristics. The average output power is -2.7 dBm at 14 mW absorbed pump power, and the

output power uniformity is +/- 1 dB. In addition, the minimum SMSR (Channel 4) is 45 dB. These devices operate well single-mode and may be best suited for CW applications were direct modulation is not required.

Figure 6.16 shows the 20 °C superimposed lasing spectra recorded from VCSEL devices with well-behaved light-out vs. light-in data (see Section 6.3.2). These devices had an average output power of -3 dBm at 7.5 mW of absorbed pump power. Their output power uniformity is +/- 1 dB and the minimum SMSR at this pump power is 36 dB. At higher pump powers the SMSR is reduced. These devices are best suited for applications involving direct modulation.

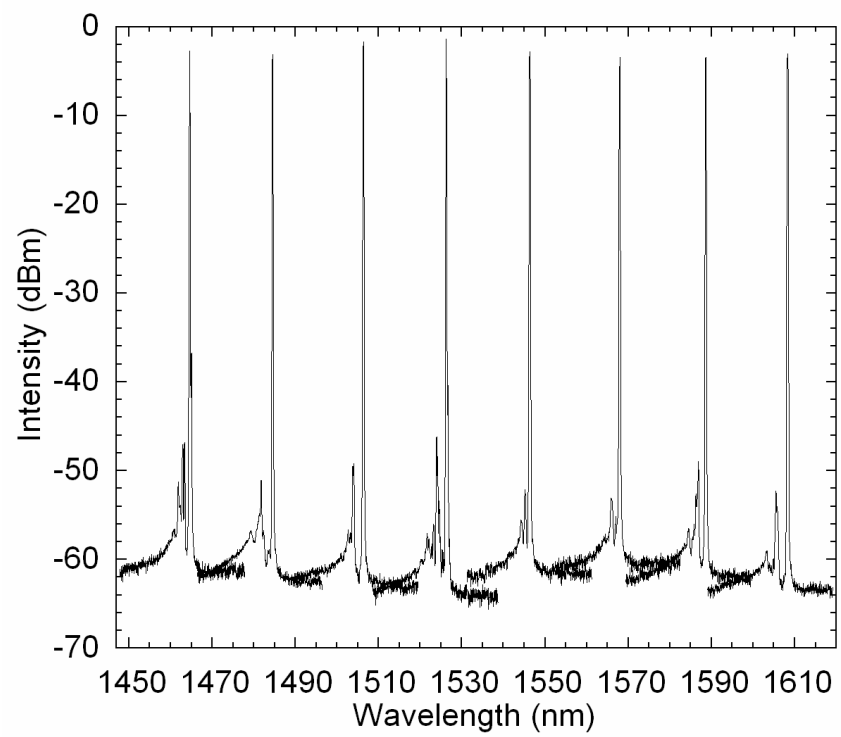

Figure 6.15. Superimposed lasing spectra from all eight wavelength channels at 14 mW of absorbed pump power and 20 °C. These devices are optimized for single-mode operation.

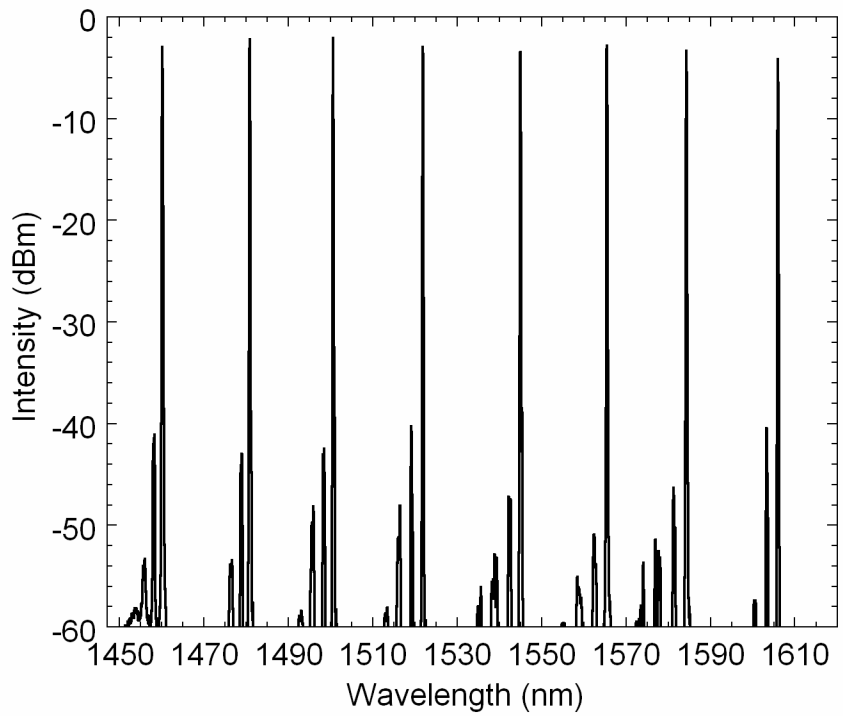

Figure 6.16. Superimposed lasing spectra from all eight wavelength channels at 7.5 mW of absorbed pump power and 20 °C. These devices are optimized for well-behaved light-out vs. light-in performance.

From Figures 6.15 and 6.16 it is clear that the Channel spacing is well controlled across the array and is almost exactly 20 nm between channels. This control is one of the principle features of the WDM array technology of this work. The actual wavelength of each channel is shorter than the target and this will be discussed in detail in Section 6.5.

6.3.2 Light-Out Vs. Light-In Over Temperature

The devices, whose spectra are shown in Figure 6.16, were selected for further testing because of their adequate single-mode behavior and their well-behaved light-out vs. light-in traces as shown for all eight channels at 20 °C in Figure 6.17. As started earlier, the devices had reduced SMSR at higher pump powers, and above 7.5 mW of absorbed pump power, the SMSR dropped below 36 dB. All channels operated to at least 65 °C with Channel 8 operating as high as 90 °C. Figure 6.18 shows the light-out vs. light-in plot for Channel 8. Specific attributes, such as peak output power, threshold, and differential efficiency, will be presented and discussed next.

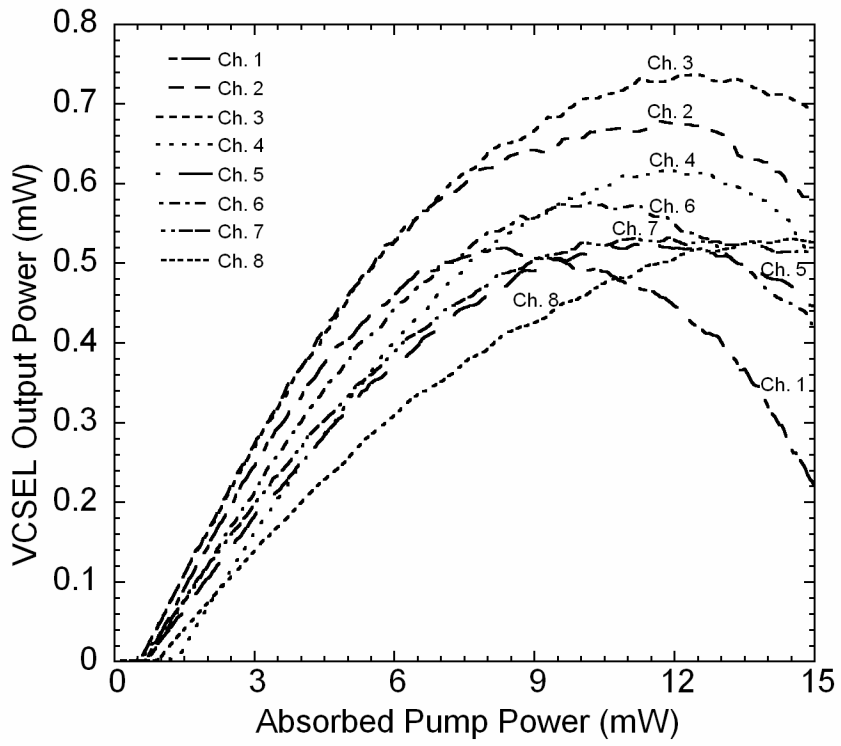

Figure 6.17. Light-out vs. light-in for the complete CWDM VCSEL array at 20 °C.

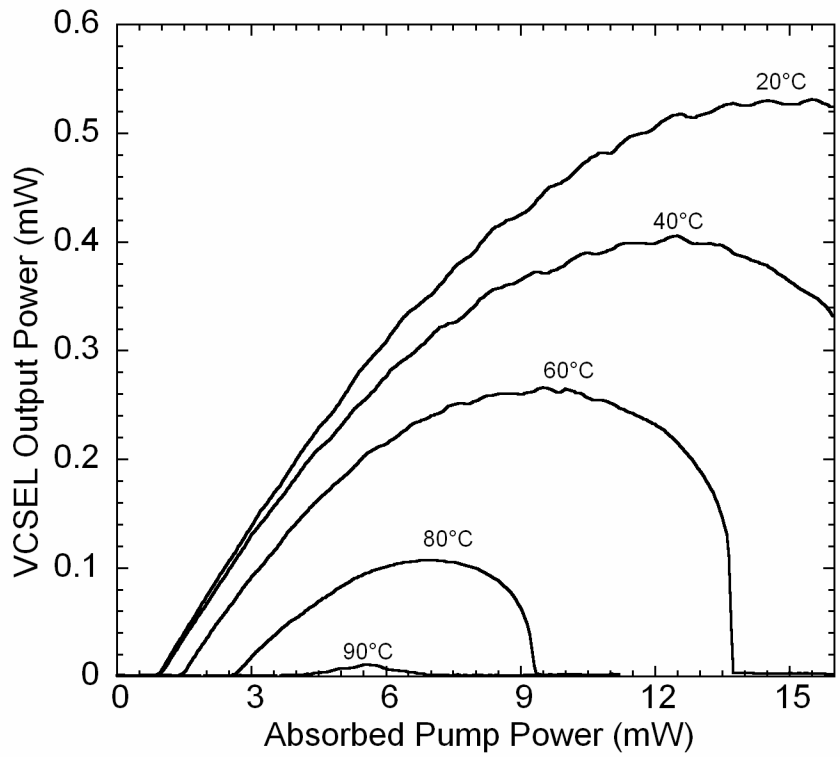

Figure 6.18. Light-out vs. light-in over temperature for Channel 8.

Based on the light-out vs. light-in data measured over temperature for each wavelength channel in the array, the data analysis routine (see Section 6.1.3) is able to extract and tabulate relevant device parameters. One area of interest is the peak output power from the elements of the array. Figure 6.19 summarizes the maximum output power for each wavelength channel over temperature. Based on this data, the peak output power drops linearly with increased temperature. Figure 6.20 shows the absorbed pump power required to reach the peak output power for each VCSEL over temperature. The trends for peak output power and the pump power required to achieve it are strongly

related to the thermal impedance of the devices, the gain-mode offset, and the depth of the carrier confinement in the active region. Section 6.4 will discuss the thermal impedance of the structures in more detail.

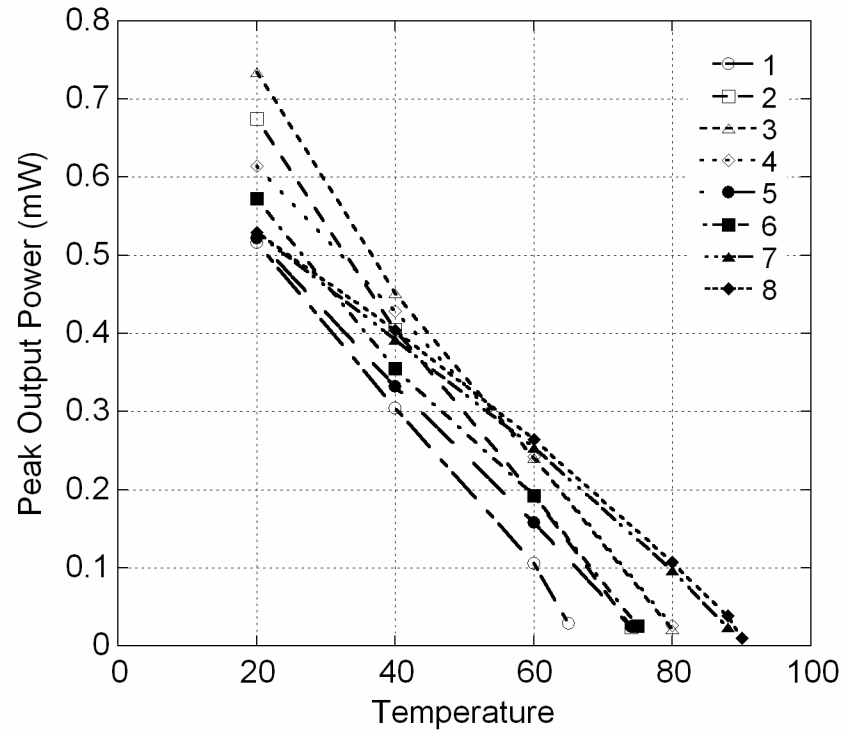

Figure 6.19. Plot of the peak output power from each VCSEL in the CWDM array over temperature.

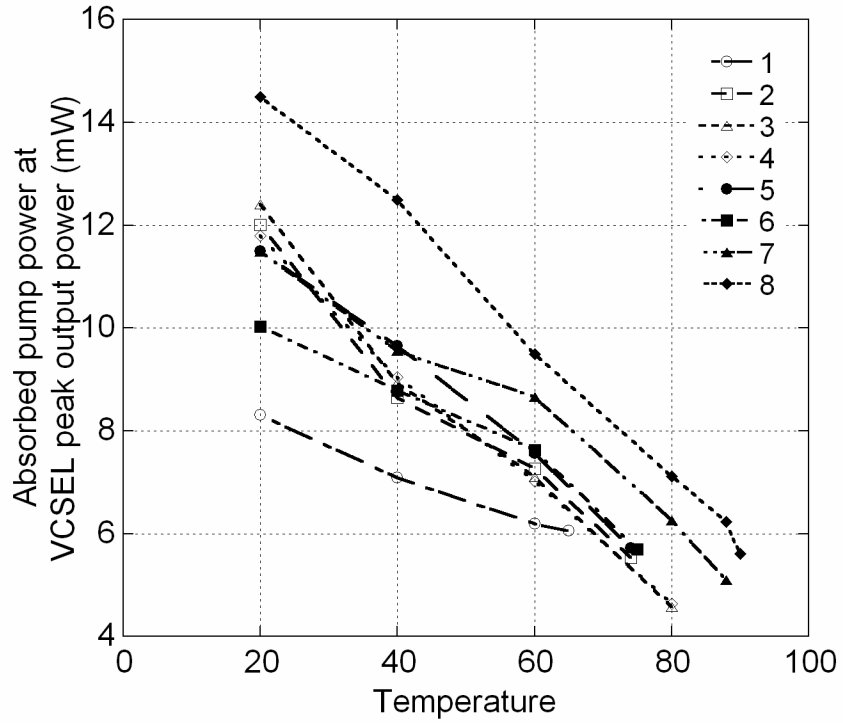

Figure 6.20. Plot of the absorbed pump power required to reach the peak VCSEL output power for each channel in the array across the operating temperature range.

Because the elements of the array exhibit total pump absorption efficiency of about 87%, less than 17 mW of pump power is required to reach the peak VCSEL output power if a 980-nm antireflection coating is used on the backside of the VCSEL array.

From Figures 6.19 and 6.20 several important observations can be made. It is evident that wavelength channels 3, 4, 7, and 8 have the highest operating temperatures. This result is due to the fact that the lasing wavelengths of these channels are longer than the gain peak of their associated active regions. Thus, as the temperature increases, the gain moves into alignment with the cavity resonance mode and improves the amount of gain available. This is discussed

more in Section 4.2.1 and is a well understood VCSEL phenomenon. Less obvious is the improved performance of channels 7 and 8. Figure 6.19 shows that these devices operate to about 90 °C, nearly 10 °C higher than channels 3 and 4. Because their gain-mode offsets are identical, this is not sufficient to explain the performance improvement. The reason for the increased performance is alluded to by Figure 6.20, where it is visible that channels 7 and 8 reach their peak output power at pump values 2 to 3 mW higher than channels 3 and 4 at 80 °C. In fact, at nearly all temperatures, Channels 5 through 8 have their peak output powers at higher pump powers than channels 1 through 4. This indicates that the VCSELs for channels 1 through 4 have already begun to shut off when 5 through 8 are still operating. The source of this improvement is the improved carrier confinement available in the quantum wells of the longer wavelength active region. Both active regions use the same barriers, so the longer wavelength PL quantum wells of the longer wavelength active region are deeper and can operate to higher internal temperatures before thermionic emission of carriers out of the wells becomes a serious problem. Thus, the deeper wells allow the devices to be pumped harder and reach higher operating temperatures.

Figure 6.21 shows the pump powers necessary to reach lasing threshold for all elements of the array over the operating temperature range. At 20 °C, the uniformity in threshold pump power is 0.75 +/- 0.38 mW. The effect of the

gain-mode offset difference of channels in the array is clearly visible in the figure. In fact this offset difference is the cause of the higher threshold of Channel 4 and the fact that its threshold reduces at higher temperatures. If Channel 4 is neglected at 20 °C, the threshold uniformity improves to 0.67 +/- 0.18 mW. The wavelength channels form natural pairs in the threshold plot. Channels with similar gain-mode offsets have similarly shaped threshold vs. temperature curves. These pairs have been highlighted in the figure through the use of the marker shapes. As an example, channels 2 and 6 (square) have trace shapes that nearly identical. This pairing was expected based on the lateral integration of two active regions used to fabricate the array.

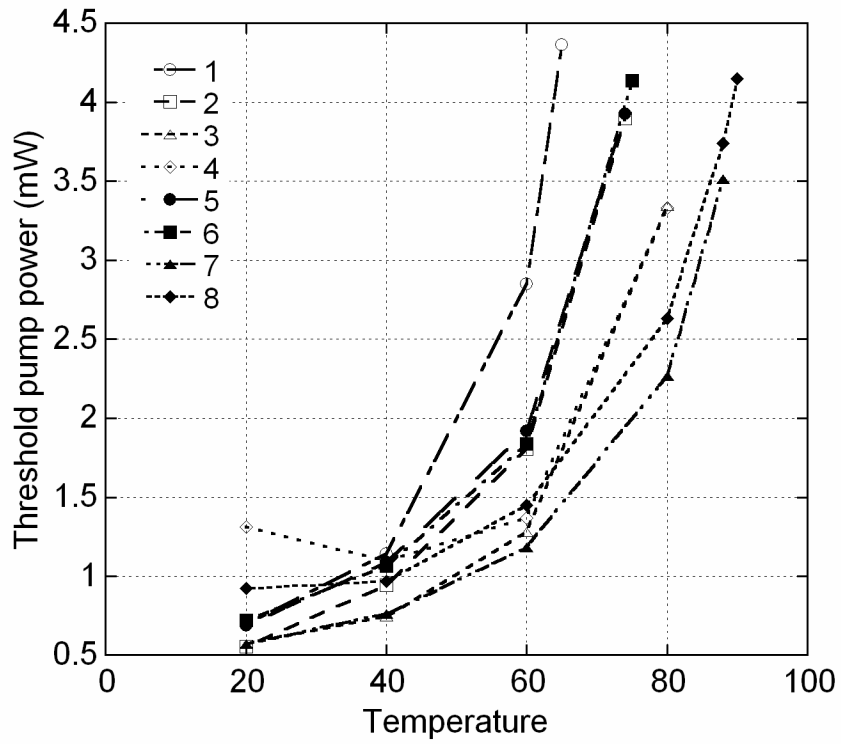

Figure 6.21. Plot of threshold pump power required to reach lasing threshold vs. the ambient stage temperature for all channels in the array.

Figure 6.22 shows the differential efficiency of each wavelength channel of the array across the operating temperature range of the array. There is more variation in the data than is desirable. The differential efficiencies are also lower that would be expected based on the data for the mirror reflectivity and the VCSEL design. If Channel 5 is used as an example and based on the mirror and active-region design, the total optical length of the VCSEL is about 1.48 μm (including 0.152-μm penetration into each mirror). Combined with the mirror design of Table 4.3, the mirror loss is about 6.34 cm^{-1} and a reasonable internal loss value is about 10 cm^{-1}. If the internal quantum efficiency is assumed to be 1, then the differential efficiency for Channel 5 should be about 0.39. This value is more than 3 times higher than the measured value of 0.123. The source of this discrepancy is not well understood and will require additional investigation. Optical pulse testing and more accurate values for the internal loss, internal quantum efficiency, and mirror reflectivity of the fully oxidized DBRs will be important to determine the source of the discrepancy.

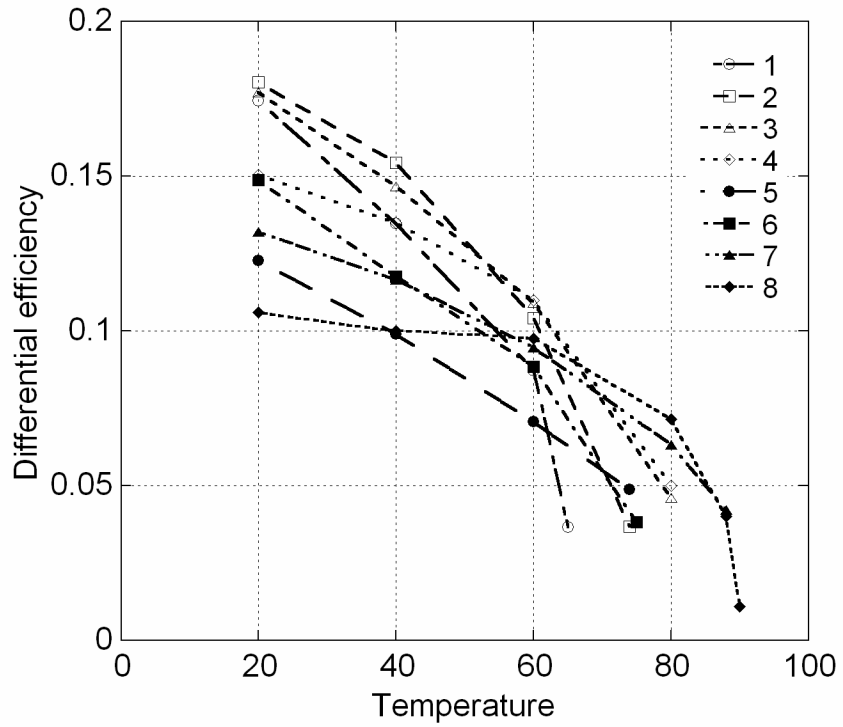

Figure 6.22. Plot of the differential efficiency vs. temperature for all wavelength channels in the CWDM array.

6.4 Thermal Properties

Thermal impedance describes the internal temperature rise of a VCSEL as a function of the amount of power dissipated by the VCSEL (input power less output optical power). This parameter is important in understanding the maximum lasing temperature of a device. The internal temperature of the device also influences the peak output power because it affects the peak power rollover position of the VCSEL. Because AlO_x is a thermally insulating material, its use in the mirror of the VCSEL structure has an impact on the

thermal impedance of the device. It is important to measure and understand the thermal impedance implications of the VCSEL design used in this work.

6.4.1 Thermal Impedance

In electrically pumped structures, heat can come from multiple joule heating sources, such as metal contacts and current spreading layers, and the total power dissipated in the actual active region is difficult to determine. This is not the case in an optically-pumped structure. In an optically-pumped device, accurate thermal-impedance measurements are easy to make because the sole heat source is located at the position of the optical pump beam and hence is defined by the area of the pump beam. The precise power dissipated is just the difference between the pump beam power and the VCSEL emission power, and all the power is dissipated right in the active region. Measurement techniques that analyze the active-region properties to determine the temperature rise can be very accurate for optically-pumped devices because all the heat is generated right at that point. The same techniques, when applied to electrically-pumped devices, can overestimate the amount of heat that is dissipated in the active area of the VCSEL and hence can underestimate the thermal impedance of the device.

A simple technique to measure the thermal impedance is to measure the wavelength shift of the output spectrum of the VCSEL under different operating

conditions [2]. First the VCSEL spectrum peak wavelength is measured under constant pump power but at different stage temperatures. Figure 6.23 shows this measurement for three different levels of dissipated power for Channel 4 of the

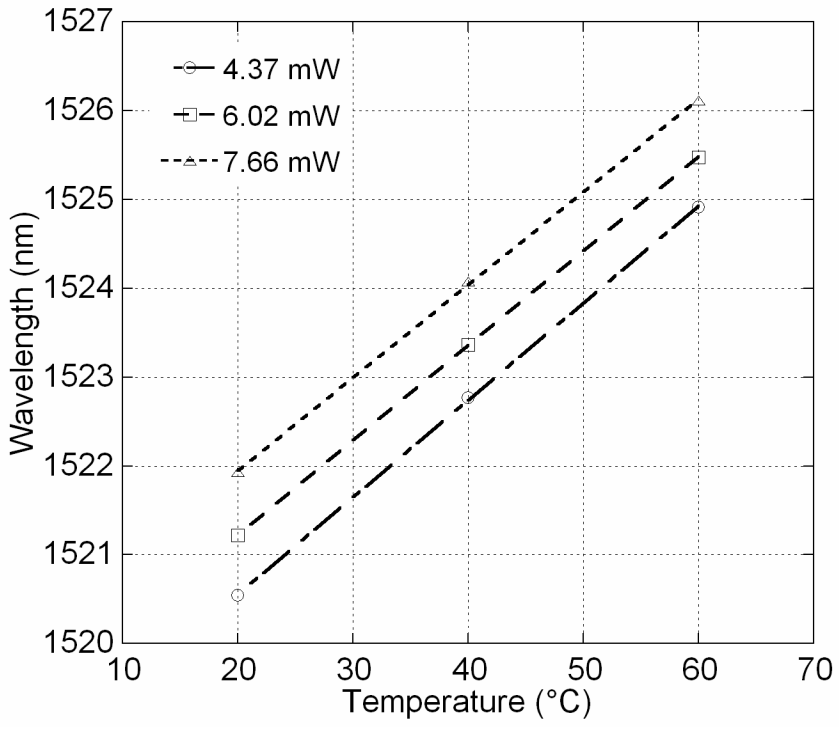

Figure 6.23. Plot of the wavelength shift vs. the stage temperature for three different levels of power dissipated in the VCSEL. The dashed lines represent linear fits to the data.

array. The slope of the linear fit to this data for the middle dissipated power level is 0.107 nm/°C and represents $\Delta\lambda/\Delta T$. Next, the VCSEL is held at a fixed stage temperature and pumped at different input power levels. The input power, less the VCSEL output power, determines the power dissipated in the device. The data for this measurement at three different temperatures is shown in Figure 6.24. The slope of the linear fit to this data at 20 °C is 0.437 nm/mW and

represents $\Delta\lambda/\Delta P_{dis}$. Because the thermal impedance is defined by $Z_T=\Delta T/\Delta P_{dis}$, the ratio of $\Delta\lambda/\Delta P_{dis}$ over $\Delta\lambda/\Delta T$ gives the thermal impedance of the device.

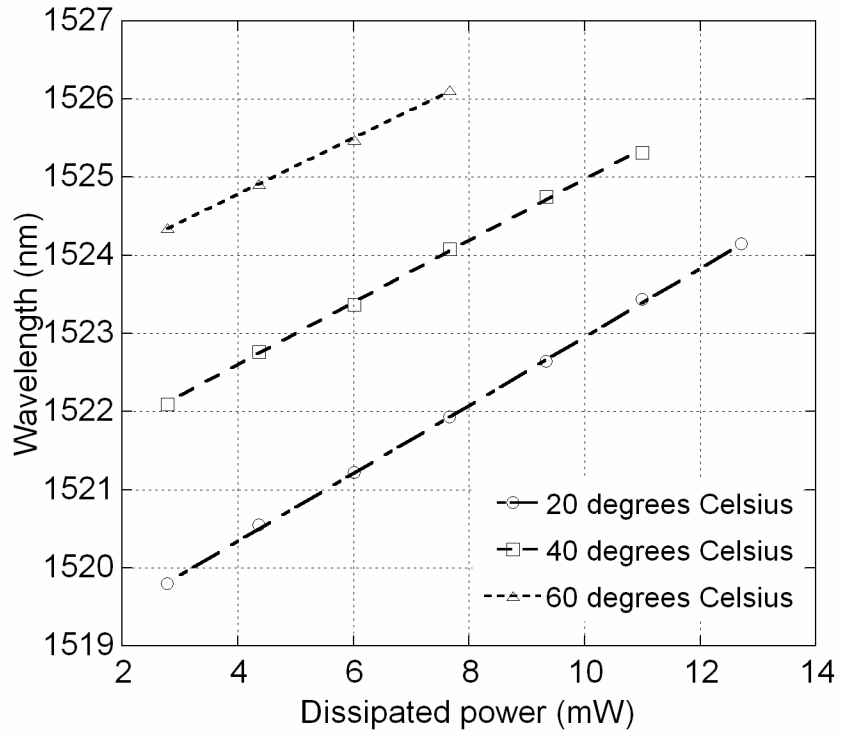

Figure 6.24. Plot of the wavelength shift vs. the power dissipated in Channel 4 of the VCSEL array at three different stage temperatures. The dashed lines represent linear fits to the data.

Figure 6.25 shows the results of the thermal impedance measurements at three different stage temperatures for all eight channels of the array for a dissipated power of about 6 mW. There is significant scatter in the data, but the trend is clear. The average thermal impedance at 20, 40, and 60 °C is 3.85, 3.68, and 3.19 °C/mW. The thermal impedance of the VCSEL drops with increasing temperatures.

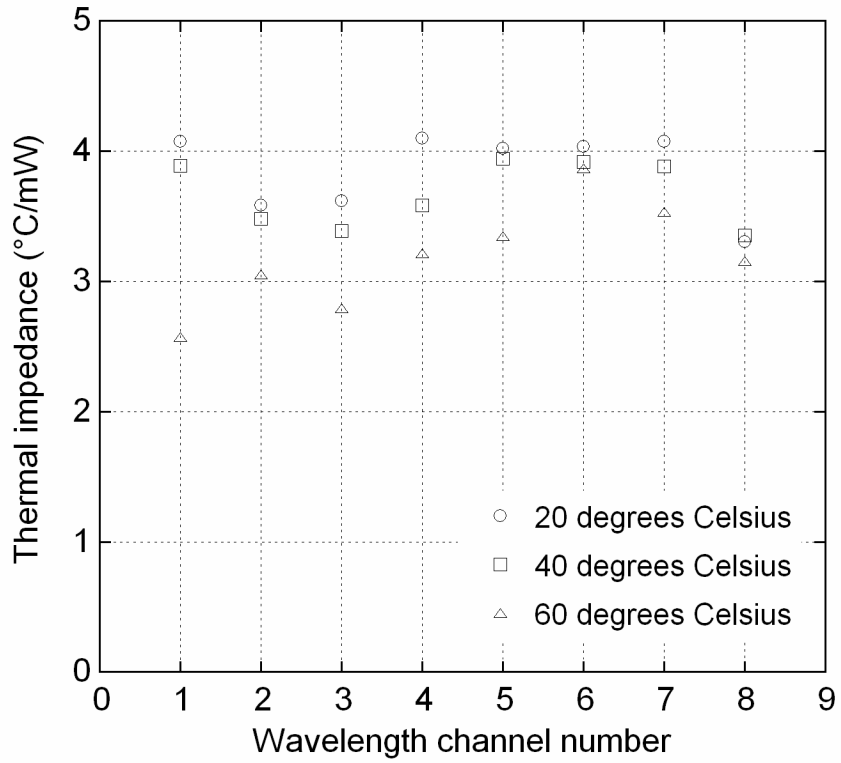

Figure 6.25. Plot of the measured thermal impedance values for all eight channels of the CWDM array at three different ambient temperatures (measured based on the 6 mW power slope as shown in Figure 6.23).

The thermal impedance value measured for these devices is about 160 to 300 % higher than other long-wavelength VCSELs with traditional AlGaAs DBRs. Double wafer-bonded VCSELs operating at 1550 nm and electrically pumped through graded composition DBRs have shown thermal impedance values of 2.4 °C/mW [3]. In addition, intra-cavity contacted electrically pumped 1.3-μm VCSELs using GaAs/$Al_{0.92}Ga_{0.08}As$ DBRs [4] have shown thermal impedance values of only 1.3 °C/mW [unpublished]. The long-wavelength VCSELs of this work would be expected to have higher thermal impedance than

traditional AlGaAs DBR VCSELs. The reason is the reduced thermal conductivity of AlO_x in the DBRs compared to AlAs. Other fully oxidized electrically-pumped DBR VCSELs operating near 980 nm have shown thermal impedance values near 2.7 °C/mW [2]. The quarter wavelength thick mirror layers designed for 1540 nm in this work are considerably thicker and can be expected to contribute to fully-oxidized DBRs with thermal-impedance values higher than their short-wavelength counterparts.

6.4.2 Thermal Conductivity

If a three dimensional heat flow model for a VCSEL is assumed, then the thermal conductivity of the VCSEL DBR and substrate is given by $\xi = (2 \cdot d \cdot Z_T)^{-1}$ [5], where d is the diameter of the VCSEL heat source (assumed to be 5 μm based on the pump beam waist). Based on this relation, the 6-period fully oxidized DBR on the GaAs substrate has a thermal conductivity of 0.26 W/cm-°C. The thermal conductivity of the AlO_x in the VCSEL mirrors is not known precisely, but an estimate based on typical values of Al_2O_3 is 0.3 W/cm-°C [6]. The GaAs layers in the mirror and the substrate are known to have a higher thermal conductivity of 0.45 W/cm-°C [5]. Thus, the DBR value calculated is below the values of either of its constituent materials and is lower than would be expected. The low thermal conductivity

value can result from a lower thermal conductivity value for the AlO_x than expected. In addition, graded AlGaAs composition layers are present in the mirror structure and alloy scattering causes these layers to have reduced thermal conductivity. Never-the-less, a value between the AlO_x and GaAs value would be expected due to the fact that the substrate below the bottom mirror is GaAs. The thermal conductivity issue will be discussed further in the next section.

6.5 VCSEL Internal Loss Analysis and Discussion

Based on the data measured in Section 6.3, it is possible to de-embed an estimate of the internal loss associated with the optically-pumped, double-oxide DBR VCSELs of this work. This parameter can be extracted by two different means and, as will be shown, both approaches yield similar values.

From Figures 6.21 and 6.22 we can see the threshold and the differential efficiency values for the VCSEL-array wavelength channels. Channel 2 and Channel 6 will be selected for analysis because the wavelengths of these channels are well aligned to the gain peak of their associated active regions at 20 °C. This alignment allows the use of gain data tabulated based on the peak gain as a function of current density. This data can be used for VCSELs with lasing wavelengths aligned with the peak gain of the active region. The gain data used is from Reference 7, and the quantum well structure used in this work is similar in structure to those used in the reference. The two-parameter fitted expression

for the gain data in Reference 7 is given by Equation 6.1 with g_0 and J_{tr} values of 583 cm^{-1} and 81 A/cm^2 respectively. Table 6.1 defines the parameters used in this section.

$$(6.1)\quad g = g_0 \cdot \ln J/J_{tr}$$

g_0	Two parameter empirical gain coefficient	583 cm-1 [8]
J_{tr}	Two parameter empirical transparency current density	81 A/cm^2 [8]
g	Material gain	
J	Current density	
η_d	Differential efficiency	
η_i	Internal quantum efficiency	1
α_m	Mirror loss	
$<\alpha_i>$	Average internal loss	
α_i	Internal loss	$<\alpha_i>$
m	Number of mirror periods	6
n_2	High index of DBR	3.378
n_1	Low index of DBR	1.537
m_{eff}	Effective number of mirror periods	
λ_0	Central DBR wavelength	1540 nm
Λ	DBR period length	
r	DBR interface reflectivity	
L_m	DBR penetration on one side	
L	Total effective VCSEL cavity length	
R_{top}	Top DBR power reflectivity	
R_{bottom}	Bottom DBR power reflectivity	
g_{th}	Threshold material gain	
Γ	Total modal confinement factor	
Γ_{enh}	Gain enhancement factor	
Γ_{fill}	Axial confinement fill factor	
Γ_{xy}	Transverse confinement factor	1
L_{active}	Total length of active gain material	
t_w	Quantum well thickness	
N_w	Number of quantum wells	3
$J_{th\ ref}$	Threshold current density per	

	reference quantum well	
$t_{w\ ref}$	Reference quantum well thickness	7 nm
J_{th}	Total threshold current density	
P_{th}	Absorbed threshold pump power	
A	Pump spot area	π x $(2.5\mu m)^2$
λ_{pump}	Pump wavelength	980 nm
q	Electron charge	1.602×10^{-19} C
h	Planks constant	6.626×10^{-34} J-s
c	Speed of light	3×10^{8} m/s

Table 6.1. List of parameter descriptions and values used for internal loss calculations.

The data in Figures 6.21 and 6.22 is scaled based on the actual pump power absorbed. All the optically generated carriers in the active region do not find their way to the quantum wells and do not have the potential to contribute to the generation of gain. Based on the active region analysis of Chapter 3, the average current density due to carrier recombination in the barrier regions can be calculated from the average carrier density in the barriers and the carrier lifetime in the barriers. This recombination current has been calculated to be only about 7 A/cm^2, and is small enough to be neglected. A more important contributor to the loss of carriers is lateral carrier diffusion. Carrier loss will be neglected in this analysis and all optically generated carriers will be assumed to find their way to the quantum wells.

From Figures 6.21 and 6.22 the threshold and differential efficiencies of Channels 2 and 6 are 0.56 mW and 18% and 0.72 mW and 15% respectively. The first way to de-embed the average internal loss is to use the differential efficiency data. Equation 6.2 describes the differential efficiency η_d as a function of the internal quantum efficiency, η_i (assumed to be 1 in this work),

the mirror loss α_m, and the average internal loss $<\alpha_i>$. Because the internal loss is assumed to be an average of the entire VCSEL cavity in this work, the average internal loss is defined as equal to the internal loss of the material, α_i.

$$(6.2)\ \eta_d = \eta_i \frac{\alpha_m}{\alpha_m + \langle \alpha_i \rangle}$$

To determine α_i from Equation 6.2, the mirror loss must be calculated. Equations 6.3 through 6.8 are used for this purpose. Equations 6.3 through 6.7 are used to determine the total length of the VCSEL cavity given the VCSEL DBR parameters [9]. The values of R_{top} and R_{bottom} for each VCSEL are given Table 4.3. For Channel 2 and Channel 6, the mirror losses are calculated to be 6.86 and 6.34 cm^{-1}. Thus, to achieve a differential efficiency value of 18 and 15%, the internal losses, α_i, are calculated to be 31 and 36 cm^{-1} respectively for Channels 2 and 6.

$$(6.3)\ m_{eff} = \frac{\tanh[m \cdot \ln(n_2/n_1)]}{\tanh[\ln(n_2/n_1)]}$$

$$(6.4)\ \Lambda = \frac{\lambda_0}{4n_1} + \frac{\lambda_0}{4n_2}$$

$$(6.5)\ r = \frac{n_2 - n_1}{n_2 + n_1}$$

$$(6.6)\ L_m = \frac{1}{2} \cdot m_{eff} \cdot \Lambda \cdot \left[\frac{1}{1 + r^2} - \frac{1}{2 \cdot m_{eff}} \right]$$

$$(6.7)\ L = 2 \cdot L_m + L_{cavity}$$

$$(6.8)\ \alpha_m = \frac{1}{L} \ln\left(\frac{1}{\sqrt{R_{top}}\sqrt{R_{bottom}}} \right)$$

An alternate way to de-embed the average internal loss of the VCSEL is to use the threshold information from the test results in Figure 6.21. Equations 6.9 through 6.15 are used for this purpose. Equation 6.9 describes the material gain required to reach lasing threshold as a function of the average internal loss, the mirror loss, and the gain region modal confinement factor for a generic laser structure. Again, equations 6.3 through 6.7 are used to calculate the effective mirror penetration for the fully-oxidized DBRs. Equations 6.10 and 6.11 are used to describe the modal confinement factor used for the gain [10]. In Equation 6.12, Equation 6.9 has been rewritten specifically for VCSELs.

Equation 6.13 uses the fitted gain function from Reference 7 to determine the threshold current density required for a quantum well of the thickness used in the reference. In Equation 6.14, the threshold current density is adjusted based on the specific design of the present VCSEL active-region structures. Equation 6.15 then uses the required threshold current density to calculate an equivalent absorbed threshold pump power, taking into account the actual internal quantum efficiency of the present VCSELs. With these expressions, it is possible to calculate the internal loss for the channel-2 and channel-6 devices. To achieve an absorbed threshold pump power of 0.56 and 0.72 mW, the internal losses are calculated to be 27 and 30 cm^{-1} respectively for Channels 2 and 6.

$$(6.9)\quad g_{th} = \frac{\langle \alpha_i \rangle + \alpha_m}{\Gamma}$$

$$(6.10)\quad \Gamma = \Gamma_{enh}\Gamma_{fill}\Gamma_{xy}$$

$$(6.11)\quad \Gamma_{fill} = \frac{L_{active}}{L}$$

$$(6.12)\quad g_{th} = \frac{1}{N_w \cdot t_w \cdot \Gamma_{enh}}\left[\ln\left(\frac{1}{\sqrt{R_{top}}\sqrt{R_{bottom}}}\right) + \alpha_i \cdot L\right]$$

(6.13) $$J_{th\_ref} = J_{tr} e^{g_{th}/g_0}$$

(6.14) $$J_{th} = \left(\frac{N_w \cdot t_w}{t_{w\_ref}} \right) \cdot J_{th\_ref}$$

(6.15) $$P_{th} = \frac{J_{th} \cdot A \cdot h \cdot c}{\eta_i \cdot q \cdot \lambda_{pump}}$$

The two different methods for de-embedding the internal loss of the double-oxide DBR optically-pumped VCSELs yield similar values. From the differential efficiency of the light-output data, Channel 2 and 6 have calculated internal losses of 31 and 36 cm^{-1}. From the threshold data for the two devices, the internal loss is calculated to be 27 and 30 cm^{-1}.

The threshold data calculation of internal loss is based on material gain curve fits from unstrained quantum wells [8]. Such wells have higher threshold current densities and lower gain than the 1% compressively-strained quantum wells used in this work. Thus, the analysis underestimates the amount of material gain for a given current density and hence underestimates the amount of internal loss. If the empirical threshold current density is reduced by 25% and the empirical gain coefficient is increased by 10%, the predicted internal loss

values for Channel 2 and 6 increase to 31 and 35 cm^{-1}. These values are in good agreement with the values predicted from the differential efficiency data (31 and 36 cm^{-1}). Such changes to the material gain empirical fit parameters are consistent with the improvements expected from the use of compressively strained quantum wells and the average internal loss for these VCSELs can be stated as approximately 34 cm^{-1}.

6.5.1 Analysis Discussion

The analysis used treats the average internal loss value as an aggregate of all the optical loss sources in the device. These optical loss sources include scattering and absorption losses associated with various regions of the VCSEL. These regions include; the active region, the fully-oxidized DBRs, and the abrupt air-gap aperture.

The active region design in this work made use of 1.22-Q InGaAsP superlattice layers on both sides of the VCSEL active region. These layers, like the barriers around the quantum wells, absorb the 980-nm pump light. The difference is that the superlattice layers are clad on both sides by InP layers. These InP layers will block the diffusion of the optically generated carriers from the superlattice layers to the quantum wells. Hence, carriers will accumulate in the superlattice layers. These free-carriers can cause absorb the lasing light and lead to increased loss in the VCSEL structure. Fortunately this effect is offset

by the placement of the superlattice layers near the optical nulls of the lasing standing wave electric field.

The DBRs are fabricated from AlO_x generated by fully oxidizing AlAs material. The loss of fully oxidized AlO_x near 1500 nm has been studied previously by others [11]. Reference 11 has found that AlO_x formed by wet thermal oxidation exhibits a loss of 2.46 cm^{-1} at 1500 nm. This value however, does not necessarily imply that the excess loss in our mirror structure will be limited to this value. In fact, the research in Reference 11 investigated layers oxidized from the surface and it is plausible that the lateral oxidation of AlAs layers will yield different material properties. The fact that VCSELs using mirrors centered with the oxidation front union point (see Section 4.1.3) did not function is an indicator that the properties of the oxidation layers are not yet fully understood. The net result is that the fully-oxidized DBRs can potentially contribute to the excess optical loss in the structure.

Abrupt apertures, such as the one used in this structure, are known to contribute to the optical loss of the structure and have been studied in detail by others [12]. The careful placement of the aperture near the optical null and careful control of the aperture thickness both minimize the impact of the aperture on the scattering loss associated with the aperture. Never-the-less, the aperture can be expected to contribute to excess optical loss in the structure.

For an un-doped optically-pumped structure, low values of average internal loss should be achievable. If the excess internal loss in the structure were reduced to 10 cm^{-1}, the performance of the VCSELs could be greatly improved. The differential efficiency of Channel 2 would be increased from 18% to about 40%. In addition, the threshold would be reduced from 0.56 mW to 0.14 mW. The increased efficiency would lead to a thermal rollover point at higher pump powers. The combined effects of the threshold improvement, the differential efficiency improvement, and the thermal rollover improvement would lead to an increase in the peak operating temperature and more than double the peak output power at all operating temperatures.

6.6 Results and Discussion

Three issues are of particular importance when analyzing the CDWM VCSEL array results: channel uniformity, wavelength control, and heat management. This section will discuss these issues in light of the previously presented device test results and analysis.

Channel uniformity refers to the uniformity of such parameters as threshold, differential efficiency, and peak output power across the different wavelength channels of the array. The data for this work was shown in Section 6.3. Uniformity is important to allow the same drive electronics to operate each

VCSEL in the array (either by controlling an integrated pump laser or by fabricating electrically pumped devices). The cost of these drive circuits is reduced if all devices have the operating characteristics. The uniformity of the present array is good considering the 140 nm wavelength span, but not sufficient for actual low-cost applications.

Several steps can be taken to improve the uniformity of the array. The most important is improving the VCSEL array active-region design. First, the nonplanar wafer bonding process should be used to integrate four active regions instead of only two. This will allow for more uniform gain-mode offset across the array and will improve the uniformity of the VCSEL thresholds and output powers over temperature. Next, slightly different composition barriers should be used in each active region to improve the carrier confinement in each active region and allow all the channels to operate to higher temperatures. The total pump absorption efficiency is quite sufficient in the present design, so the new design can be made such that the absorber length and composition are balanced to allow for the same pump power absorption in each active region.

Once the integrated active-region design is improved, the mirror processing can be improved to flatten the mirror reflectivity available for each VCSEL in the array (different anti-reflection coating thicknesses in different areas). This step will improve the uniformity of the differential efficiency of the VCSELs in the array. Additionally, some of the observed test variability could

be due to an imperfect backside substrate polish, and improving this polish can be expected to further improve the VCSEL output uniformity.

Wavelength control is another area of critical importance in CWDM VCSEL arrays. At first glance, Figure 6.16 shows that at 20 °C all the VCSELs in the array are about 5-10 nm short of their wavelength targets. Because most low-cost CWDM applications require un-cooled operation from 0 to 70 °C, the array results presented here are actually about 7 to 12 nm short of the channel-band center (about 1 nm of wavelength shift for every 10 °C of temperature change). The ITU CWDM specifications allow the wavelength of a channel to be about +/- 6-7 nm off the target. Thus, accounting for the 0 to 70 °C range of operation, the VCSEL channels can be -6 to -1 nm off the target (assuming about 7 nm of wavelength shift over temperature) at 0 °C or -4 to 1 nm off the target at 20 °C. Shifting all the wavelength of the entire VCSEL array fabricated in this work by 6 nm would bring the array within the CWDM specifications.

The wavelength selection technique presented in this work is sufficient to achieve the required wavelength control. However, the fine-pitch superlattice presented in Chapter 4 should be modified from the current thickness to allow for 5 nm wavelength corrections. In addition, a non-destructive technique for thickness characterization should be utilized to allow for the entire active-region

wafer to be analyzed thereby improving the processed array yield. This technique has not been developed as part of this work. Though progress can be made in this area, the present work represents a significant step forward in this area by allowing the material thicknesses to be adjusted after growth.

The final area of discussion inspired by the results presented in this chapter is in the area of thermal management. The comparison presented earlier between the VCSELs of this work and of other approaches has shown that these devices have a thermal impedance 160 to 300 % higher than other long-wavelength VCSELs. At first inspection, this seems to represent a significant and perhaps catastrophic disadvantage. For example, if these devices were to be electrically pumped they might be expected to operate near 2 volts with 15 mA of current. At such an operation point the VCSEL may have to dissipate as much as 30 mW of power and hence could be expected to self heat by about 115 °C. Such a device would likely not operate at room temperature and is not practical for real applications.

Poor thermal conductivity of VCSEL DBRs is not a new problem and has been overcome before. Electrically-pumped 1.5-μm VCSELs using Sb-based DBR mirrors [13] have been demonstrated above 88 °C. This is despite the fact that the Sb materials have a low thermal conductivity of only 0.03 W/cm-°C. In the Sb DBR work, early VCSEL designs required heat extraction through the thermal insulating DBR, as do the VCSELs of this CWDM array,

and showed high thermal impedance values near 8 °C/mW. This value is twice as high as the values measured in the fully oxidized DBR work. Through careful design and the use of heat spreading layers and thick gold layers, the thermal impedance of the Sb-DBR devices was improved to 2 °C/mW and 88-°C CW operation was achieved. Such a dramatic improvement in heat extraction was the result of intelligent design and an understanding of the mirror limitations. Similar device improvements can be implemented with the fully-oxidized DBRs of this work and thermal impedance values comparable to AlGaAs-based DBR VCSELs should be possible. Such improvements will be discussed in more detail in the Chapter 7.

6.7 Summary

Test results from optically-pumped CWDM VCSEL arrays spanning a record 140 nm from 1470 nm to 1610 nm have been presented in this chapter. The VCSEL devices are based on the design and fabrication techniques presented in Chapters 2 though 5. In order to test the optically-pumped arrays, a specialized precision test system was designed and built. Using this system, the modal confinement characteristics of optically-pumped VCSELs were characterized and understood, device optical spectra and light output properties were

measured and analyzed, and the thermal impedance of the design was determined.

With the proper control of the index guide strength it was shown that it is possible to maintain adequate single-mode performance while attaining well-behaved VCSEL output properties. The CWDM VCSEL array exhibited single-mode output powers at 20 °C of about -3 dBm with +/- 1 dB of output power variation at an absorbed pump power of 7.5 mW. The SMSR was 36 dB, though this value decreased at higher VCSEL output powers. The threshold uniformity of the array was 0.75 +/- 0.38 mW at room temperature and all devices operated up to 65 °C. The differential efficiency of the array at 20 °C was 14.9 +/- 3.7 %. This value was below the expected value and requires further understanding.

The thermal impedance of the VCSEL design was measured using a wavelength shift technique and was found to be 3.85 °C/mW at 20 °C. This value is higher than other long-wavelength VCSEL designs due to the low thermal conductivity of AlO_x. Intelligent heat removal designs similar to those used in other VCSEL research should allow this value to be further reduced.

The next chapter will summarize the results of this thesis work and build upon them to recommend future improvements and identify additional technical areas where the developed technologies can make important contributions.

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Chapter 7

Summary and Future Work

This thesis work developed the first ever device intrinsic vertical and lateral heterogeneous integration technique and used the technique to develop the widest wavelength span WDM VCSEL array ever reported [1]. The integration technique, called nonplanar wafer bonding, was demonstrated to be an effective technique capable of integrating dissimilar lattice-matched structures adjacent to each other on a lattice-mismatched substrate. Nonplanar wafer bonding was demonstrated with about 50% integrated area coverage and bond area yield levels of about 80%. Material characterization and numerical modeling of the nonplanar wafer bonding process verified the ability of the technique to accomplish the integration without degrading the material quality.

The newly developed nonplanar wafer bonding technique was used to demonstrate the widest wavelength span ever reported from a long-wavelength

multi-wavelength VCSEL array. The record wavelength span of 140 nm, extending from 1470 to 1610 nm, was made possible with nonplanar wafer bonding to integrate multiple active regions with different wavelength gain peaks on the wafer surface.

To enhance the performance of the optically-pumped VCSEL array, a novel active-region design was developed to improve the uniformity of carrier filling in the quantum wells when long pump-absorber layers are used. The new design was shown to reduce the lasing threshold by 50% while improving the peak operating temperature by 20 °C. With the new design, uniform carrier filling of the quantum wells could be achieved while simultaneously achieving over 80% single-pass pump power absorption.

To enable the wide wavelength span VCSEL arrays to be fabricated, fully oxidized mirrors were developed for use at long wavelengths and were adapted for use in optically-pumped VCSELs. These mirrors achieved stop-band widths near 1200 nm and 99% mirror reflectivities with only four mirror periods. The novel VCSEL structure also made use of air-gap annuli located at the wafer-bonded interface to provide modal confinement. The effect of these structures on single-mode performance and on laser output stability was investigated.

The final VCSEL arrays fabricated used two active regions integrated by the nonplanar wafer bonding technique using a nonplanar pressure block. The

top and bottom mirrors were fully-oxidized DBRs and air-gap annuli of different depths providing various amounts modal confinement were integrated on each wavelength region of the array. The array had eight different wavelength channels in a two-dimensional configuration on the wafer surface. Each die size was 1.25 mm by 1 mm. The VCSELs in the array were designed to span 140 nm from 1470 to 1610 nm in 20-nm steps. The VCSELs were also designed to be optically pumped with a 980 nm external pump laser through the polished backside of the wafer.

To facilitate reproducible testing of the optically-pumped VCSEL structures, a precision automated test system was developed. With this system, the VCSEL/pump laser alignment could be maintained for extended periods of time and only minor adjustments were required during measurement temperature changes. The system facilitated the collection of large amounts of data from all wavelength channels in the array at multiple temperatures and pump powers. Automated software routines were written to aid in the analysis of the collected data.

The 8-channel multiple-wavelength VCSEL array operated in a single transverse and longitudinal mode with as much as 45-dB SMSR and spanned a record wavelength range from 1470 nm to 1610 nm. The output power uniformity at a constant absorbed pump power of 14 mW was -2.7 dBm +/- 1 dB at 20 °C. All channels operated up to at least 65 °C with some channels

operating as high as 90 °C. The relative wavelength spacing of the channels of the array were precisely maintained at 20 nm, though the absolute wavelengths required a 6-nm red shift to fall within the CWDM system specifications.

The lateral integration technique developed, and the VCSEL arrays fabricated, represent novel technologies and are the first of their kind. Having been used to fabricate high-performance VCSELs, the nonplanar wafer bonding integration technique has been shown to be an effective lateral heterogeneous integration technology. The VCSEL arrays fabricated represent a significant step in the development of a single-chip source for low-cost CWDM communications networks. In addition, the fundamental integration approach used is capable of even wider wavelength arrays, spanning hundreds of nanometers on a single chip.

Inherent in integration approaches are limitations imposed by the integration technique itself. In this work the integration process influenced the selection of the InGaAsP material system for increased selectivity in wet-chemical etching of the active regions. The integration process also required the use of broad band mirrors such as the fully-oxidized mirrors used in this work. These decisions have an influence on the performance of the overall integrated chip as has been discussed in Sections 6.5 and 6.6. In chip-level integration, each VCSEL wavelength could be made using a separate active region wafer and DBR mirrors optimized for each wavelength. The individual chips could be

expected to have improved thermal performance because higher thermal conductivity mirrors could be used and a better thermal performing active region material system such as AlInGaAs could be used. With a separate active region for each wavelength, the gain-mode alignment could also be maintained for each wavelength channel. Some type of superlattice would still be needed to compensate for growth error, but this superlattice need not be as thick as was used in this work. In exchange for this improved performance, one would have the problem of trying to control the wavelengths during the fabrication of eight different structures. In addition, once the chips were fabricated, they would need to be singulated and precisely aligned and mounted together onto a common substrate. This singulation and mounting process does allow for the removal of bad devices, but also introduces more handling and potential yield loss steps. With an improved VCSEL design, as will be discussed in the next section, many of the limitations of the presently integrated devices can be overcome and the impact of the heterogeneous integration approach on the array performance can be minimized.

The work of thesis has been motivated by expanding the capabilities of heterogeneous integration and hence, a wafer-scale integration approach was selected. In real commercial applications the proper balance between performance and cost must be maintained in order to achieve success. Such factors affect the amount and type of integration selected. Integration

approaches, be they chip-scale of wafer-scale, have an impact on such factors as yield, production time, production volume, and performance. In some cases for example, lateral heterogeneous integration may not be able to compete with a well-developed chip-scale assembly and alignment capability. In other cases wafer-scale heterogeneous integration may be the only way to reach a performance objective. It is only by exploring the capabilities of each approach that such a final determination can be made. Regardless, the development of lateral heterogeneous integration is an important capability in the ongoing development of higher complexity and higher performance optoelectronics systems.

7.1 Future Work

Based on the results of this thesis work, several areas of future improvements have been identified. These areas include improvements to the nonplanar wafer bonding integration technique, demonstration of electronic and photonic integration using nonplanar wafer bonding, and improvements to the CWDM VCSEL design.

7.1.1 Nonplanar Wafer Bonding For Photonic ICs

Nonplanar wafer bonding can be improved to reduce the amount of wasted space on the chip and allow for section-to-section in-plane optical coupling. By

allowing laterally integrated sections to be optically coupled to each other, nonplanar wafer bonding can be used to develop photonic ICs (PICs). The ability of nonplanar wafer bonding to integrate arbitrary dissimilar structures adjacent to each other on the wafer surface could allow separately optimized semiconductor optical amplifier regions, laser regions, and modulator regions to be coupled to each other on the same chip. Present integration techniques require repeated regrowth steps or compromises in the device design in order to integrate these functionalities on the same chip. If nonplanar wafer bonding were to allow these regions to be laterally integrated and optically coupled, ideal optimized structures could be used for each function of the PIC.

Key improvements need to be made to allow nonplanar wafer bonding to be used in complex PICs. The most important improvement is to reduce the size of the bending accommodation region. One way to accomplish this may be to develop a thin-film bonding technique. With such a technique, the bending region could be reduced to just a few microns (from hundreds) because only the thin epitaxial layers would need to conform to the transfer substrate. The etched-back bending regions could then be filled with regrown material or bridged by an out-of-plane waveguide layer (3-D coupling) [2].

7.1.2 Nonplanar Wafer Bonding For Electronic and Photonic Integration

The nonplanar wafer bonding techniques developed in this thesis work are well suited for use in the integration of electronic and photonic components. An area for future work is the integration of on-chip drive circuits with high-speed and high-performance optical modulators. These devices can operate in excess of 40 Ghz and can benefit from the on-chip integration of GaAs of InP-based drive electronics directly adjacent to the optical modulator. Such integration is well within the scope of the lateral heterogeneous integration technique developed here and can have a large impact on the cost and performance of these components. Figure 7.1 shows one potential integration scheme. Drive and bias electronics can be integrated with both vertical and in-plane optical devices, forming complex single-chip transceivers.

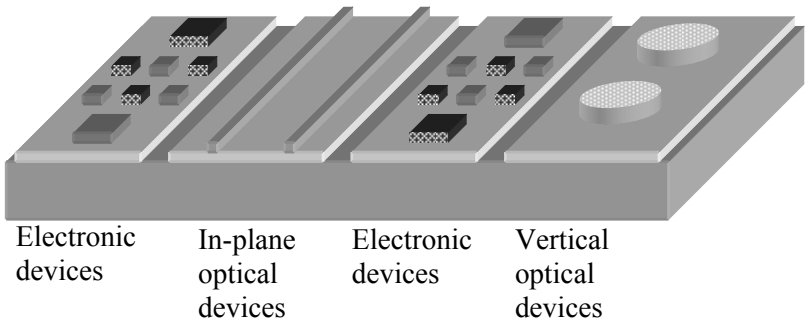

Figure 7.1. Schematic showing electronic and optical devices integrated by nonplanar wafer bonding. Electrical interconnects are not shown.

7.1.3 CWDM VCSEL Array Improvements

The CWDM VCSELs developed in this thesis work lay a foundation for the development of arrays suitable for use in commercial systems. In order for this progression to be made, further improvements in design and performance are necessary. Several of these improvements, including wavelength control and uniformity were already discussed in detail in Section 6.6. An important improvement required is the transition to an electrically-pumped VCSEL design and the required improvements in heat management required (see Section 6.6). Also important is the understanding and elimination of the large internal loss present in the completed VCSEL arrays as analyzed in section 6.5.

As discussed in Section 6.5.1, the 31 cm^{-1} internal loss value extracted for the optically pumped VCSELs of this work is significantly higher than what is expected for an un-doped, optically-pumped VCSEL. Section 6.5.1 predicts that there are two potential causes for this high loss, the fully-oxidized DBRs and free-carrier absorption from optically-generated carriers trapped in the superlattice layers of the VCSEL. Section 6.5.1 also discusses the large performance benefits that can be expected from improving this internal loss value. Future work should be conducted to isolate the cause of the problem and engineer around it. If the loss is in the mirrors, it is possible that the oxidation process can be investigated and developed to eliminate excess absorption and scatter. If the loss is in the superlattice, the composition of the layers can be

changed to prevent strong absorption of the pump and the buildup of carriers in this region. Also, the layer thicknesses can be adjusted to allow carriers to more easily tunnel out of the superlattice layers.

In order for the CWDM VCSEL arrays of this work to find use in commercial applications, it is likely they will need to be electrically-pumped devices. Extensive work has been done in recent years on electrically-pumped long-wavelength VCSELs and much of this work can be directly applied the fabrication platform developed here. The double wafer-bonded tunnel-junction VCSELs in Reference 3 use the same process flow as the VCSELs of this work.

Figure 7.2 shows a schematic picture of the proposed electrically-pumped CWDM VCSEL array with two different active regions used. As in the optically-pumped arrays of this work, each of the active regions can be used to support multiple wavelengths using superlattice etching. The process to fabricate the arrays can closely follow that used to fabricate the single wavelength arrays in Reference 3. In this reference, the active region wafer is regrown with a tunnel junction. After this tunnel junction is regrown, it is patterned and etched away, leaving circular tunnel junction regions on the wafer surface. By leaving the tunnel junction for current injection only in selected areas, each of these circles will define a VCSEL current and index aperture in the completed device. After etching the tunnel junction, an n-doped contact and current spreading layer is grown over the entire surface. In the referenced work,

the active region is then double wafer bonded and intra-cavity contacted. This same approach to VCSEL formation could be used for CWDM arrays by nonplanar wafer bonding. The modification is that the active region wafer should be step-etched prior to the growth of the tunnel junction. Then the VCSELs can be fabricated in the same way as described in Chapter 5.

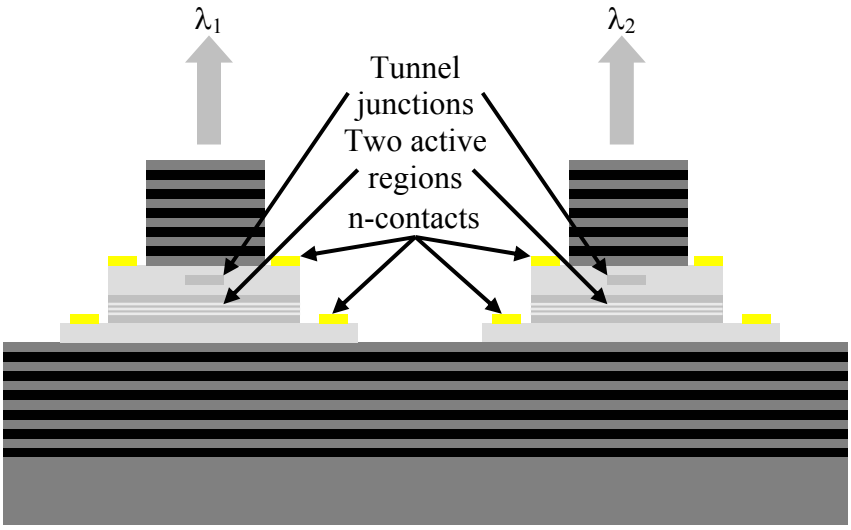

Figure 7.2. Schematic of two electrically pumped VCSELs with different active regions integrated by nonplanar wafer bonding.

As was pointed out in Section 6.5, the thermal impedance of the present double oxide-DBR VCSEL configuration is not well suited for electrical pumping because the excess heat generated is difficult to extract through the fully oxidized DBRs due to their low thermal conductivity.

Fortunately, the thermal conductivity problem has already been solved by others working on tunnel junction long-wavelength VCSELs with thermally

insulating DBRs. As was discussed in Section 6.5, Reference 4 has developed techniques to extract heat form a VSCEL structure with a thermal impedance even higher that those of this work. The techniques include heat spreading layers and thick gold for improved heat extraction from the active region. Combined with flip-chip mounting, such techniques could drastically improve the thermal impedance of electrically pumped VCSELs with fully oxidized DBRs. Figure 7.3 shows a potential flip-chip configuration for bottom-emitting electrically pumped VCSELs that could be applied to this work. The thick gold contact layers help remove heat from the structure and transfer it to the heat sink and signal routing board (aluminum nitride or similar)

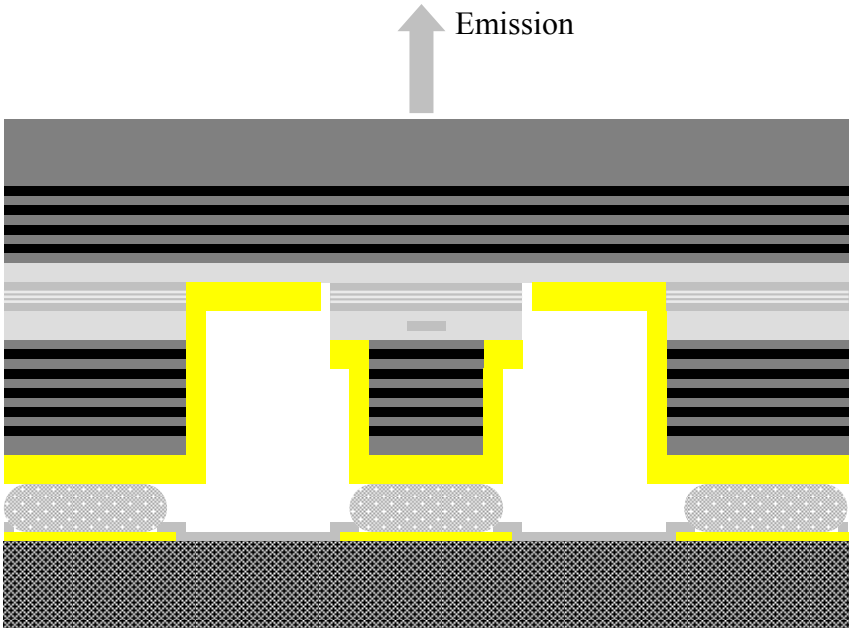

Figure 7.3. Schematic of a bottom-emitting, electrically-pumped VCSEL flip-chip mounted for improved thermal management.

Thus, with a comprehensive and intelligent VCSEL design it will be possible to fabricate electrically pumped CWDM VCSEL arrays that meet the performance requirements of commercial applications. The core technological innovations developed in this thesis can also be used to extend the operating span of the CWDM array to several hundred nanometers, allowing a single VCSEL array to span from 1310 nm to 1610 nm.

References

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Appendix A

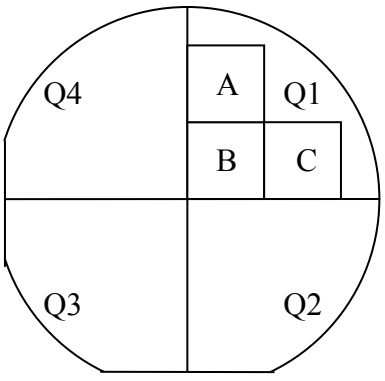
Process Follower for WDM VCSEL Array with Traditional DBRs and Backside Processed Nonplanar Wafer Bonding

Nonplanar (backside processed) VCSEL Process – Traditional DBRs

InP wafer growth number: UCSB S020415B
Piece number: Q3B
Back mirror growth number: Gore 010620H
Piece number: Q4B
Front mirror growth number: Gore 010621A
Piece number: Q4B
1.0 Cleave and clean sample

1.1 Cleave a 1 cm^2 sample from the InP wafer

1.2 Record the piece number



1.3 Cleave a 1 cm^2 piece from the back mirror wafer

1.4 Record the piece number

1.5 Cleave a 1 cm^2 piece from the front mirror wafer

1.6 Record the piece number

1.7 Mark back of front mirror for later substrate removal

1.8 Measure reflectivity of back mirror piece (file name):_PR018-bm.sp_

1.9 Measure reflectivity of front mirror piece (file name):_PR018-fm.sp_

1.10 Measure PL on active region (file name):_skipped_

1.11 Clean samples with DI, Acetone, and IPA

2.0 Etch uniform index guide on front mirror and dummy GaAs sample

2.1 Pattern circles Layer 1
- 2.1.1 Spin 4110
  - 2.1.1.1 5K, 45sec, 90sec bake @ 95ºC
- 2.1.2 Edge bead removal
  - 2.1.2.1 Wait 5 minutes
  - 2.1.2.2 Expose edge bead 60 seconds
  - 2.1.2.3 Develop 60 seconds
- 2.1.3 Pattern Mask: ***Optically Pumped Mask 1***, Layer: Pattern 1
  - 2.1.3.1 Use vacuum contact
  - 2.1.3.2 Expose 10sec develop 45sec

2.2 Etch circles Layer 1
- 2.2.1 O_2 descum (300 mTorr, 100W, 15sec) – provides wetting surface
- 2.2.2 Calibrate etch rate for 350A - 29 sec H_3PO_4:H_2O_2:H_20 2:1:60 (~730A/min) on dummy sample
  - 2.2.2.1 Strip PR with Acetone and IPA
  - 2.2.2.2 Dektak to determine trench depth:_300-325 Angstrom_
  - 2.2.2.3 Rate: _11.2 A/sec_

2.2.3 Etch 350A - _30_ sec H_3PO_4:H_2O_2:H_20 2:1:60
2.2.3.1 Use wet transfer
2.2.4 DI rinse
2.2.5 Strip PR with Acetone and IPA
2.2.6 Dektak to determine trench depth:_325 A_

2.3 Pattern circles Layer 2
2.3.1 Spin 4110
2.3.1.1 5K, 45sec, 90sec bake @ 95ºC
2.3.2 Edge bead removal
2.3.2.1 Wait 5 minutes
2.3.2.2 Expose edge bead 60 seconds
2.3.2.3 Develop 60 seconds
2.3.3 Pattern Mask: ***Optically Pumped Mask 1***, Layer: Pattern 2
2.3.3.1 Use vacuum contact
2.3.3.2 Expose 10sec, do **NOT** develop

2.4 Pattern circles Layer 3
2.4.1 Pattern Mask: ***Optically Pumped Mask 1***, Layer: Pattern 3
2.4.1.1 Use vacuum contact
2.4.1.2 Expose 10sec, do **NOT** develop

2.5 Pattern circles Layer 4
2.5.1 Pattern Mask: ***Optically Pumped Mask 1***, Layer: Pattern 4
2.5.1.1 Use vacuum contact
2.5.1.2 Expose 10sec develop 45sec

2.6 Etch Pattern Layers 2, 3, & 4
2.6.2 Etch 350A - _30_ sec H_3PO_4:H_2O_2:H_20 2:1:60 (~730A/min)
2.6.2.1 Use wet transfer
2.6.3 DI rinse
2.6.4 Strip PR with Acetone and IPA
2.6.5 Dektak to determine depth:_300 A_

3.0 Defect removal step on back mirror

3.1 Tergitol Clean samples

3.2 Inspect and map defect locations

3.3 Spin 4110
- 3.2.1 5K, 45sec, 90sec bake @ 95ºC

3.4 Expose defects with height on microscope (150x)
- 3.4.1 Use microscope Iris to reduce aperture size
- 3.4.2 Expose 5sec develop 60sec

3.5 Etch for 9 minutes in H_3PO_4:H_2O_2:H_20 1:1:10

3.6 Inspect

3.7 Strip PR with Acetone and IPA

4.0 Defect removal step on front mirror

4.1 Inspect and map defect locations

4.2 Spin 4110
- 4.2.1 5K, 45sec, 90sec bake @ 95ºC

4.3 Expose defects with height on microscope (150x)
- 4.3.1 Use microscope Iris to reduce aperture size
- 4.3.2 Expose 5sec develop 60sec

4.4 Etch for 6 minutes in H_3PO_4:H_2O_2:H_20 1:1:10

4.5 Inspect

4.6 Strip PR with Acetone and IPA

5.0 Pattern and etch step on epitaxial side of InP wafer

5.1 Pattern step
- 5.1.1 Spin 4330
  - 5.1.1.1 5K, 45sec, 90sec bake @ 95ºC
- 5.1.2 Edge bead removal
  - 5.1.2.1 Wait 5 minutes
  - 5.1.2.2 Expose edge bead 90 seconds
  - 5.1.2.3 Develop 90 seconds

5.1.3 Pattern Mask: ***Step Etch Evaluation (Mask1***) Layer: ***Step Etch 2***
- 5.1.3.1 Align corner of sample to the center of the cross alignment bracket on mask
- 5.1.3.2 Expose 18sec develop 90sec
- 5.1.3.3 Use microscope to expose undeveloped patches
  - 5.1.3.3.1 5sec exposure, 30sec develop

5.1.4 Tergitol spray clean

5.1.5 Bake @ 110°C for 60seconds

5.2 Etch step

5.2.1 Etch 30 sec in 3:1 H_3PO_4:HCl to remove top cladding
- 5.2.1.1 Use wet transfer

5.2.2 Gentle DI rinse

5.2.3 Etch for 12 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove MQW's
- 5.2.3.1 Use only 10 minutes for fresh etchant
- 5.2.3.2 Use wet transfer

5.2.4 Gentle DI rinse

5.2.5 Etch 30 sec in 3:1 H_3PO_4:HCl to remove bottom cladding
- 5.2.5.1 Use wet transfer

5.2.6 Gentle DI rinse

5.2.7 Etch for 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs S.L. layer
- 5.2.7.1 Use wet transfer

5.2.8 Gentle DI rinse

5.2.9 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP S.L. layer
- 5.2.9.1 Use wet transfer

5.2.10 Gentle DI rinse

5.2.11 Repeat 3 more times from 5.2.7 (4 S.L. periods in total)

5.2.12 Etch for 25 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs stop etch
- 5.2.12.1 Use wet transfer

5.2.13 Gentle DI rinse and dry

5.2.14 3K spin strip PR with Acetone and IPA

6.0 Profile Sample

6.1 Take complete Dektak Profile of step etched surface

6.1.1 Average Step:_1.23 μm_

6.2 Measure PL across sample
- 6.2.1 Use PL mapper and take a 2-D wafer map
  - 6.2.1.1 6mm x 6mm with 250μm spacing

7.0 Mount sample epitaxy side down with InP sample pieces for lapping

7.1 Tergitol spray clean

7.2 Coat front of sample with 1 spin SF11
- 7.2.1 Bake at 200°C, 60sec

7.3 Vacuum mount with 4 more 1 cm^2 pieces to the lapping block, epitaxial (PMGI) side down
- 7.3.1 Use MWH135 wax on hot plate set to 180°C
- 7.3.2 Clean with Acetone and IPA

8.0 Lap and remount for polishing

8.1 Lap on 9um diamond grit lapping paper to about 150μm thick

8.2 Clean sample thoroughly with acetone and IPA

8.3 Demount on hot plate set to 160°C
- 8.3.1 Do not clean wax off sample and dummies

8.4 Vacuum mount pieces to glass cover slips using additional MWH135 wax
- 8.4.1 Use a 160°C hot plate temperature

8.5 3K spin clean with Acetone and IPA

8.6 Vacuum mount sample and dummy pieces to glass polishing puck
- 8.6.1 Place real sample in center
- 8.6.2 Use MWM070 on a 130°C hot plate

8.7 Clean excess MWM070 wax
- 8.7.1 Use WaxStrip (20g) mixed with DI (200ml) heated in the ultrasound (45°C, setting 5) for 10 minutes
- 8.7.2 Swab with a foam swap and ultrasonically clean for 2 more minutes
- 8.7.3 Rinse thoroughly with DI

9.0 Polish InP

9.1 Measure wafer thickness: _151_μm

9.2 Polish with 1% Br:Meth to 100μm (assume 20μm/min), time:_2:30_min:sec

9.3 Polish for 15seconds with 0.1% Br:Meth and Methanol rinse

9.4 Demount glass cover slips from polishing puck on a 110°C hotplate

9.5 Clean sample, two dummies, and polishing puck

- 9.5.1 Use WaxStrip (20g) mixed with DI (200ml) heated in the ultrasound (45°C, setting 5) for 5 minutes
- 9.5.2 Swab with a foam swap and ultrasonically clean for 2 more minutes
- 9.5.3 Rinse thoroughly with DI and dry

9.6 Finish Etch

- 9.6.1 Etch sample and dummy for 2 minutes in 0.1% Br:Meth

10.0 Pattern and etch deformation on polished side of wafer

10.1 Pattern deformation step (**repeat on dummy samples**)

- 10.1.1 Spin 4330
  - 10.1.1.1 5K, 45sec, 90sec bake @ 95ºC
- 10.1.2 Edge bead removal
  - 10.1.2.1 Wait 5 minutes
  - 10.1.2.2 Expose edge bead 90 seconds
  - 10.1.2.3 Develop 90 seconds
- 10.1.3 Pattern Mask: ***Step Etch Evaluation (Mask1***) Layer: ***Deform 2***
  - **10.1.3.1 <u>Use IR aligner</u>**
  - 10.1.3.2 Expose 18 sec develop 90sec
  - 10.1.3.3 Tergitol spray clean
  - 10.1.3.4 Hard Bake 110°C 60sec

10.2 Etch deformation step on dummy sample

- 10.2.1 Etch in 3:1 H_3PO_4:HCl
  - 10.2.1.1 Etch in ultrasound (25°C, setting 5)
  - 10.2.1.2 Hold horizontal

10.2.1.3 Assume 1.62 um/min etch rate and use the average step height number
10.2.1.3.1 Etch time: 45 sec
10.2.2 DI rinse and dry
10.2.3 Strip PR with Acetone and IPA
10.2.4 Dektak Etch:_1.11_
10.2.5 Determine rate:_0.02333 μm/sec___
10.2.6 Repeat with second dummy if rate is suspect

10.3 Etch deformation step
10.3.1 Etch in 3:1 H_3PO_4:HCl (same mixture as before)
10.3.1.1 Etch in ultrasound (25°C, setting 5)
10.3.1.2 Hold horizontal
10.3.1.3 Assume _0.02444_ μm/sec etch-rate and use average step height number
10.3.1.3.1 Etch time:_50 sec_
10.3.2 DI rinse and dry
10.3.3 3K spin strip PR with Acetone and IPA
10.3.4 Dektak Etch:_1.57 μm__
10.3.5 Determine rate:_0.0315 μm/sec_
10.3.6 Repair step height by opening previously exposed areas and etching to lower by: _1.57-1.23=0.34 -> 11 second etch__

11.0 Profile Sample
11.1 Take complete Dektak Profile of step etched surface
11.1.1 Average Step:_1.22 μm_

12.0 Demount sample

12.1 Tergitol spay clean

12.2 Soak in clean acetone overnight to separate from glass cover slip
12.2.1 Rinse in clean acetone, IPA and dry

12.3 Clean sample in hot 1165 stripper

12.4 Acetone clean and IPA rinse and dry

12.5 Keep sample clean and bond immediately

13.0 Bond InP epitaxial side to GaAs Back Mirror

13.1 Clean samples
- 13.1.1 Rinse with Acetone and IPA (GaAs only)
- 13.1.2 Swab with tergitol and spray with Tergitol (GaAs only)
- 13.1.3 DI rinse and dry (GaAs only)
- 13.1.4 O_2 descum (300 mTorr, 100W, 15sec) (both samples)
- 13.1.5 Dip in BOE for 5seconds for InP and GaAs (use basket)
- 13.1.6 DI rinse and dry

13.2 Bond Samples
- 13.2.1 Dip in NH_4OH for 1 minute
- 13.2.2 Wet transfer to Methanol
- 13.2.3 Wet transfer to wipe
- 13.2.4 Abut samples and flip InP onto GaAs
- 13.2.5 Place samples together on to graphite block
- 13.2.6 Tighten screws and rewet with Methanol
  - 13.2.6.1 Use 0.30 on torque wrench
- 13.2.7 Bond in furnace
  - 13.2.7.1 Use 85°C/min to 630°C for 30min
  - 13.2.7.2 –10°C/min to 300°C
  - 13.2.7.3 Step down to 25°C
- 13.2.8 Remove from fixture when below 100ºC

13.3 Remove InP substrate
- 13.3.1 Rinse with Acetone and IPA
- 13.3.2 Etch in 2.5:1 HCl:H_2O for about 15min
- 13.3.3 Rinse thoroughly in water and IPA and dry

13.4 Remove non-bonded areas – only if large un-bonded areas exist
- 13.4.1 Spin SF15 and bake on 200°C hot plate
- 13.4.2 Strip PMGI with heated 1165
- 13.4.3 Acetone and IPA rinse
- 13.4.4 Repeat if necessary

13.5 Etch stop etch
- 13.5.1 1min in 1:1:10 H_2SO_4:H_2O_2:H_2O for .2μm (15 sec overetch)
- 13.5.2 Rinse thoroughly in water and IPA and dry

14.0 Pattern and Etch deformation areas and excess epitaxy

14.1 Pattern etch back step
- 14.1.1 2 spins 4110
  - 14.1.1.1 5K, 45sec, (90sec bake @ 95ºC between and after)
- 14.1.2 Edge bead removal
  - 14.1.2.1 Wait 5 minutes
  - 14.1.2.2 Expose edge bead 90 seconds
  - 14.1.2.3 Develop 90 seconds
- 14.1.3 Pattern Mask: ***Nonplanar Wafer Bond Mask Rev. 2***
  Layer: ***Etch Back 2***
  - 14.1.3.1 Use IR aligner
  - 14.1.3.2 Expose 20 sec develop 45sec

14.2 Etch back
- 14.2.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP S.L. layer
  - 14.2.1.1 Use wet transfer
- 14.2.2 Gentle DI rinse
- 14.2.3 Etch for 25 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs S.L. layer
  - 14.2.3.1 Use wet transfer
- 14.2.4 Gentle DI rinse
- 14.2.5 Repeat 3 more times from 14.2.1 (4 S.L. periods in total)
- 14.2.6 Etch 30 sec in 3:1 H_3PO_4:HCl to remove top InP cladding
  - 14.2.6.1 Use wet transfer
- 14.2.7 Gentle DI rinse
- 14.2.8 Etch 12 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove MQW's
  - 14.2.8.1 Use 10 minutes for fresh etchant
  - 14.2.8.2 Use wet transfer
- 14.2.9 Gentle DI rinse
- 14.2.10 Etch 30 sec in 3:1 H_3PO_4:HCl to remove bottom cladding
  - 14.2.10.1 Use wet transfer
- 14.2.11 Gentle DI rinse
- 14.2.12 Etch for 25 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs stop etch
  - 14.2.12.1 Use wet transfer
- 14.2.13 Gentle DI rinse
- 14.2.14 Strip PR with Acetone and IPA

15.0 Universal superlattice adjust (only if necessary) (remove ½ periods)

15.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP S.L. layer
15.1.1 Use wet transfer

15.2 Gentle DI rinse

~~15.3 Etch for 25 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs S.L. layer~~
~~15.3.1 Use wet transfer~~

~~15.4 Gentle DI rinse~~

15.5 ~~Repeat from 15.1 for each full period needing removal~~

15.6 Strip PR with Acetone and IPA

16.0 Dektak sample
16.1 Locate defects

17.0 Spot remove defects

17.1 Inspect and map defect locations

17.2 Spin 4330
17.2.1 5K, 45sec, 90sec bake @ 95ºC
17.2.2 Repeat (two coats necessary)

17.3 Expose defects with height on microscope (150x)
17.3.1 Exposure 5sec develop 60sec

17.4 Etch using 3:1 H_3PO_4:HCl and 1:1:10 H_2SO_4:H_2O_2:H_2O

17.5 Inspect

17.6 Strip PR with Acetone and IPA

18.0 Etch WDM superlattice adjustment etches

18.1 The etchant used will depend on how many ½ periods were removed in step 15.0. If an even number (InP surface), then begin with 3:1 H_3PO_4:HCl, or else begin with 1:1:10 H_2SO_4:H_2O_2:H_2O

18.2 Pattern with first mask layer
- 18.2.1 3 Spins 4110
  - 18.2.1.1 5K, 45sec, 90sec (bake @ 95ºC before and after)
- 18.2.2 Edge bead removal
  - 18.2.2.1 Wait 5 minutes
  - 18.2.2.2 Expose edge bead 90 seconds
  - 18.2.2.3 Develop 2 minutes
- 18.2.3 Pattern Mask: ***Nonplanar Wafer Bond Mask Rev. 2***
  Layer: ***Step Etch 2***
  - 18.2.3.1 Align with alignment marks in gap between bonded material from first bond
  - 18.2.3.2 Expose 20sec develop 90sec
  - 18.2.3.3 Use microscope to expose undeveloped patches
    - 18.2.3.3.1 5sec exposure, 30sec develop
- 18.2.4 Tergitol clean
- 18.2.5 Hard bake 110 °C, 60sec

~~18.3 Etch step 1 (Even number of half periods removed – InP on top)~~
- ~~18.3.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP~~
- ~~18.3.2 Gentle DI rinse~~
- ~~18.3.3 Etch 25 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs~~
  - ~~18.3.3.1 Use wet transfer~~
- ~~18.3.4 Gentle DI rinse~~
- ~~18.3.5 Strip PR with Acetone and IPA~~

18.4 Etch step 1 (Odd number of half periods removed – InGaAs on top)
- 18.4.1 Etch 25 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs
- 18.4.2 Gentle DI rinse
- 18.4.3 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP
  - 18.4.3.1 Use wet transfer
- 18.4.4 Gentle DI rinse
- 18.4.5 Strip PR with Acetone and IPA

18.5 Pattern second step
- 18.5.1 Spin 4330

18.5.1.1 5K, 45sec, 90sec bake @ 95ºC
18.5.2 Edge bead removal
18.5.2.1 Wait 5 minutes
18.5.2.2 Expose edge bead 80 seconds
18.5.2.3 Develop 2 minutes
18.5.3 Pattern Mask: ***Nonplanar Wafer Bond Mask Rev. 2***
Layer: ***Step Etch 1***
18.5.3.1 Align crosshairs
18.5.3.2 Expose 18sec develop 90sec
18.5.3.3 Use microscope to expose undeveloped patches
18.5.3.3.1 5sec exposure, 30sec develop
18.5.3.4 Tergitol clean
18.5.3.5 Hard bake 110 °C, 60sec

~~18.6 Etch step 2 (Even number of half periods removed – InP on top)~~
~~18.6.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP~~
~~18.6.2 Gentle DI rinse~~
~~18.6.3 Strip PR with Acetone and IPA~~

18.7 Etch step 2 (Odd number of half periods removed – InGaAs on top)
18.7.1 Etch 25 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs
18.7.2 Gentle DI rinse
18.7.3 Strip PR with Acetone and IPA

19.0 Bond InP epitaxial layers to patterned front GaAs mirror

19.1 Clean samples
19.1.1 Rinse with Acetone and IPA
19.1.2 Swab with Tergitol and spray with Tergitol
19.1.3 DI rinse and dry
19.1.4 O_2 descum (300 mTorr, 100W, 15sec)
19.1.5 Dip both in BOE for 5 seconds
19.1.6 DI rinse and dry

19.2 Bond Samples
19.2.1 Dip in NH_4OH for 1 minute
19.2.2 Wet transfer to Methanol

19.2.3 Wet transfer to wipe
19.2.4 Abut samples and flip InP onto GaAs
19.2.4.1 ***USE 90° ROTATION! wr.t. Nonplanar bond***
19.2.5 Place samples together on to graphite block
19.2.6 Tighten screws and rewet with Methanol
19.2.6.1 Use 0.55 on torque wrench
19.2.7 Bond in furnace
19.2.7.1 Use 85°C/min to 600°C for 30min
19.2.7.2 –10°C/min to 300°C
19.2.7.3 Step down to 25°C
19.2.8 Remove from fixture when below 100ºC

20.0 Polish back mirror GaAs substrate (unmarked side)

20.1 Mount and lap
20.1.1 Lap about 25um with 9μm grit paper
20.1.2 Clean fixture and sample thoroughly
20.1.3 Lap about 25um with 3μm grit paper
20.1.4 Clean fixture and sample thoroughly
20.1.5 Wipe on red silk pad with Alumina powder and Bleach mixture
20.1.6 Immediate water rinse
20.1.7 Repeat silk pad and rinse until cloudiness is gone

20.2 Tergitol spray clean

~~20.3 15 sec dip in hot 4:1:1 H_2SO_4:H_2O_2:H_2O (stir vigorously)~~

21.0 Remove front mirror GaAs substrate (marked side)

21.1 Lap to remove 200um
21.1.1 Use 9 or 12um grit

21.2 Wax mount to glass slide

21.3 Etch in stirring 30:1 Peroxide: Ammonium Hydroxide (150ml:5ml) – about 2 hours
21.3.1 Remove after sample turns pink or promptly when sample turns violet and green

21.4 Promptly etch stop etch
21.4.1 10sec in BOE

21.5 Cotton swab in Tergitol if necessary

21.6 Demount from glass slide

21.7 Remove non-bonded areas – only if large un-bonded areas exist
21.7.1 Spin SF15 and bake on 200°C hot plate
21.7.2 Strip PMGI with heated 1165
21.7.3 Acetone and IPA rinse
21.7.4 Tergitol clean
21.7.5 Repeat if necessary

22.0 Deposit pump targets

22.1 Spin SF11
22.1.1 5K, 45sec, 90sec bake @ 200ºC

22.2 Spin 4330
22.2.1 5K, 45sec, 90sec bake @ 95ºC

22.3 Edge bead removal
22.3.1 Wait 5 minutes
22.3.2 Expose edge bead 90 seconds
22.3.3 Develop 90 seconds
22.3.4 Pattern Mask: ***Optically pumped***
Layer: ***Pump Targets***
22.3.4.1 Use IR aligner
22.3.4.2 Expose 18sec develop 90sec
22.3.4.3 DUV expose 200 seconds
22.3.4.4 SAL101 develop 2 minutes

22.4 Evaporate Ti/Au 200/1000

22.5 Liftoff in heated 1165 stripper

22.6 Acetone and IPA rinse

APPENDIX A

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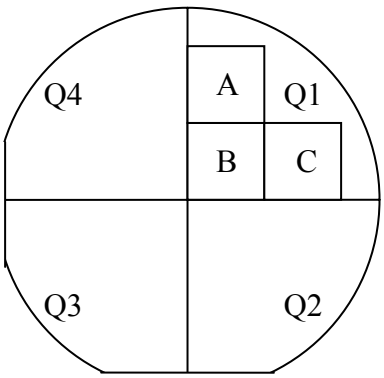
Appendix B

Process Follower for CWDM VCSEL Array with Fully Oxidized DBRs and Nonplanar Wafer Bonding With a Nonplanar Pressure Block

2-D WDM Fully Oxidized DBR Nonplanar Wafer Bonded

VCSEL Process (Nonplanar Pressure Block)

InP wafer growth number: TW 0306266-C
Piece number: Q4B (&A for NP Block)
Back mirror growth number: Gore B021101C-1
Piece number: Q1C
Front mirror growth number: Gore B021101E-1
Piece number: Q2B



1.0 Cleave and clean sample

1.1 Cleave a 1x2 cm sample from the InP wafer

1.1.1 Cleave sample to produce

perfectly parallel 2cm sides
1.1.2 Mark the side for later lapping with an 'X'

1.2 Record the piece number

1.3 Cleave a 9x10 mm piece from the back mirror wafer

1.4 Record the piece number

1.5 Cleave a 9x10 mm piece from the front mirror wafer

1.6 Record the piece number

1.7 Mark back of front mirror for later substrate removal

1.8 Measure reflectivity of back mirror piece

1.9 Measure reflectivity of front mirror piece

1.10 Fit mirror reflectivity spectrums and determine number of superlattice periods to remove for this process run (see bold type sections below)

1.11 Clean samples with DI, Acetone, and IPA

1.12 Tergitol spray clean samples

2.0 Etch index guide on front mirror

2.1 Pattern index guide 1 on sample and dummy piece
- 2.1.1 Spin 4110
  - 2.1.1.1 5K, 45sec, 90sec bake @ 95ºC
- 2.1.2 Edge bead removal
  - 2.1.2.1 Wait 5 minutes
  - 2.1.2.2 Expose edge bead 60 seconds
  - 2.1.2.3 Develop 60 seconds
- 2.1.3 Pattern Mask: ***Mask 4*** Layer: ***Index Pattern***
  - 2.1.3.1 Use vacuum contact
  - 2.1.3.2 Align index guides to the long side of the sample
  - 2.1.3.3 Expose 10sec develop 45sec

2.2 Etch index guide on dummy piece
- 2.2.1 Etch __60__sec H_3PO_4:H_2O_2:H_20 2:1:60 for __600Å___ depth
  - 2.2.1.1 Use wet transfer
- 2.2.2 DI rinse
- 2.2.3 Strip PR with Acetone and IPA
- 2.2.4 Dektak to determine trench depth:_700 A_rate: 11A/sec

2.3 Etch deepest index guide on sample
- 2.3.1 Etch _45_sec H_3PO_4:H_2O_2:H_20 2:1:60 for __500Å___ depth
  - 2.3.1.1 Use wet transfer
- 2.3.2 DI rinse
- 2.3.3 Strip PR with Acetone and IPA
- 2.3.4 Dektak to determine trench depth:_Not accurate_

2.4 Pattern index guide 2 on sample
- 2.4.1 Spin 4110
  - 2.4.1.1 5K, 45sec, 90sec bake @ 95ºC
- 2.4.2 Edge bead removal
  - 2.4.2.1 Wait 5 minutes
  - 2.4.2.2 Expose edge bead 60 seconds
  - 2.4.2.3 Develop 60 seconds
- 2.4.3 Pattern Mask: ***Mask 4*** Layer: ***Index Pattern***
  - 2.4.3.1 Align to etched square on sample, not cross
  - 2.4.3.2 Use vacuum contact
  - 2.4.3.3 Expose 10sec develop 45sec

2.5 Etch index guide on sample
- 2.5.1 Etch _40_sec H_3PO_4:H_2O_2:H_20 2:1:60 for __440Å ___ depth
  - 2.5.1.1 Use wet transfer
- 2.5.2 DI rinse
- 2.5.3 Strip PR with Acetone and IPA
- 2.5.4 Dektak to determine trench depth:_____

2.6 Pattern index guide 3 on sample
- 2.6.1 Spin 4110
  - 2.6.1.1 5K, 45sec, 90sec bake @ 95ºC
- 2.6.2 Edge bead removal
  - 2.6.2.1 Wait 5 minutes

2.6.2.2 Expose edge bead 60 seconds
2.6.2.3 Develop 60 seconds
2.6.3 Pattern Mask: ***Mask 4*** Layer: ***Index Pattern***
2.6.3.1 Use vacuum contact
2.6.3.2 Expose 10sec develop 45sec

2.7 Etch index guide on sample
2.7.1 Etch _35_sec H_3PO_4:H_2O_2:H_20 2:1:60 for __380Å ___ depth
2.7.1.1 Use wet transfer
2.7.2 DI rinse
2.7.3 Strip PR with Acetone and IPA
2.7.4 Dektak to determine trench depth:_____

2.8 Pattern index guide 4 on sample
2.8.1 Spin 4110
2.8.1.1 5K, 45sec, 90sec bake @ 95ºC
2.8.2 Edge bead removal
2.8.2.1 Wait 5 minutes
2.8.2.2 Expose edge bead 60 seconds
2.8.2.3 Develop 60 seconds
2.8.3 Pattern Mask: ***Mask 4*** Layer: ***Index Pattern***
2.8.3.1 Use vacuum contact
2.8.3.2 Expose 10sec develop 45sec

2.9 Etch index guide on sample
2.9.1 Etch _30_sec H_3PO_4:H_2O_2:H_20 2:1:60 for __320Å ___ depth
2.9.1.1 Use wet transfer
2.9.2 DI rinse
2.9.3 Strip PR with Acetone and IPA
2.9.4 Dektak to determine trench depth:_____

3.0 Defect removal step on back mirror

3.1 Inspect and map defect locations

3.2 Spin 4330
3.2.1 5K, 45sec, 90sec bake @ 95ºC

3.3 Expose defects with height on microscope (150x)

3.3.1 Exposure 8sec develop 60sec

3.4 Etch for 2 minutes in H_3PO_4:H_2O_2:H_20 1:1:10

3.5 Inspect

3.6 Strip PR with Acetone and IPA

4.0 Defect removal step on front mirror

4.1 Inspect and map defect locations

4.2 Spin 4330
4.2.1 5K, 45sec, 90sec bake @ 95ºC

4.3 Expose defects with height on microscope
4.3.1 Exposure 8sec develop 60sec

4.4 Etch for 80 seconds in H_3PO_4:H_2O_2:H_20 1:1:10

4.5 Inspect

4.6 Strip PR with Acetone and IPA

5.0 Etch Top AR adjustment layers

5.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

5.2 Etch 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer

~~**5.3 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer**~~

~~**5.4 Etch 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer**~~

5.5 DI rinse and N_2 blow dry

6.0 Pattern and etch step on epitaxial side of InP wafer

6.1 Clean masks

6.2 Pattern step

- 6.2.1 Spin 4330
  - 6.2.1.1 Apply ample PR to ensure uniform coverage
  - 6.2.1.2 5K, slow ramp, 45sec, 90sec bake @ 95ºC
- 6.2.2 Edge bead removal Mask: ***NP BOND MASK 3*** layer: ***EDGE BEAD***
  - 6.2.2.1 Wait 5 minutes
  - 6.2.2.2 Expose edge bead 90 seconds
  - 6.2.2.3 Develop 90 seconds
- 6.2.3 Pattern Mask: ***NP BOND MASK 1*** Layers: ***STEP ETCH & DEFORM ETCH***
  - 6.2.3.1 Place 1 cm^2 under the STEP ETCH pattern and the other 1 cm^2 under the DEFORM ETCH pattern. This approximately corresponds aligning one edge to the fourth alignment target from the edge.
  - 6.2.3.2 Align sample so there is a fat and a narrow bar on each side
  - 6.2.3.3 Expose 20sec develop 90sec
  - 6.2.3.4 Use microscope to expose undeveloped patches
    - 6.2.3.4.1 5sec exposure, 30sec develop
- 6.2.4 Tergitol spray clean
- 6.2.5 Bake @ 110°C for 60seconds
- 6.2.6 O_2 descum 100W/300mT for 1min, or until clean

7.0 Etch Step 1 – use wet transfer for all and DI rinse

~~**7.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer**~~

~~**7.2 Etch 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer**~~

7.3 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

7.4 Etch 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer

7.5 Etch 30 sec in 3:1 H_3PO_4:HCl to remove cladding

7.6 Etch for 3:30 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove first MQW

7.7 Etch 10 sec in 3:1 H_3PO_4:HCl to remove carrier blocking layer

7.8 Etch for 5:06 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove second MQW

7.9 Etch 10 sec in 3:1 H_3PO_4:HCl to remove carrier blocking layer

7.10 Etch for 9:52 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove third MQW

7.11 Etch 10 sec in 3:1 H_3PO_4:HCl to remove bottom cladding

7.12 Etch for 30 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs superlattice layer

7.13 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

7.14 Repeat steps 7.12and 7.13 two more times to remove a total of 3 superlattice periods

7.15 Etch for 10 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs etch stop layer

7.16 Etch bottom AR adjustment layers

7.16.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

7.16.2 Etch 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer

~~**7.16.3 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer**~~

~~**7.16.4 Etch 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer**~~

7.17 DI rinse and N_2 blow dry

7.18 Clean with Acetone and IPA

7.19 If necessary soak for 15 minutes in TRX @ 80°C and IPA rinse

7.19.1 Use a glass dish

8.0 Cleave sample

8.1 Cleave sample into 2 1cm^2 pieces
8.1.1 One piece is the bond piece, the other is the pressure block piece

9.0 Measure linear PL Map of InP piece to be bonded

10.0 Coat Pressure Block with SiNx

10.1 Tergitol spray clean

10.2 Deposit 1000Å at 250°C

11.0 Mount bond piece epitaxy side down for lapping

11.1 Tergitol spray clean sample for bonding

11.2 Coat front of sample with 1 spin SF11
11.2.1 Bake at 200°C, 60sec
11.2.2 Bake at 300°C, 3min

11.3 Vacuum mount to the lapping block, epitaxial (PMGI) side down
11.3.1 Use MWH135 wax on hot plate set to 180°C

12.0 Lap

12.1 Lap on 9um diamond grit lapping paper to 100μm thick

12.2 Clean sample thoroughly with acetone and IPA

12.3 Remove sample
12.3.1 Use 200°C hot plate and a wood stick

12.4 Clean sample in hot 1165 stripper

12.5 Acetone clean and IPA rinse and dry

12.6 Keep sample clean and bond immediately

13.0 Bond InP epitaxial side to GaAs piece

13.1 Prepare fixture and furnace
13.1.1 Lap fixture on 3um lapping paper about 10 passes

13.1.2 Program furnace

13.2 Clean samples
- 13.2.1 Rinse with Acetone and IPA (GaAs only)
- 13.2.2 Swab with tergitol and spray with Tergitol (GaAs only)
- 13.2.3 DI rinse and dry (GaAs only)
- 13.2.4 O_2 descum (300 mTorr, 100W, 15sec) (both samples)
- 13.2.5 Dip in BOE for 5seconds for InP and GaAs (use basket)
- 13.2.6 DI rinse and dry

13.3 Setup Fixture
- 13.3.1 Place Pressure Block Piece in fixture with epitaxial side up and the edge stripe opposite the pinching mechanism

13.4 Bond Samples
- 13.4.1 Dip in NH_4OH for 1 minute
- 13.4.2 Wet transfer to Methanol
- 13.4.3 Wet transfer to wipe
- 13.4.4 Abut samples and flip GaAs onto InP
  - 13.4.4.1 Keep track of which side of the InP has the edge strip
- 13.4.5 Place samples together on pressure block piece in fixture so edge stripes are on opposite sides
- 13.4.6 Apply finger tight pinching pressure
- 13.4.7 Apply dome and cover
- 13.4.8 Tighten screws
  - 13.4.8.1 Use 0.45 in-lb on torque wrench
- 13.4.9 Relieve pinching pressure
- 13.4.10 Bond in furnace
  - 13.4.10.1 Use 85°C/min to _600___°C for 30min
  - 13.4.10.2 –10°C/min to 300°C
  - 13.4.10.3 Step down to 25°C
- 13.4.11 Remove from fixture when below 100ºC

13.5 Remove InP substrate
- 13.5.1 Mount for lapping with InP side up
- 13.5.2 Lap to remove 25um
- 13.5.3 Demount
- 13.5.4 Clean with Acetone and IPA
- 13.5.5 Etch in 3:1 $HCl:H_2O$ for about 15min
- 13.5.6 Rinse thoroughly in water and IPA and dry

13.6 Remove non-bonded areas – only if large un-bonded areas exist
- 13.6.1 Spin SF15 and bake on 200°C hot plate
- 13.6.2 Strip PMGI with heated 1165
- 13.6.3 Acetone and IPA rinse
- 13.6.4 Repeat if necessary

13.7 Etch stop etch
- 13.7.1 50sec in 1:1:10 H_2SO_4:H_2O_2:H_2O for .2μm (over etch)
  - 13.7.1.1 Stir vigorously
- 13.7.2 Rinse thoroughly in water and IPA and dry

13.8 DI rinse and N_2 blow dry

14.0 Pattern and Etch deformation areas and excess epitaxy

14.1 Pattern etch back step
- 14.1.1 Spin 4330
  - 14.1.1.1 5K, slow ramp, 45sec, 90sec bake @ 95ºC
- 14.1.2 Edge bead removal
  - 14.1.2.1 Wait 5 minutes
  - 14.1.2.2 Expose edge bead 90 seconds
  - 14.1.2.3 Develop 90 seconds
- 14.1.3 Pattern Mask: ***NP Bond Mask 1***
  Layer: ***Etch Back***
  - 14.1.3.1 Expose 25 sec develop 90sec
  - 14.1.3.2 Use microscope to expose undeveloped patches
    - 14.1.3.2.1 5sec exposure, 30sec develop
- 14.1.4 Tergitol spray clean
- 14.1.5 Bake @ 110°C for 60seconds
- 14.1.6 O_2 descum 100W/300mT for 1min, or until clean

15.0 Etch back 1

15.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

15.2 Etch 30 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer

15.3 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

15.4 Etch 30 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer

15.5 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

15.6 Etch 30 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer

15.7 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP cladding

15.8 Etch for 7:10 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove third QW

15.9 Etch 10 sec in 3:1 H_3PO_4:HCl to remove carrier blocking layer

15.10 Etch for 4:50 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove second QW

15.11 Etch 10 sec in 3:1 H_3PO_4:HCl to remove carrier blocking layer

15.12 Etch for 3:20 min in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove first QW

15.13 Etch 30 sec in 3:1 H_3PO_4:HCl to remove InP cladding

15.14 Etch for 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs superlattice layer

15.15 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

15.16 Etch for 20 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs superlattice layer

15.17 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

15.18 Etch for 10 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAs etch stop layer

15.19 Gentle DI rinse and dry

15.20 Clean with Acetone and IPA

15.21 If necessary soak for 15 minutes in TRX @ 80°C and IPA rinse
15.21.1 Use a glass dish

16.0 Dektak sample
16.1 Locate defects

17.0 Spot remove defects

17.1 Inspect and map defect locations

17.2 Spin 4330
17.2.1 5K, 45sec, 90sec bake @ 95ºC
17.2.2 Repeat (two coats necessary)

17.3 Expose defects with height on microscope (150x)
17.3.1 Exposure 5sec develop 60sec

17.4 Etch using 3:1 H_3PO_4:HCl and 1:1:10 H_2SO_4:H_2O_2:H_2O

17.5 Inspect

17.6 Strip PR with Acetone and IPA

17.7 Tergitol spray clean

18.0 Universal Superlattice adjustment

18.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer

18.2 Etch 10 sec in 3:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer

~~**18.3 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP superlattice layer**~~

~~**18.4 Etch 10 sec in 3:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP superlattice layer**~~

18.5 DI rinse and N_2 blow dry

19.0 Etch WDM superlattice adjustment etches

19.1 Pattern with first mask layer
- 19.1.1 Spin 4330
  - 19.1.1.1 5K, 45sec, 90sec bake @ 95ºC
- 19.1.2 Edge bead removal
  - 19.1.2.1 Wait 5 minutes
  - 19.1.2.2 Expose edge bead 90 seconds
  - 19.1.2.3 Develop 2 minutes
- 19.1.3 Pattern Mask: ***NP BOND MASK 3*** Layer: ***Superlattice Etch 1***
  - 19.1.3.1 Align crosshairs
  - 19.1.3.2 Expose 18sec develop 90sec
  - 19.1.3.3 Use microscope to expose undeveloped patches
    - 19.1.3.3.1 5sec exposure, 30sec develop
  - 19.1.3.4 Tergitol spray clean if dirty
  - 19.1.3.5 O_2 descum 100W/300mT for 15sec

19.2 Etch step 1 (Even number of half periods removed – InP on top)
- 19.2.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP
- 19.2.2 Etch 30 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP
- 19.2.3 Gentle DI rinse
- 19.2.4 Strip PR with Acetone and IPA

~~**19.3 Etch step 1 (Odd number of half periods removed – InGaAsP on top)**~~
- ~~19.3.1 Etch 30 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP~~
- ~~19.3.2 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP~~
- ~~19.3.3 Gentle DI rinse~~
- ~~19.3.4 Strip PR with Acetone and IPA~~

19.4 Pattern second step
- 19.4.1 Spin 4330
  - 19.4.1.1 5K, 45sec, 90sec bake @ 95ºC
- 19.4.2 Edge bead removal
  - 19.4.2.1 Wait 5 minutes

19.4.2.2 Expose edge bead 80 seconds
19.4.2.3 Develop 2 minutes
19.4.3 Pattern Mask: ***NP BOND MASK 3*** Layer: ***Superlattice Etch 2***
19.4.3.1 Align crosshairs
19.4.3.2 Expose 18sec develop 90sec
19.4.3.3 Use microscope to expose undeveloped patches
19.4.3.3.1 5sec exposure, 30sec develop
19.4.3.4 Tergitol spray clean if dirty
19.4.3.5 O_2 descum 100W/300mT for 15sec

19.5 Etch step 2 (Even number of half periods removed – InP on top)
19.5.1 Etch 10 sec in 3:1 H_3PO_4:HCl to remove InP
19.5.2 Gentle DI rinse
19.5.3 Strip PR with Acetone and IPA

~~**19.6 Etch step 2 (Odd number of half periods removed – InGaAsP on top)**~~
~~19.6.1 Etch 30 sec in 1:1:10 H_2SO_4:H_2O_2:H_2O to remove InGaAsP~~
~~19.6.2 Gentle DI rinse~~
~~19.6.3 Strip PR with Acetone and IPA~~

19.7 If necessary soak for 15 minutes in TRX @ 80°C and IPA rinse
19.7.1 Use a glass dish

20.0 Dektak

21.0 PL Map

22.0 Bond InP epitaxial layers to patterned front GaAs mirror

22.1 Clean samples
22.1.1 Rinse with Acetone and IPA
22.1.2 Swab with Tergitol and spray with Tergitol
22.1.3 DI rinse and dry
22.1.4 O_2 descum (300 mTorr, 100W, 15sec)
22.1.5 Dip both in BOE for 5 seconds
22.1.6 DI rinse and dry

22.2 Bond Samples
- 22.2.1 Dip in NH_4OH for 1 minute
- 22.2.2 Wet transfer to Methanol
- 22.2.3 Wet transfer to wipe
- 22.2.4 Abut samples and flip InP onto GaAs
  - 22.2.4.1 ***USE 90° ROTATION! wr.t. superlattice etch and 0° rotation w.r.t.the nonplanar bond***
- 22.2.5 Place samples together on to graphite block
- 22.2.6 Tighten screws and rewet with Methanol
  - 22.2.6.1 Use 0.45 on torque wrench
- 22.2.7 Bond in furnace
  - 22.2.7.1 Use 85°C/min to 600°C for 30min
  - 22.2.7.2 –10°C/min to 300°C
  - 22.2.7.3 Step down to 25°C
- 22.2.8 Remove from fixture when below 100ºC

23.0 Lap front Substrate for removal

23.1 Lap to remove 370um
- 23.1.1 Use vacuum mount on lapped metal block
- 23.1.2 Use 12um grit

24.0 Polish back mirror GaAs substrate (unmarked side)

24.1 Mount and lap
- 24.1.1 Lap about 25um with 9μm grit paper
- 24.1.2 Clean fixture and sample thoroughly
- 24.1.3 Lap about 25um with 3μm grit paper
- 24.1.4 Clean fixture and sample thoroughly
- 24.1.5 Wipe on silk pad with Alumina powder and Bleach mixture
- 24.1.6 Immediate water rinse
- 24.1.7 Repeat silk pad and rinse until cloudiness is gone

25.0 Remove front mirror GaAs substrate (rough lapped side)

25.1 Wax mount to glass cover slip
- 25.1.1 Clean sample in heated 1165 stripper
- 25.1.2 Use SBT 135 wax and 170°C hot plate
- 25.1.3 Drop sample, lapped side up, onto heated wax onto center

of glass cover slip and allow to naturally flatten
25.1.4 Remove from hot plate and spin clean with acetone and IPA
25.1.4.1 3K spin speed
25.1.5 Swab and spray clean with Tergitol to remove wax residue

25.2 Etch
25.2.1 4:1 Citric:Peroxide (60ml H2O:60g Citric powder:25ml H2O2)
25.2.1.1 Stirring (facing away from bar), on 25°C plate
25.2.1.2 About 0.6um per minute: about 60 minutes
25.2.2 Remove after sample turns shinny and quick DI rinse

25.3 Promptly etch stop etch
25.3.1 Dip in 1:3 HCl:DI for 1 minute
25.3.2 Dip in 1:10 HF:DI for 20sec
25.3.3 Inspect and repeat 1:10 HF:DI dip if large amounts of debri remain

25.4 Remove non-bonded areas – only if large un-bonded areas exist
25.4.1 Spin SF15 and bake on 200°C hot plate
25.4.2 Strip PMGI with heated 1165
25.4.3 Acetone and IPA rinse
25.4.4 Repeat if necessary

25.5 Foam swab in Tergitol if necessary

25.6 Demount from glass slide

26.0 Etch Oxidation Holes

26.1 Deposit 2500A SiNx on sample
26.1.1 Spin clean with Acetone and IPA
26.1.2 O_2 descum (300 mTorr, 100W, 15sec)
26.1.3 Deposit 2500A SiNx on front side

26.2 Pattern oxidation holes on sample
26.2.1 Spin HMDS
26.2.1.1 10 second soak, 5K, 45sec

26.2.2 Spin 4330
26.2.2.1 5K, 45sec, 90sec bake @ 95ºC
26.2.3 Edge bead removal
26.2.3.1 Wait 5 minutes
26.2.3.2 Expose edge bead 90 seconds
26.2.3.3 Develop 2 minutes
26.2.4 Pattern Mask: ***MASK 4 (Iron Oxide)***
Layer: ***Oxidation Trenches***
26.2.4.1 Use IR aligner
26.2.4.2 Expose 20sec develop 60sec

26.3 Etch holes
26.3.1 CF4 etch SiNx 4min (300mT, 100W) sample
26.3.2 Cl etch
26.3.2.1 60 second 1:20 NH4OH:DI rinse, N2 dry
26.3.2.2 19.5 sccm BCl3, 1.5 sccm Cl2, 15mT, 75W
26.3.2.2.1 Lower electrode to 2.4”
26.3.2.3 Time: 6min (5 min minimum for top DBR)
26.3.2.4 DI rinse after immediately after etching
26.3.2.5 Remove PR with Heated 1165 stripper sample
26.3.2.6 Acetone and IPA rinse
26.3.2.7 Spin clean with Acetone and IPA
26.3.3 MHA Etch
26.3.3.1 O2 clean chamber (20sccm, 125mT, -500V 20min)
26.3.3.2 MHA precoat (4/20/10sccm, 75mT, -450V, 10min)
26.3.3.3 Load sample
26.3.3.4 MHA over-etch (4/20/10sccm, 75mT, -450V)
26.3.3.4.1 22min (15min for Active and 7 to stop on AlAs)
26.3.3.5 O2 clean sample (20sccm, 125mT, -300V 11min)
26.3.4 Etch AlAs surface layer sample and dummy piece
26.3.4.1 BOE dip 15sec and DI rinse
26.3.5 Cl etch sample
26.3.5.1 60 second 1:20 NH4OH:DI rinse, N2 dry

26.3.5.2 19.5 sccm BCl3, 1.5 sccm Cl2, 15mT, 75W
26.3.5.3 Time: 8min (7 min minimum for bottom DBR)
26.3.5.4 DI rinse immediately after etching

27.0 Oxidize

27.1 N2 @ 8, DI @ 80°C, Furnace @ 430°C

27.2 First cal @ 16minutes

27.3 Final time: _14 min_

28.0 Remove SiNx

28.1 CF4 etch SiNx 75 seconds (300mT, 100W)

29.0 Deposit pump targets

29.1 Spin OCG 825
29.1.1 5K, 45sec, 90sec bake @ 95ºC

29.2 Flood expose
29.2.1 10sec

29.3 Spin 4110
29.3.1 5K, 45sec, 90sec bake @ 95ºC

29.4 Pattern Mask: ***NP BOND MASK 3*** Layer: ***Pump Targets***
29.4.1 Use IR aligner
29.4.2 Align exposed cross should be just above the labels (R1)
29.4.3 Expose 10sec develop 45sec

29.5 Evaporate Ti/Au 50/1000

29.6 Liftoff in heated 1165 stripper

29.7 Acetone and IPA rinse

29.8 Tergitol spray and swab clean

30.0 Coat both sample sides with 1540 nm AR coating

30.1 Calibration: e-beam evaportate SiO on Si wafer – 8-10 A/sec

30.2 Measure reflectivity with spectrometer: Reflection minimum_1530nm_

30.3 Measure film index with filmetrics: _1.753____

30.4 O_2 descum sample (300 mTorr, 100W, 15sec)

30.5 Deposit on backside of sample

30.6 Repeat deposition on front side of sample