Vertical and Lateral Heterogeneous Integration

Jon Geske[1], Vijay Jayaraman[2], Yae L. Okuno[1], and John E. Bowers[1]

[1]University of California, Department of Electrical and Computer Engineering,
Santa Barbara, CA 93106, Tel: 1 805 893 4883, Fax: 1 805 893 7990
[2]Gore Photonics, 425 Commerce Court, Lompoc, CA 93436

The wafer-scale integration of advanced optical, electrical, and micromechanical semiconductor devices on a single chip requires techniques for combining differing semiconductor structures in the plane of the wafer. We have developed a technique for achieving large-scale monolithic integration of lattice-mismatched materials in the vertical direction and the lateral integration of dissimilar lattice-matched structures. The technique uses a single non-planar wafer-bonding step to transform epitaxial structures into lateral epitaxial variation across the surface of a wafer.

Non-planar wafer bonding begins with multiple epitaxial regions grown vertically on a wafer as shown for the case of four different regions in Fig. 1. The surface is then etched with a step shaped profile to reveal a different epitaxial region on each step level. The backside of the wafer is etched to have a profile complimentary to the step etched epitaxial film side of the wafer, as shown in Fig. 2(a). This substrate thickness adjustment etch is designed to yield an identical substrate plus epitaxial film thickness at each lateral point on the wafer. The lateral offset between the front side and backside step edges determines the distance over which the substrate and epitaxial layers must accommodate the deformation. The wafer is then direct wafer bonded [1] to a transfer substrate. We can remove the original growth substrate leaving the epitaxial layers attached to the transfer substrate as depicted in Fig. 2(b). At this point the excess epitaxial layers and the deformation accommodation regions are etched back, leaving a different epitaxial region at each lateral position on the transfer substrate as represented by Fig. 2(c).

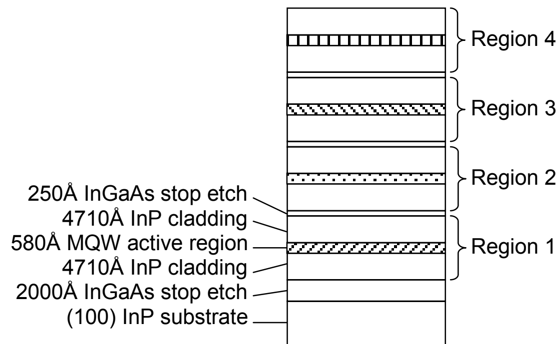

Fig. 1: Structure schematic

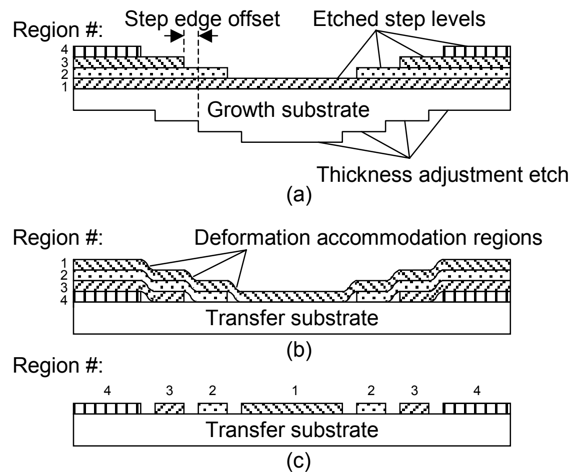

Fig. 2: Process flow cross-sections

We have used this technique to integrate onto a GaAs wafer surface four different unstrained multi-quantum well (MQW) active-regions grown lattice-matched on InP (Fig. 1). The MQW active-regions consisted of three 60Å InGaAsP quaternary (Q) quantum wells with 100Å 1.1-µm Q barriers. Each of the four regions were separated by a 250Å InGaAs stop etch layer for ease of processing and substrate removal. The photoluminescence (PL) peaks of the four regions were intentionally different and located at 1280, 1336, 1260, and 1320nm, listed in order of their growth on the substrate. Each region had a thickness of 1µm, for a total epitaxial film thickness of about 4µm.

The epitaxial layers were etched with a step profile to reveal a different region on each step level. The step levels were 500µm wide and 1.025µm high. The substrate was thinned to 200µm and the backside was etched with the same step profile as the epitaxial film side, except with a 200µm lateral step edge offset. The semiconductor direct wafer bond was performed at 630°C for 30 minutes in a nitrogen gas ambient under pressure in a graphite fixture. The pressure used (3 MPa) was in the same range used in the planar bonding of InP to GaAs in the fabrication of 1.55µm vertical-cavity surface-emitting lasers (VCSELs) [2].

After bonding the InP to the GaAs transfer substrate, the InP substrate was removed and the excess epitaxial layers and the deformation accommodation regions were etched back by selective chemical etching to reveal

well-bonded stripes of MQW active regions across the GaAs transfer substrate surface. Fig. 3 shows the stripes of epitaxial regions separated by the etched deformation accommodation regions. The roughness of the deformation accommodation regions is due to the uneven etching of the GaAs transfer substrate during the etch-back process. PL measurements recorded after wafer bonding are shown in Fig. 4. The PL prior to wafer bonding is not shown, but comparison with the PL plots in Fig. 4 indicates no degradation in the intensity, no shift in the wavelength, and no broadening of the PL peaks after wafer bonding. Optical inspection of the surface shows a well-bonded surface with very little damage due to bonding. Scanning electron microscope (SEM) micrographs of the bonded interface also reveal a uniform wafer bonded interface.

The combination of good PL and a mechanically well-bonded surface supports our conclusion that the non-planar wafer bonding technique shows promise as a method for achieving vertical and lateral heterogeneous integration across a wafer. We believe that this technique may allow for the monolithic integration of various optical, electrical, and micromechanical components on a single wafer, including the integration of electronics with lasers, photodetectors, and modulators.

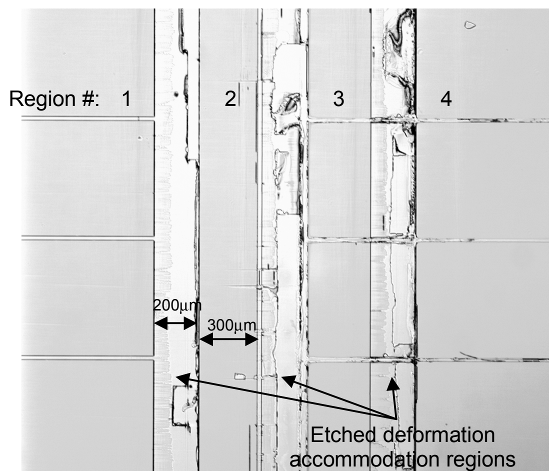

Fig. 3: Wafer surface after non-planar bonding

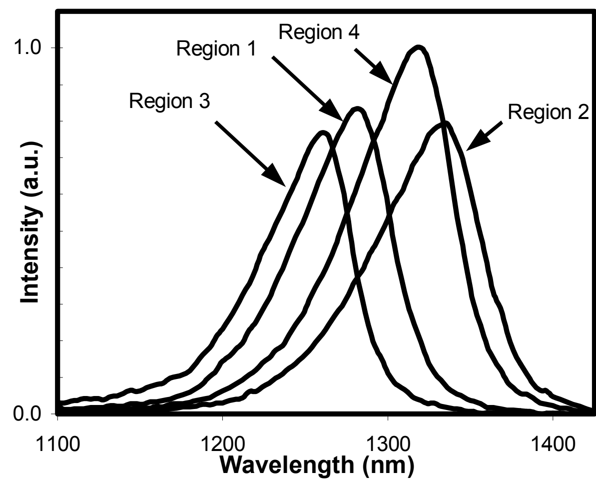

Fig. 4: PL after non-planar bonding

We propose using non-planar wafer bonding to achieve two-dimensional Wavelength Division Multiplexed (WDM) VCSEL arrays. By using non-planar wafer bonding an array with a wavelength range beyond the gain bandwidth of a single active region can be achieved. Coarse wavelength control can be achieved in the lateral dimension using non-planar wafer bonding, and fine wavelength control can be achieved in the transverse dimension using cavity mode adjustment etches as described in Ref. [3]. Fig. 5 shows a schematic of a proposed example structure for emission from 1275nm to 1350nm.

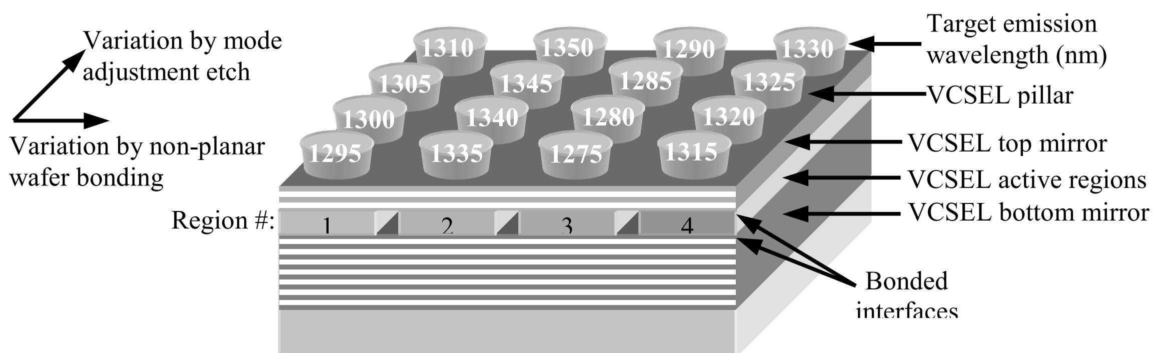

Fig. 5: Schematic of proposed two-dimensional VCSEL array using non-planar wafer bonding

References:

[1] Z. Liau and D. Mull, App. Phys. Lett. 56, 737 (1990).

[2] A. Black, A. Hawkins, N. Margalit, D. Babic, A. Holmes, Jr., Y. Chang, P. Abraham, and J. Bowers, IEEE Journal of Selected Topics in Quantum Electronics 3, 943 (1997).

[3] V. Jayaraman and M. Kilcoyne, Proc. SPIE 2690, 325 (1996).