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SiGeC Cantilever Micro Cooler

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ABSTRACT

The fabrication and characterization of SiGeC cantilever microcoolers are described. Silicon on insulator (SOI) was used as the substrate, and two layers of 3 µm p-$SiGe_{0.07}C_{0.0075}$ and 1.14 µm n-$SiGe_{0.07}C_{0.0075}$ lattice matched to silicon were grown using molecular beam epitaxy. The uni couple cooler was fabricated using conventional integrated circuit (IC) processing, and the cantilever structure was finally formed by removing the backside Si of SOI substrate by deep reactive ion etching. Devices with different n- and p-side length ratios were characterized. Cooling by 1.2K has been measured at room temperature. Modeling showed that the device performance was dominated by the smaller cooling temperature of the p-SiGeC leg of the cantilever structure. Parasitic heat conduction through the Si buffer layer is the main limitation to the device performance.

INTRODUCTION

Heat generation and thermal management are becoming one of the barriers to further increase speeds and decrease feature sizes in integrated circuits. Thin film coolers that can be monolithically integrated with high speed, high power electronic and optoelectronic devices have been an active area of research [1-3].

Due to the larger lattice constant of germanium compared to silicon (4.2%), Ge and SiGe grown on silicon are compressively strained, thus buffer layers are required for the growth of thick Si/Ge and SiGe/Si superlattice layers. This increases the cost of material growth and the complexity of integration with Si-based devices. By adding a small amount of carbon into the SiGe material system, strain can be adjusted due to the small lattice constant of carbon. By properly selecting the Ge and C ratio, SiGeC can be lattice matched to silicon, and thick SiGeC or SiGeC/Si superlattice can be directly grown on Si without strain.

For potential integration with silicon circuits, studies on SiGe/Si and SiGeC/Si microcoolers have been carried out [4-6]. Single element microcoolers are usually limited by the heat conduction from substrate to the cooling side via electrode metal pads. In addition, in these short leg structures, transferring the heat perpendicular to the thin film layer, requires large current densities and thus Joule heating in the electrodes and in metal-semiconductor contact layer could dominante. Using a cantilever structure to transfer heat in the plane of the thin film is a promising solution to the problems for micro coolers [7-9]. Previous demonstrations used selective growth of n- and p-layers in different areas of the substrate and there were limitations due to the material quality. Here we use an alternative solution with only a single MBE growth of the whole structure. As we will see in the following, while this introduces some parasitic heat

conduction paths, uni-couple coolers made of n- and p-legs are demonstrated and cooling by 1.2C has been achieved.

MATERIAL GROWTH AND DEVICE FABRICATION

The sample was grown in a Perkin-Elmer Si molecular beam epitaxy (MBE) growth chamber on a 125 mm diameter silicon on insulator (SOI) wafer consisting of 200 nm silicon on 3 μm SiO_2 layer and 500μm silicon substrate. The 200 nm silicon layer was used as growth buffer, and the cantilever structures were supported by the 3 μm thick SiO_2 membrane. First 3 μm p-type $SiGe_{0.07}C_{0.0075}$ layer was grown, followed by 1.1 μm n-$SiGe_{0.07}C_{0.0075}$ layer. The compositions of the $SiGe_{0.07}C_{0.0075}$ layers were designed so that the lattice constant matches that of silicon. The p-$SiGe_{0.07}C_{0.0075}$ layer was doped to approximately 5 x 10^{19} cm^{-3} by B, and n-$SiGe_{0.07}C_{0.0075}$ doped to approximately 5 x 10^{19} cm^{-3} by Sb.

The device structure is shown in Figure 1. The device consists of two mesas on the 3 μm SiO_2 layer. These two mesas are connected with metal. The jointing surfaces of the metal and the two legs form the device's cooling interfaces. One of the legs is composed of a mesa of 1.1 μm high n-SiGeC on 3 μm high p-SiGeC on the 200 nm Si buffer layer; the active cooling layer of this leg is the top 1.1 μm n-SiGeC layer. In a typical bias condition to achieve cooling, no current will flow through the p-layer of this leg. The other leg consists of 2.6 μm p-SiGeC mesa on the 200 nm Si buffer. These two legs of different heights were formed by using twice dry etches; the first etch was from the top n-SiGeC down to p-SiGeC with the etch depth of 1.5 μm; the second went from the first etch stop down to the SiO_2. A 3 μm metal of Ti/Al/Ti/Au was deposited to connect these two legs and to form probe pads. The cantilever structure was finally realized by removing the silicon substrate of the SOI beneath the device cooling interfaces. Figure 2 shows the bottom view of the final formed cantilever device structures. By removing the substrate and isolating the cooling junction, the device performance is improved. Physically, the structure consists of two coolers; one is n-type, and the other is p-type. The cooling interfaces of these two coolers are connected with metal, therefore the device overall performance will be determined by the smaller cooling of the two legs. One should note that to achieve cooling, electrons are injected from the one mesa's p-SiGeC to the metal and then to the n-SiGeC on the other mesa. Thus the pn-junction which is formed under the n-leg is reverse biased. This is the reason that the two leg structure can be grown using a single MBE growth. Heat conduction through the p-SiGeC underneat n-SiGeC, is parasitic and reduces the overall cooling performance, but we will see that this is not a major dominant factor.

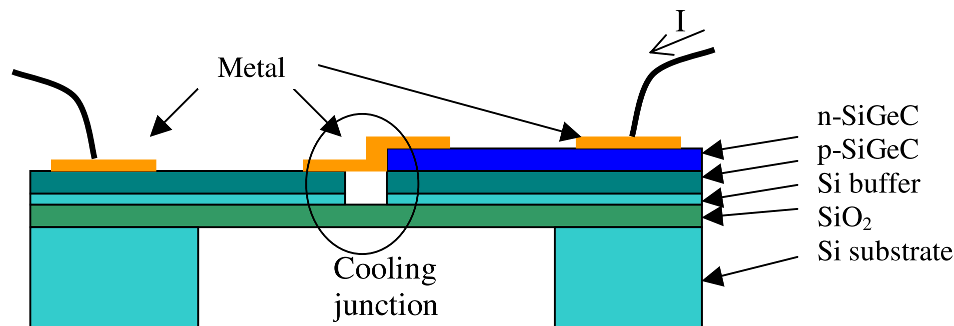
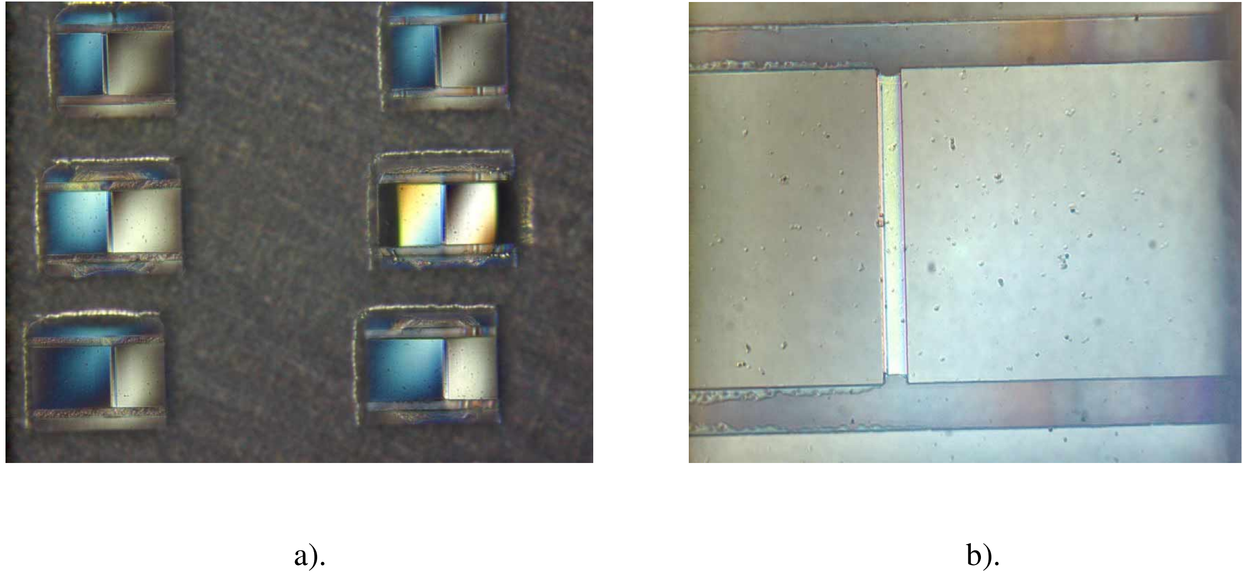


Figure 1. Schematic diagram of a SiGeC cantilever thin film microcooler.



a). b).

Figure 2. Bottom view of a SiGeC cantilever structure when the 500 μm Si of the SOI substrate has been removed. a) Six cantilever microcoolers with different n and p side length ratio. b) Backside view of a cantilever microcooler on the 3 μm SiO_2 membrane of the SOI substrate.

DEVICE MODELING

Additional SiGeC samples for material property measurements were grown on semi-insulating silicon substrates with MBE. The Seebeck coefficient, doping, and mobility of these materials were measured and thus the thermoelectric power factor was derived. The SiGeC cantilever cooler device was grown on SOI wafer using similar growth conditions. Unfortunately, we did not have calibration samples with the exact structure of the cantilever device, but the compositions are quite similar. Table 1 shows some of material characterization results.

Table 1. Measurement results for SiGeC alloy grown using MBE.

Type	Structure	Doping (cm^{-3})	Mobility (cm^2/Vs)	Seebeck (μV/ K)	$S^2\sigma$ (W/cmK^2)
n	2.0μm $Si_{0.89}Ge_{0.1}C_{0.01}$	4.31×10^{18}	80.53	-470	1.23×10^{-5}
n^-	0.968μm $Si_{0.8925}Ge_{0.1}C_{0.0075}$	9.0×10^{14}	205	-4630	6.33×10^{-7}
p	0.613μm $Si_{0.8925}Ge_{0.1}C_{0.0075}$	6.3×10^{19}	10.6	230	5.65×10^{-6}

When the doping is very low, such as sample, the Seebeck coefficient and mobility is large, but the power factor is low, which means that the maximum cooling temperature for this material will be small. It is obvious that low doping is generally not suitable for micro cooler applications. Our measurements show that the thermelectric power factor $S^2\sigma$ for n-SiGeC is a factor of two larger then that of p-SiGeC, so microcoolers of n-SiGeC will get much more cooling temperature difference than that of p-SiGeC ones. As n-SiGeC and p-SiGeC cooling interfaces are closely connected to each other with 3 μm Au layer, the overall performance of cantilever cooler will be limited by p-SiGeC leg. It would be better for both p and n materials to have similar thermoelectric power factors.

There are several non-ideal factors that affect the overall performance of microcoolers, such as contact resistance, Joule heating from electrodes and heat conduction, but unlike single element thin film microcoolers; contact resistant is no longer the crucial limitation to the cantilever microcooler performance. This is because of longer leg lengths on the order of 100-200 microns, cantilever resistance is much greater than that of single element thin film microcooler. The ratio of contact resistant r_c to the device inherent resistance R, r_c/R, is very small on the order of 10^{-2}. With the specific contact resistance on the order of 10^{-6} to 10^{-7} Ωcm^2, the effect of r_c on maximum cooling temperature is thus very small.

The cantilever structure consists of two legs, and the heat pump rate for each of the n- or p-legs can be approximately described as:

$$Q_c = ST_cI - 0.5I^2d/\sigma A - \Delta T\kappa A/L \quad (1)$$

Where S is the Seebeck coefficient, T_c is the temperature of the cold side, σ is electrical conductivity, κ is thermal conductivity, A is the cross section area of the cantilever leg; ΔT is the temperature difference, and L the cantilever leg length.

If there were no parasitic thermal conduction layers for each side, such as the p-SiGeC and Si buffer layers of the n-type device mesa, and the Si buffer layer of the p-type mesa, the maximum cooling temperature $(\Delta T)_{n_max}$ for n-side and $(\Delta T)_{p_max}$ for p-side of the cantilever structure can be expressed as:

$$(\Delta T)_{n_max} = 0.5Z_nT_c^2 = 0.5S_n^2T_c^2\sigma_n/\kappa_n \quad (2)$$

$$(\Delta T)_{p_max} = 0.5Z_pT_c^2 = 0.5S_p^2T_c^2\sigma_p/\kappa_p \quad (3)$$

The maximum cooling temperatures for n-side $(\Delta T)_{n_max}$ and p-side $(\Delta T)_{p_max}$ are calculated to be about 12 K and 2.5 K respectively based on the measured material values in table 1 for the SiGeC samples.

By taking into account the effects from parasitic thermal conduction due to inactive layers, the effective thermal conductivity for n-SiGeC and p-SiGeC legs can be approximately expressed as:

$$\kappa_n = (A_{SiO2}\,\kappa_{SiO2} + A_{Si}\,\kappa_{Si} + A_{n\text{-}SiGeC}\,\kappa_{n\text{-}SiGeC} + A_{p\text{-}SiGeC}\,\kappa_{p\text{-}SiGeC}) / A_{p\text{-}SiGeC} \quad (4)$$

$$\kappa_p = (A_{SiO2}\,\kappa_{SiO2} + A_{Si}\,\kappa_{Si} + A_{n\text{-}SiGeC}\,\kappa_{n\text{-}SiGeC}) / A_{n\text{-}SiGeC} \quad (5)$$

where $A_{p\text{-}SiGeC}$ and $A_{n\text{-}SiGeC}$ are the p-SiGeC and n-SiGeC active layer cross section area, and A_{Si} and A_{SiO2} are the Si buffer layer and SiO_2 layer cross section area respectively. κ_{SiO2}, κ_{Si}, $\kappa_{p\text{-}SiGeC}$ and $\kappa_{n\text{-}SiGeC}$ are the thermal conductivities of SiO_2, Si buffer layer, p-SiGeC and n-SiGeC layers respectively.

The calculated maximum cooling temperature is 4.2 K for n-side $(\Delta T)_{n_max}$, and 1.2 K for p-side $(\Delta T)_{p_max}$ respectively. Therefore, the two-leg cantilever device maximum cooling temperature will be 1.2 K, which is determined by the p-side. By studying various parameters, we see that the main limitation to the device performance is the heat flow from the Si buffer layer on the p-side. Figure 3 shows the effect of the Si buffer layer thickness on the cooling of p-side SiGeC mesa.

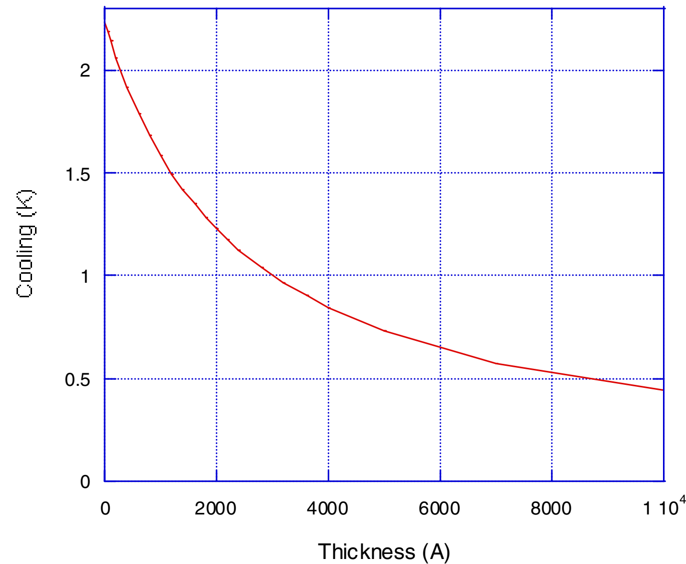


Figure 3. The maximum cooling temperature versus silicon buffer thickness for p-side SiGeC cantilever structure.

RESULTS AND DISCUSSIONS

SiGeC cantilever micro coolers with various widths and length ratios of n- to p-legs were fabricated. Cooling temperatures over 1.2 K have been measured with use of micro-thermocouples at room temperature. Figure 4 shows the measurement result for a cantilever device that is 250 μm wide and about 300 μm long. n and p-legs have equal lengths. The inherent resistance is about 30 Ω. The ohmic contact areas for n and p sides are 230 × 10 μm^2. With the specific contact resistivity on the order 10^{-6} to 10^{-7} Ωcm^2 as measured in our transmission line method (TLM) experiments, the contribution from contact resistance is much less than the device body resistance, so it is no longer the major limitation to the device performance.

As the p-SiGeC layer and n-SiGeC layers have different electrical conductivity and Seebeck coefficients, their optimal currents for maximum cooling are different. The optimal current can be expressed as:

$$I_{opt} = ST_cA\sigma/L \quad (6)$$

Since the two legs are electrically in series, in order to achieve maximum cooling both sides should be designed to have the same optimum current. From equation (6), we can see that this can be achieved by making $S_nL_p = S_pL_n$; where S_n, S_p are Seebeck coefficients and L_p and L_n are the mesa lengths, for the n-side and p-side respectively. Figure 5 shows the experimental results for different length ratio of n-side leg to p-side leg. The best cooling was obtained with the

devices with mesa length ratio L_n/L_p ~ 1/2 to 3/2, which is very close to our Seebeck measurements for p and n SiGeC samples, which shows the S_p/S_n is about 1/2.

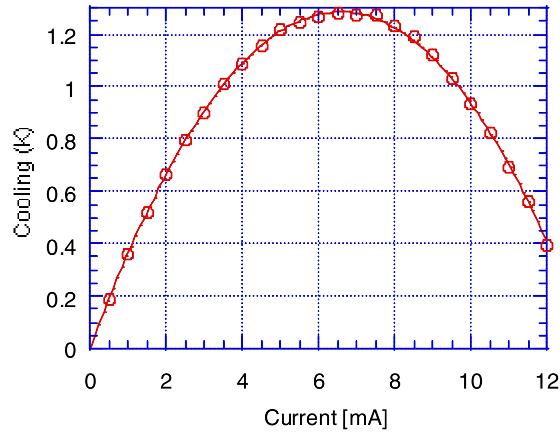


Figure 4. Measured results for 250 μm width cantilever devices.

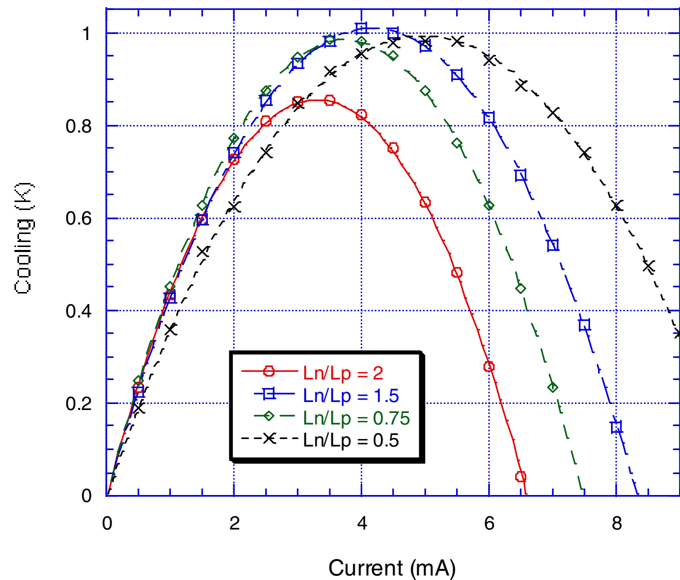


Figure 5. Measured results for cantilever devices with different n and p leg length ratio.

The primary limitation to the cooler performance is parasitic thermal conduction through the buffer layers. The parasitic thermal conduction for the p-side leg comes mainly from silicon buffer layer; while for the n-side, the parasitic thermal conduction come from both the silicon

buffer layer as well as the p-SiGeC layer beneath the n-SiGeC one. As our calculations indicate that the cooling for p-side leg is smaller than that for n-side, the device performance will be limited mainly by the thermal conduction from the 200 nm Si buffer layer beneath the p-side p-SiGeC.

CONCLUSION

Cantilever microcoolers were fabricated using single epitaxial growth and standard IC processing. Cooling by 1.2K has been measured at room temperature. The overall cantilever device cooling temperature is determined to be limited by the p-SiGeC, which has lower cooling ability than that of the n-SiGeC. Modeling calculations and measurement results show that the main limitation to the device performance is the parasitic thermal conduction from the 200 nm Si buffer layer of SOI substrate.

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