2.56 Tbps (8 × 8 × 40 Gbps) Fully-Integrated Silicon Photonic Interconnection Circuit

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Abstract: We demonstrate a fully-integrated photonic Wavelength Division Multiplexing (WDM) transceiver circuit with heterogeneous integration on silicon, and on-chip interconnection with total transmission capacity up to 8×8×40 Gbps.
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1. Introduction

Silicon photonics technology has promise to overcome the I/O limit of copper interconnects, and achieve high-speed and cost-effective chip level photonic interconnection to enable future Exascale performance computers and datacenters [1]. For a realistic on-chip and inter-chip optics link, bandwidth density and total power consumption are the major challenges. Consequently, fully integration of all photonics components on chip, with high speed modulators and photodetectors, and especially lasers as light source, is needed for scalable and energy efficient system topology designs. A library of functional devices on Si have been developed on silicon with the heterogeneous integration method, including low loss waveguides, low threshold distributed feedback (DFB) lasers, high speed electroabsorption modulators (EAM) and photodetectors on silicon [2, 3], enabling a large scale photonic integration implementation. In this paper we demonstrate a high speed heterogeneous integrated circuit on silicon for on-chip interconnection. An eight-node ring-bus network architecture was utilized with eight-channel WDM transmitters and receivers in each node.

2. Photonics circuit architecture

A schematic of the photonic transceiver circuit is shown in Fig. 1. Eight transceiver nodes connect to the ring-bus silicon waveguide with a broadband switch. Extra switches on the bus are connected with ports to facet port for fiber coupling or lead to monitoring individual devices. By thermally controlling the switch array, the signal generated at transmitter (Tx) at one node is routed to the receiver (Rx) of other nodes or coupled out of chip through optical fiber. Each transmitter has 8 channels with single mode short cavity DFB laser [4], monitoring photodetector (MPD) and EAM on each channel [5]. The corresponding receiver has PIN type InGaAs photodetectors (PD) and semiconductor optical amplifiers (SOA) on part of the channels. Eight-channel array waveguide gratings (AWGs) were used as multiplexer and demultiplexer (Mux/DeMux) with 200 GHz channel space in C/L band. The switches in the architecture utilize a Mach-Zehnder interferometer formed with two 3-dB adiabatic couplers (AC) on silicon, for a broadband operation for the WDM signal.

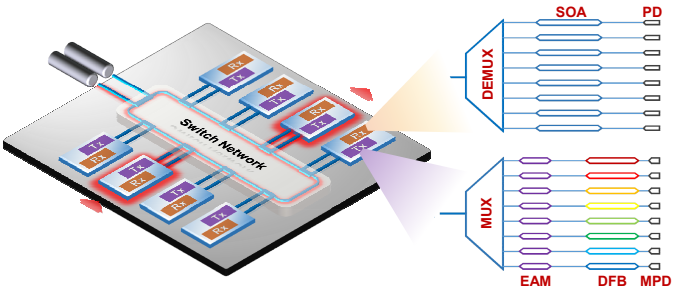

Fig. 1 Architecture of the heterogeneous integrated transceiver circuit

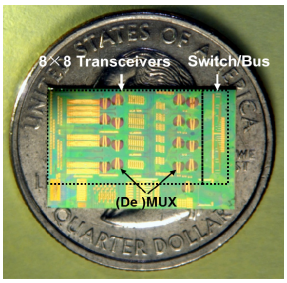

Fig. 2 Photo of transceiver circuit

The CMOS compatible fabrication of the transceiver circuit includes two major parts: silicon process on silicon on insulator (SOI) substrate, e.g. definition of Bragg grating, waveguide, switches and AWGs; III/V process for active components after III/V die bonding. In order to optimize the performance of individual devices, the III/V layer stack for DFB/SOA, EAM and PD were designed and grown separately, and selectively transferred to patterned SOI substrate. The actual layout of the transceiver chip as shown in Fig. 2, was adjusted to accommodate the bonded epi positions.

3. Performance characterization

The performance of the AC switch is shown in Fig. 3. By thermally tuning with a TiPt heater, a minimum extinction ratio (ER) of 16 dB between the on and off status was achieved across the transceiver wavelength from 1550 nm to 1575 nm, with low insertion loss below 1 dB. Fig. 4 shows the light-current and current-voltage curve of DFB lasers on silicon with 400 μm long and 26 μm wide mesa and 1 μm wide Si waveguide. The laser has a threshold current of 7.5 mA with a threshold current density of 470 A/cm^2 at 20 °C. The insert in Fig. 4 shows its single wavelength operation above threshold, with a side mode suppression ratio larger than 55 dB. Fig. 5 shows the transmission spectrum of two back-to-back cascaded AWGs on one waveguide, representing the alignment between two AWGs in corresponding Tx and Rx. The total insertion loss is below 3 dB after two AWGs, with a transmission non-uniformity of all eight channels better than 0.5 dB and a cross talk level about -28 dB. The normalized DFB lasing spectrum within the AWG channels are shown in same plot. The transmission spectrum of the EAM integrated on the same chip with 100 μm long cavity, as shown in Fig. 6, shows a wide working optical bandwidth from 1550 nm to 1580nm, and ER better than 5 dB with 1 V bias swing. The process yield of passive components was close 100%, and an overall yield was about 90% including active and passive components.

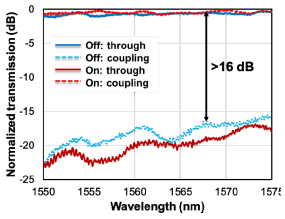

Fig. 3 Transmission spectrum of AC switch

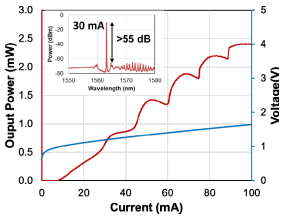

Fig. 4 LI and IV curves of 400 μm DFB and spectrum

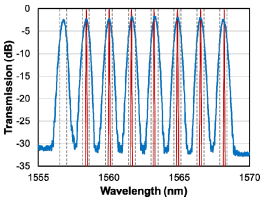

Fig. 5 Transmission spectrum of cascaded AWGs and DFBs spectrum in the eight channels

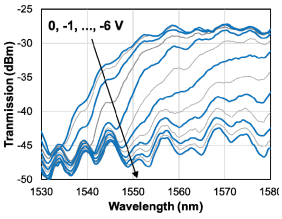

Fig. 6 Transmission spectrum of EAM with reverse bias

Fig. 7 shows the setup of the on-chip communication test. The switch array was controlled by a multi-pin DC probe card to route signal among transceivers. The DFB current and AWG heaters were adjusted appropriately to align the lasing wavelength to the transceiver channels. The small signal response of the transmitter-receiver link was characterized, and shows a 6-dB bandwidth of EAM+PD of 24 GHz as shown in Fig. 8. The data transmission test was applied with a 40 GHz pattern generator and 2^7-1 PRBS signal. Data rate up to 40 Gbps per channel performance is shown in Fig. 9, with the vertical scale in the eye diagram of 50 mV/div. Although only one channel can be tested simultaneously due to the driver limit, the result shows a potential large capacity of the transceiver array, with 320 (8×40) Gbps per transceiver, and 2.56 Tbps (8×320 Gbps) for the whole interconnection circuit.

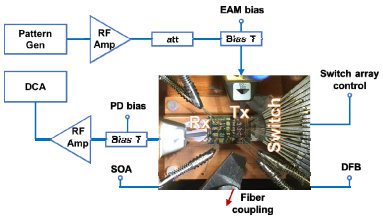

Fig. 7 Setup for on-chip link test

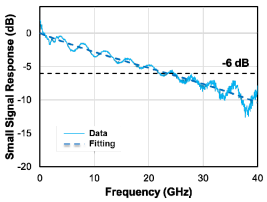

Fig. 8 Small signal response of EAM-PD channel

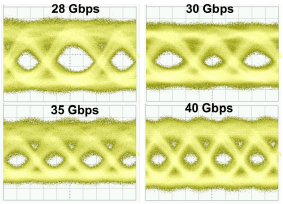

Fig. 9 Eye diagram of on-chip communication

4. Summary and conclusions

In this paper we show breakthrough results on a fully integrated photonics interconnection circuit on silicon. With heterogeneous integration of III/V materials on Si, over 400 functional components (including passive components) were integrated into a system with large communication capacity, promising a solution for future low cost and large bandwidth chip level interconnection.

5. References

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