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Citation: Applied Physics Letters **107**, 081106 (2015); doi: 10.1063/1.4929441
View online: http://dx.doi.org/10.1063/1.4929441
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/107/8?ver=pdfcov
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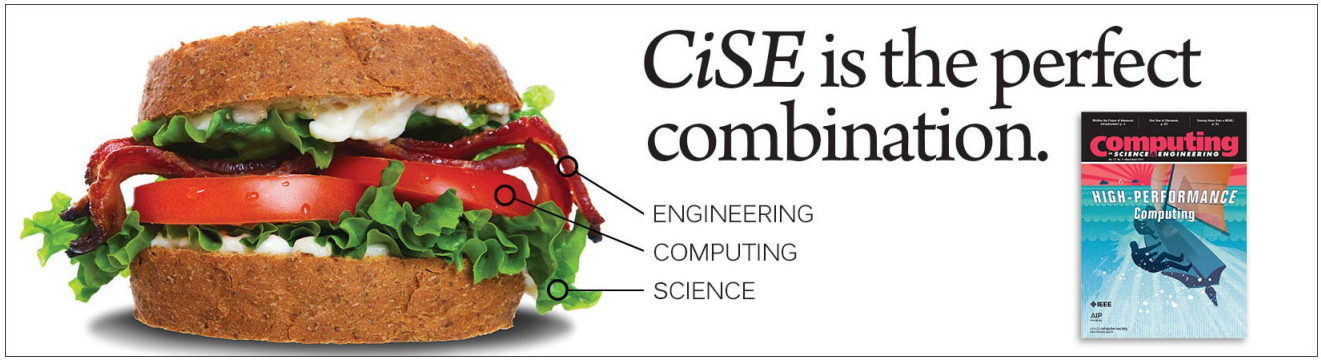

InAs/GaAs quantum dots on GaAs-on-V-grooved-Si substrate with high optical quality in the 1.3 μm band

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(Received 10 June 2015; accepted 12 August 2015; published online 24 August 2015)

We report self-assembled InAs/GaAs quantum dots (QDs) grown on a specially engineered GaAs-on-V-grooved-Si substrate by metal-organic vapor phase epitaxy. Recessed pockets formed on V-groove patterned Si (001) substrates were used to prevent most of the hetero-interfacial stacking faults from extending into the upper QD active region. 1.3 μm room temperature emission from high-density ($5.6 \times 10^{10}\,cm^{-2}$) QDs has been obtained, with a narrow full-width-at-half-maximum of 29 meV. Optical quality of the QDs was found to be better than those grown on conventional planar offcut Si templates, as indicated by temperature-dependent photoluminescence analysis. Results suggest great potential to integrate QD lasers on a Si complementary-metal-oxide-semiconductor compatible platform using such GaAs on Si templates. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4929441]

Integration of III-V lasers operating at optical communication wavelengths on Si substrates represents one major step towards on-chip optical interconnect.[1] Currently, hybrid III–V-on-Si technology appears to be most mature and has demonstrated the most advanced integrated devices and photonic circuits.[1,2] Monolithic integration by direct epitaxial growth offers an alternative with potential lower cost and improved yield. Yet, heteroepitaxy is extremely challenging, due to the formation of a high density of dislocations and antiphase-domains (APDs).[3] Recent demonstration of high-performance 1.3 μm quantum dot (QD) lasers directly grown on Ge-on-Si and Si substrates by molecular beam epitaxy (MBE)[4–10] has spurred renewed interest in pursuing epitaxial lasers on Si. The three-dimensional nature of QDs is less vulnerable to non-radiative defects as compared with their quantum well counterparts, leading to improved performance and longer lifetime for lasers.[10] So far, all these QD lasers have been exclusively grown on offcut Si substrates,[4–10] thereby compromising full compatibility with the mainstream Si complementary-metal-oxide-semiconductor (CMOS) platform. In addition, there are only limited studies on the growth and characterization of InAs/GaAs QDs on Si by metal-organic vapor phase epitaxy (MOVPE),[11] which is the preferred growth technique in CMOS manufacturing.

Recently, we reported a strategy to extend the growth of planar GaAs nanowires on (001) Si to antiphase-domain-free GaAs thin films.[12] By utilizing V-grooved Si (111) surfaces and a specially engineered "tiara"-like patterned-Si structure, most of the defects can been localized in the V-grooves, leading to high-crystalline-quality GaAs-on-V-grooved-Si (GoVS) (001) substrates. In this paper, we move forward to explore self-organized InAs/GaAs QDs grown on the GoVS substrates using MOVPE. Highly uniform QDs with density above $10^{10}\,cm^{-2}$ and ground state emission of $\sim$1.3 μm at room temperature (RT) were obtained. The identical QD active structure has been grown on a lattice-matched GaAs substrate and a 1-μm GaAs buffer on a planar (001) Si wafer with a 4° offcut angle for comparisons. Atomic force microscopy (AFM), transmission electron microscopy (TEM), and temperature-dependent photoluminescence (PL) were conducted, revealing superior structural and optical properties of the QDs on the V-groove patterned Si over traditional offcut Si substrate.

The material growth was conducted in an Aixtron AIX-200/4 MOVPE system. The GoVS substrate consisting of 1-μm GaAs thin film on V-groove patterned (001) Si was prepared using the same procedure as reported in Ref. 12. Meanwhile, a 1-μm GaAs-on-silicon template was grown on a 4° offcut Si substrate using the two-step growth method[13] for comparison. The high-crystalline-quality GoVS substrate was put into the reactor together with the offcut Si template and a GaAs substrate side by side for the subsequent growth of the QD structure. A thin GaAs buffer of 100 nm was first grown at 630 °C. Then, the temperature was decreased to 500 °C to grow a 2 nm $In_{0.12}Ga_{0.88}As$ wetting layer (WL) with a growth rate of 2 nm/min. This was followed by a 1.9 monolayer (ML) InAs deposition with a low growth rate of 0.63 ML/min and a V/III mole ratio of 0.375. The V/III ratio of 0.375 was chosen so that a high density of InAs QDs with few large coalesced islands can be achieved. A growth interruption of 20 s was introduced subsequently, without tertiarybutylarsine (TBA) flux to facilitate dots formation. An additional 50 nm GaAs capping layer was grown on top with a growth rate of 15 nm/min for PL evaluation. A schematic of the QD structure on the patterned Si substrate is shown in Fig. 1.

TEM characterization was conducted using a JEOL2010F field-emission microscope operating at 200 keV to analyze structural properties. Taken along the [110] zone axis, the cross-sectional bright-field TEM images in Figs. 2(a) and 2(b) present the QD structure grown on the GoVS substrate and on the planar offcut Si template, respectively. Plane-view TEM was used to quantify threading dislocation density (TDD). The TDD was determined by counting numbers of dislocations in a given area based on an average

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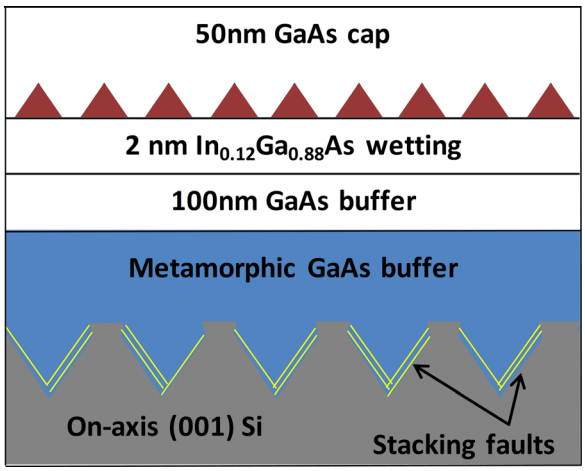

FIG. 1. Schematic of InAs/GaAs quantum-dots on the GoVS substrate.

number of 30 plane-view TEM images for accuracy. Figs. 2(c) and 2(d) show typical plane-view TEM images of the GoVS substrate and the offcut silicon template, respectively. A three-fold reduction of TDD was achieved on the GoVS substrate ($2.77 \times 10^8\,cm^{-2}$) as compared to the offcut silicon template ($8.31 \times 10^8\,cm^{-2}$). In the GoVS substrate, most defects generated at the GaAs/Si hetero-interface were trapped by the V-grooved structure, as highlighted in Fig. 2(e). While in the offcut Si template, a larger amount of stacking faults (SFs) and threading dislocations were observed in the GaAs buffer. Some of the dislocation lines punch through the active region and hence create non-radiative recombination centers, as evidenced by Fig. 2(f). A zoomed-in TEM image of the QD active region on the GoVS substrate is given in Fig. 2(g), showing that low defect density can be attained in the upper grown active region to facilitate the formation of uniform dot arrays. A high resolution TEM image is given in Fig. 2(h), revealing the typical size and shape of the dots. These results clearly show that the specially engineered GoVS substrate not only eliminates the necessity of using offcut Si substrates to suppress APD formation[12] but also exhibits distinct superiority over the traditional offcut Si template in defect trapping and reduction.

Surface morphologies of the uncapped samples were characterized by AFM to reveal the size, density, and distribution of the QDs. As shown in Fig. 3, highly uniform QDs have been achieved, with densities of $6.2 \times 10^{10}\,cm^{-2}$, $5.6 \times 10^{10}\,cm^{-2}$, and $4.8 \times 10^{10}\,cm^{-2}$ on the GaAs substrate, the GoVS substrate, and the offcut Si template, respectively. The density of coalesced dots on the GoVS substrate is slightly higher ($2.1 \times 10^9\,cm^{-2}$) compared to that on the GaAs substrate ($1.5 \times 10^9\,cm^{-2}$), but much smaller compared to the one on the offcut Si template ($3.4 \times 10^9\,cm^{-2}$). The larger density of coalesced islands formed on the offcut Si template could be attributed to the more defective buffer and, as a result, is responsible for the inferior PL performance.

Temperature-dependent PL measurements were carried out to compare optical properties using a 671 nm all-solid-state red laser as the excitation source. As shown in Fig. 4(a), the ground-state emission of the QDs grown on the GoVS substrate takes place at ~1300 nm at room temperature (RT). The PL curve yields a narrow full-width-at-half-maximum (FWHM) of 29 meV. The peak intensity was lower by a factor of 2 and peak wavelength blue-shifted by 10 nm compared to that grown on the native GaAs substrate. The RT-PL for QDs on the offcut Si template is obviously poorer compared to that on the GoVS substrate (0.6 times smaller in peak intensity and 1.2 times broader in line-

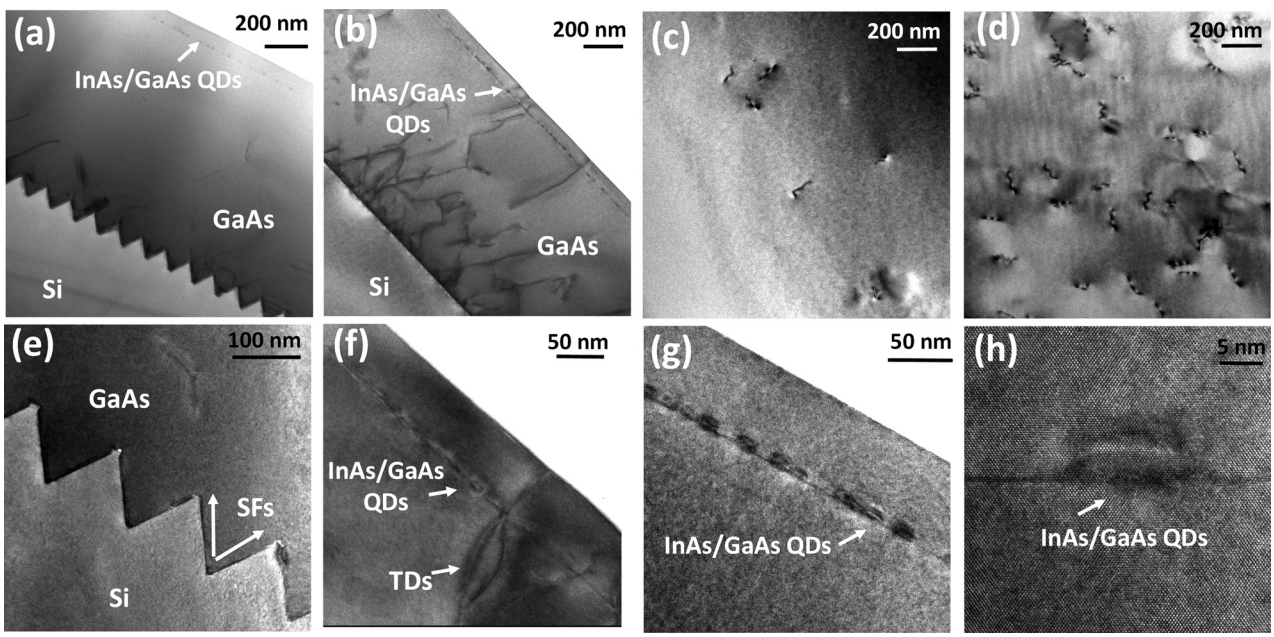

FIG. 2. (a) Cross-sectional TEM image of the QDs structure grown on the GoVS substrate, (b) cross-sectional TEM image of the QDs structure grown on the offcut Si template, (c) plane-view TEM images showing the threading dislocations on the GaAs surface for the GoVS substrate, (d) plane-view TEM images showing the threading dislocations on the GaAs surface for the offcut silicon template, (e) cross-sectional TEM image showing the defect trapping in the coalesced GaAs thin film on the GoVS substrate, (f) cross-sectional TEM image showing the defects penetrating through QDs region on the offcut Si template, (g) cross-sectional TEM image of the InAs/GaAs dot arrays on the GoVS substrate, and (h) high-resolution TEM image revealing the typical size and shape of the dots.

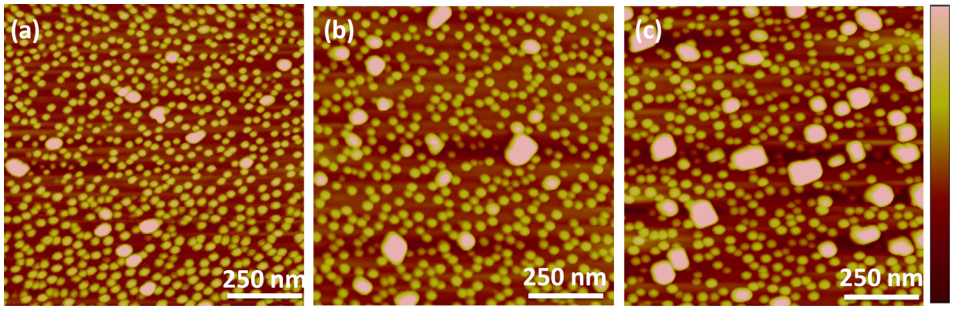

FIG. 3. AFM image of the uncapped QDs on (a) the GaAs substrate, (b) the GoVS substrate, and (c) the offcut silicon template. The vertical bar is 20 nm.

width), consistent with the TEM images where a higher defect density in the active region is observed. It should be noted that the reduced PL intensity on the Si substrates as compared to that on the GaAs substrate is partially related to the compromised PL efficiency by the high defect density buffer. Some of the carriers that diffused into the buffer layer on Si substrates will be trapped, while this is not an issue on GaAs. Fig. 4(b) displays low-temperature PL comparison of the three QD structures. At 40 K, the PL line shape is clearly asymmetric and a tail appears on the high energy side. The tail keeps its shape and position with the change of incident power, suggesting that it stems from the ground state emission of the dots with different size rather than emission from excited states.[14] It is noted that, on the offcut Si template, the tail dissolves into the main peak, giving rise to a much broader line-width and weaker signal at 40 K. In contrast, samples on the GoVS substrate and native GaAs substrate share similar differences in PL line shape at 40 K, similar to those at room temperature.

A comparison of the temperature-dependent line-width and peak position is shown in Fig. 4(c). An anomalous decrease of line-width with increasing temperature[15,16] is observed for the sample on the offcut Si template, while this trend is less obvious for the samples on the GoVS substrate and the GaAs substrate. At the low temperature range, indiscriminate population of the dots by carriers gives rise to a broad line-width. When temperature increases, thermal escape of carriers from smaller dots is easier than that from larger dots, as the larger dots have confined states at lower energies and the smaller dots at higher energies.[17] This results in a preferential quenching of photoluminescence from the smaller QDs, leading to red-shifting of the PL peak with a concomitant decrease in the line-width.[15] The QDs on the offcut Si template witness a more obvious inhomogeneous broadening of the dot size distribution and, as a result, show stronger temperature dependency.

Fig. 4(d) depicts the integrated PL intensity as a function of the reciprocal temperature for the three samples. The PL quenching at high temperatures is fitted with the Arrhenius equation,[18] giving thermal activation energies of about 110 meV, 108 meV, and 103 meV for the samples on the GaAs substrate, the GoVS substrate, and the offcut silicon template, respectively. As the emission peak and thermal activation energy remain close in value, similar band structures of the QDs are expected for the three samples,[7] indicating that the emission intensity difference shown in Figs. 4(a) and 4(b) is mainly ascribed to the defect density in the materials. The inset of Fig. 4(d) presents a comparison of the PL

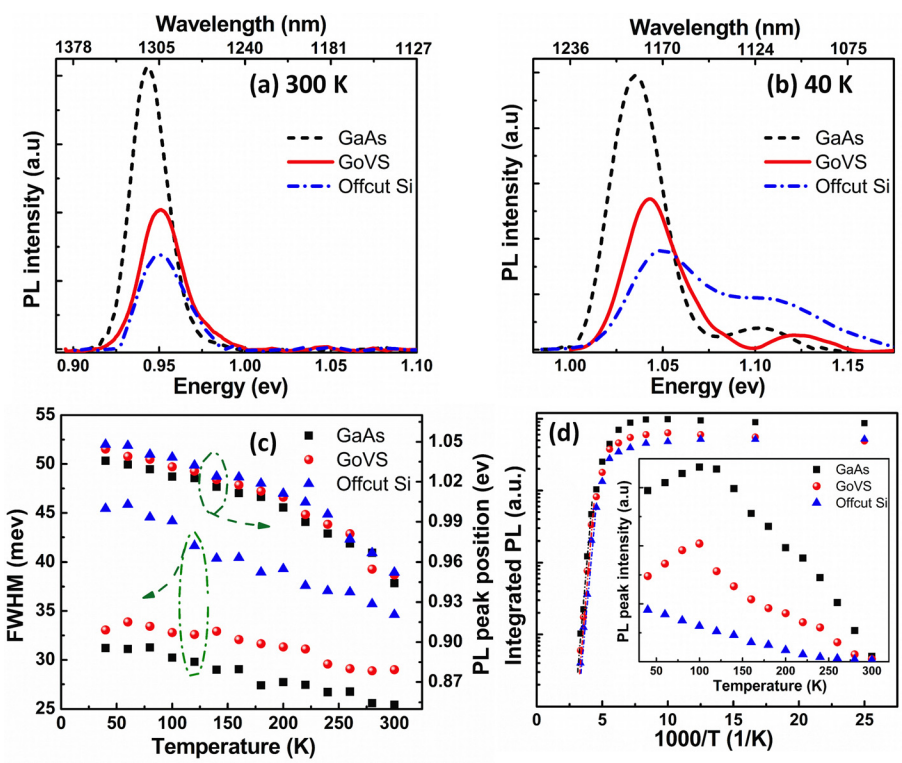

FIG. 4. (a) Room temperature (300 K) and (b) low temperature (40 K) PL spectra of the InAs/GaAs QDs grown on the GaAs substrates, the GoVS substrate, and the offcut Si template. (c) Temperature dependent FWHM and peak position of InAs/GaAs QDs on the GaAs substrates, the GoVS substrate, and the offcut Si template. (d) Integrated PL intensity as a function of the reciprocal temperature of InAs/GaAs QDs on the GaAs substrates, the GoVS substrate, and the offcut Si template; the inset shows the temperature dependent peak intensity of the three samples.

peak intensity. From 40 K to 100 K, an abnormal increase in ground-state PL intensity[15,19] occurs for the QDs on the GoVS substrate and the GaAs substrate, while continuous PL quenching is observed for QDs grown on the offcut Si template. When temperature increases in this range, carriers excited in the wetting layer are more likely to gain sufficiently large thermal energy to diffuse, be trapped, and ultimately recombine in the dots. This recapturing effect is stronger than thermal activation in QDs, contributing to the increase in PL intensity, as is the case for QDs on the GoVS substrate and the GaAs substrate. For QDs grown on the offcut Si template, however, photo-carriers in the wetting layer recombine non-radiatively instead of relaxing into the dots. Thus, PL intensity decreased due to aggravated carrier escaping and trapping process induced by a larger amount of non-radiative recombination centers in the active layer.

In conclusion, InAs/GaAs QDs emitting in the 1.3 μm band at room temperature have been achieved on a specially engineered GaAs-on-V-grooved-Si substrate by MOVPE. The structural and optical properties were characterized and compared with QDs grown on a lattice-matched GaAs substrate and on an offcut Si template. An enhanced PL intensity quenching with increasing temperature was observed on the offcut Si template due to thermal escape of carriers from QDs to non-radiative recombination centers. This is partly related to a higher density of defects penetrating the active region, as seen in the TEM images, and partly related to the higher density of coalesced dots according to AFM measurement. The superior optical quality of the InAs/GaAs quantum dots grown on V-groove patterned Si over traditional offcut Si template offers great opportunities for realizing a CMOS-compatible monolithic platform in III-V/Si integration.

This work was supported in part by Grant Nos. 614312 and 614813 from the Research Grants Council of Hong Kong. The authors would like to thank SEMATECH for providing the initial nano-patterned Si substrates and the MCPF of HKUST for technical support. Helpful discussions with C. Liu are also acknowledged.

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