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Low threading dislocation density GaAs growth on on-axis GaP/Si (001)

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We report a systematic study of high quality GaAs growths on on-axis (001) GaP/Si substrates using molecular beam epitaxy. Various types of dislocation filter layers and growth temperatures of initial GaAs layer were investigated to reduce the threading dislocation densities in GaAs on GaP/Si. Electron channeling contrast imaging techniques revealed that an optimized GaAs buffer layer with thermal cycle annealing and InGaAs/GaAs dislocation filter layers has a threading dislocation density of $7.2 \times 10^6\,\mathrm{cm}^{-2}$, which is a factor of 40 lower than an unoptimized GaAs buffer. The root-mean-square surface roughness was greatly decreased from 7.8 nm to 2.9 nm after the optimization process. A strong enhancement in photoluminescence intensity indicates that the optimized GaAs template grown on on-axis (001) GaP/Si substrates is a promising virtual substrate for Si-based optoelectronic devices. *Published by AIP Publishing.*

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I. INTRODUCTION

The epitaxial growth of GaAs layers on Si substrates has been extensively studied for large-scale, high performance III-V optoelectronic devices on Si, since the first demonstration by molecular beam epitaxy (MBE).[1] One of the main obstacles to overcome from a materials standpoint is the large lattice mismatch between GaAs and Si (~4%), which typically generates a high density of threading dislocation (TDs), up to $\sim 10^9\,\mathrm{cm}^{-2}$. Such high threading dislocation densities (TDDs) in the GaAs buffer layers have hindered successful demonstrations of high performance and reliable optoelectronic devices on Si substrates. In order to reduce the TDD, various growth techniques such as two-step growths,[2] dislocation filter layers (DFLs),[3] and thermal cycle annealing (TCA)[4] were introduced, and high quality GaAs buffers on Si with TDDs as low as $\sim 1 \times 10^6\,\mathrm{cm}^{-2}$ have been reported. Antiphase-domains (APDs) that arise from the polar (III-V) on non-polar (IV) growth interface are another type of defect that can readily form during GaAs/Si heteroepitaxy. APDs are two-dimensional defects, and they are known to be electrically active and detrimental to device performance.[5] To avoid the formation of APDs, almost all previous studies on GaAs heteroepitaxy on Si were carried out on intentionally miscut (typically 4°–6°) Si substrates to prepare diatomic steps on the surface.

Recently, the epitaxial growth of optoelectronic devices using "on-axis" (001) Si substrates has gained attention because offcut Si substrates are considered not fully compatible with current CMOS processing foundries.[6–8] However, the optimization of GaAs buffer growth on on-axis Si substrates has not yet been studied, and reported devices grown on unoptimized GaAs buffers with a relatively high TDD ($\sim 10^8\,\mathrm{cm}^{-2}$) have revealed considerably degraded performance. The APD-free GaAs growth on 300 mm size on-axis (001) Si wafers has been recently reported using metalorganic chemical vapor deposition (MOCVD) with improved optical and electronic properties.[9] Nevertheless, the GaAs layer contained a high density of TDs ($\sim 3 \times 10^9\,\mathrm{cm}^{-2}$) and stacking faults ($7 \times 10^7\,\mathrm{cm}^{-2}$), which is not suitable for the growth of high performance devices.[10] We have recently demonstrated highly efficient, record-low threshold current InAs quantum dot lasers grown epitaxially on on-axis GaP/Si, enabled by an optimized GaAs buffer layer (TDD $= \sim 7.2 \times 10^6\,\mathrm{cm}^{-2}$).[11] However, the detailed MBE growth condition for the high quality GaAs buffer on the GaP/Si substrates has yet to be reported.

In this work, we present a systematic study of GaAs buffer layer growth on on-axis GaP/Si (001) substrates using MBE, leading to low TDD and low root-mean-square (RMS) surface roughness. We have investigated various types of DFLs and the role of the initial GaAs growth temperatures in reducing TDDs in the GaAs buffer layer. The optimized GaAs buffer showed a TDD of $7.2 \times 10^6\,\mathrm{cm}^{-2}$ based on electron channeling contrast imaging (ECCI) measurements. This is a reduction by a factor of 40 compared with the unoptimized one (TDD$= 2.8 \times 10^8\,\mathrm{cm}^{-2}$). We also have conducted atomic force microscopy (AFM) measurements to study the surface morphology. The root-mean-square (RMS) surface roughness of the GaAs layers on GaP/Si was improved from 7.8 nm to 2.9 nm in $10 \times 10\,\mu\mathrm{m}^2$ scans. The optical properties of the GaAs layers were assessed by measuring photoluminescence (PL) spectra at room temperature and an enhancement of the integrated PL intensity by a factor of 7 was observed after the optimization.

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II. EXPERIMENTAL DETAILS

All samples were grown in a Veeco Gen-II MBE chamber. The GaP/Si (001) on-axis wafer used in the work is commercially available in 300 mm size from $NAsP_{III/V}$ GmbH with potentially small unintentional miscut (0.1°–0.2°). Through a special pre-epitaxial heat treatment on the Si surface, APDs terminate in the pseudomorphically grown 45 nm thick GaP layer.[12] The GaP/Si wafer was cleaved into small pieces and loaded into the MBE chamber with molybdenum adapting plates. After the oxide desorption at 630 °C under As_2-overpressure, the substrate temperature was lowered to grow an initial 100 nm thick low-temperature GaAs (LT-GaAs) layer at a V/III ratio of 30. The growth temperature for the LT-GaAs layer ranged from 400 °C to 550 °C, while the growth rate was kept at 0.1 μm/h. Figure 1(a) shows *in-situ* reflection high energy electron diffraction (RHEED) patterns during the initial LT-GaAs layer growth. The relatively spotty patterns indicate the formation of GaAs islands on the GaP/Si substrate. A smooth surface was recovered when the LT-GaAs layer thickness was ~25 nm (not shown here). The substrate temperature was raised back to 600 °C to grow a 3 μm thick high-temperature GaAs (HT-GaAs) layer using a V/III ratio of 20 and a growth rate of 1 μm/h. During the HT-GaAs growth, typical (2×4) streaky RHEED patterns were clearly observed as shown in Fig. 1(b). It should be noted that we kept the total III-V layer thickness identical to the reference sample (3145 nm) in this study because the TDD decreases with a thicker buffer layer (typically TDD ~1/film thickness).[13,14]

Etch pit density (EPD) and plan-view transmission electron microscopy (TEM) methods have been traditionally used to count TDs in GaAs buffer layers.[15,16] Instead, the ECCI technique has recently received much attention as a useful tool for non-destructive, rapid, and accurate TD measurement for III-V materials.[17–19] Furthermore, TDs generated during strain relaxation tend to form in clusters and the limited resolution (a few microns) of the EPD technique can result in underestimating the actual TDD.[15,20] A FEI Quanta 400f scanning electron microscope equipped with a field-emission electron gun and a pole-piece mounted back-scattering detector was used for ECCI. The electron accelerating voltage ranged from 20 to 30 keV with a ~5 nA beam current.

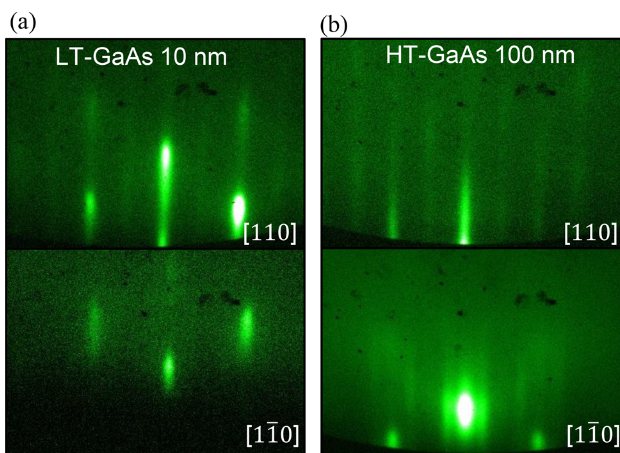

FIG. 1. RHEED patterns of (a) 10 nm thick LT-GaAs layer and (b) 100 nm thick HT-GaAs layer on GaP/Si substrate.

We first consider the possible electron channeling pattern (ECP) conditions for TD detection. Strain relaxation in this high lattice-mismatch GaAs/Si (or GaAs/GaP/Si) system occurs through a relatively complex process.[21] The large misfit induces the formation of GaAs islands on Si (or GaP/Si) in the first few monolayers, which results in a high density of 90° pure edge dislocations.[22,23] However, the edge dislocations are sessile and cannot glide along the interface to allow further strain relaxation. Therefore, 60° glissile misfit dislocations (MDs) begin to nucleate as the GaAs layer thickness increases to fully relax. Eight of the twelve slip systems (Burgers vectors and glide planes) in the zincblende structure are glissile dislocations during growth in the [001] direction. These are listed below.[24]

a/2[10$\bar{1}$] (111), a/2[01$\bar{1}$] (111), a/2[101] ($\bar{1}\bar{1}$1), a/2[011] ($\bar{1}\bar{1}$1), a/2[101] ($\bar{1}$11), a/2[01$\bar{1}$] ($\bar{1}$11), a/2[10$\bar{1}$] (1$\bar{1}$1), and a/2[011] (1$\bar{1}$1), where a is lattice constant of GaAs.

Other possible MDs are sessile dislocations with Burgers vectors and line directions in the plane of the interface. The Burgers vectors are the type of a/2[110]. These dislocations are formed by either dislocation fusion processes or during the initial GaAs islanding phase. Therefore, if we use a channeling condition consisting of both the {040} and {220} excitation, the $\mathbf{g} \cdot \mathbf{b}$ invisibility criterion can be avoided for dislocations that have threaded onto the surface. One such channeling condition used in this work is shown in Fig. 2(a). The sample was tilted at an angle of 2°–3° to achieve the channeling condition. An exemplary plan-view ECCI image of the reference sample is shown in Fig. 2(b). The small bright/dark spots are individual TDs on the surface. Additionally, segments of dislocations have been shown to have a tendency to appear bright as a result of increasing depth and deviations from the exact Bragg condition.[25] We have detected ~500 TDs by imaging an area of 180 μm^2 from the reference sample, and the TDD is $\sim 2.8 \times 10^8\,cm^{-2}$. The TDD from the unoptimized GaAs buffer layer on GaP/Si is consistent with the value measured by plan-view TEM.[6,26] The RMS surface roughness of GaAs buffers was calculated by averaging five different images using a Veeco Dimension 3100 AFM machine. Figure 2(c) shows a representative $10 \times 10\ \mu m^2$ AFM image with a line scan profile along the [110] direction, and the average RMS roughness was 7.8 nm. This high surface roughness is mainly due to the islanding growth mechanism in the initial GaAs layer.

III. RESULTS

A. *In-situ* thermal cycle annealing (TCA)

We first investigate the effects of TCA in the GaAs buffer layers on on-axis GaP/Si. A 100 nm LT-GaAs layer was grown on the GaP/Si wafer at 500 °C. Four cycles of thermal annealing were applied after growing a 1.5 μm thick HT-GaAs layer at 600 °C, which was followed by another 1.5 μm HT-GaAs layer to complete the growth. During TCA, the substrate was first heated to 700 °C under As_2-

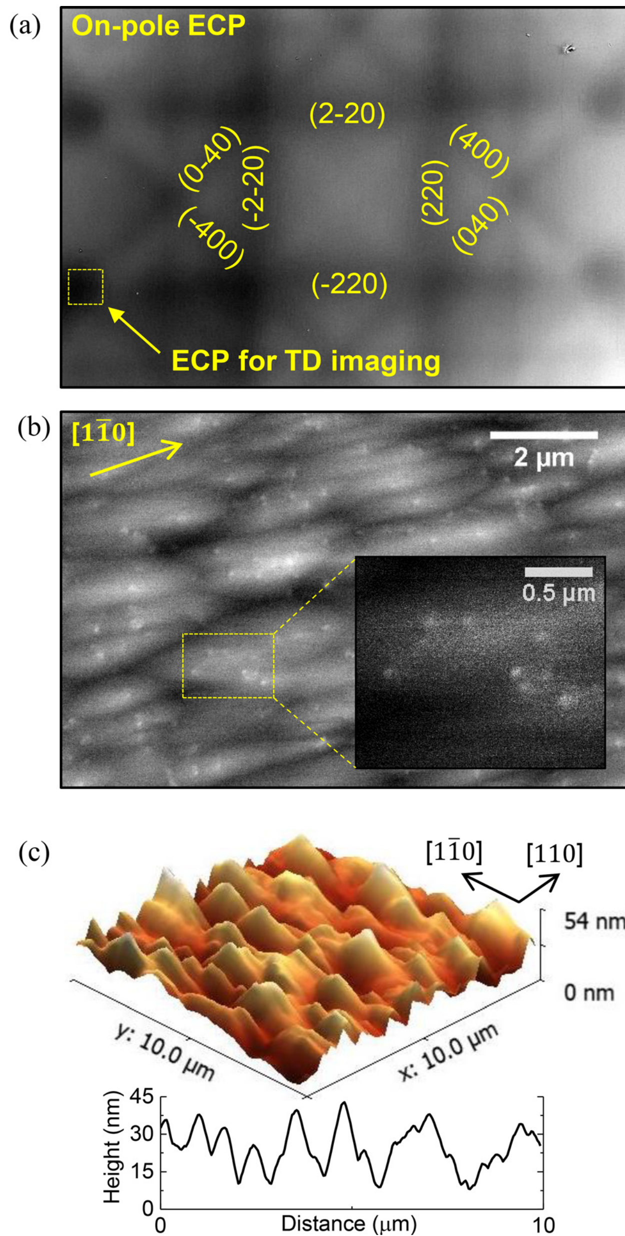

FIG. 2. (a) On-pole electron channeling pattern from GaAs on on-axis (001) GaP/Si. (b) ECCI and (c) $10 \times 10\,\mu m$ AFM image and line profile along [110] direction of GaAs on GaP/Si reference sample. Threading dislocations are shown as bright/dark spots. The inset of (b) is zoomed-in image showing distinctive 8 threading dislocations.

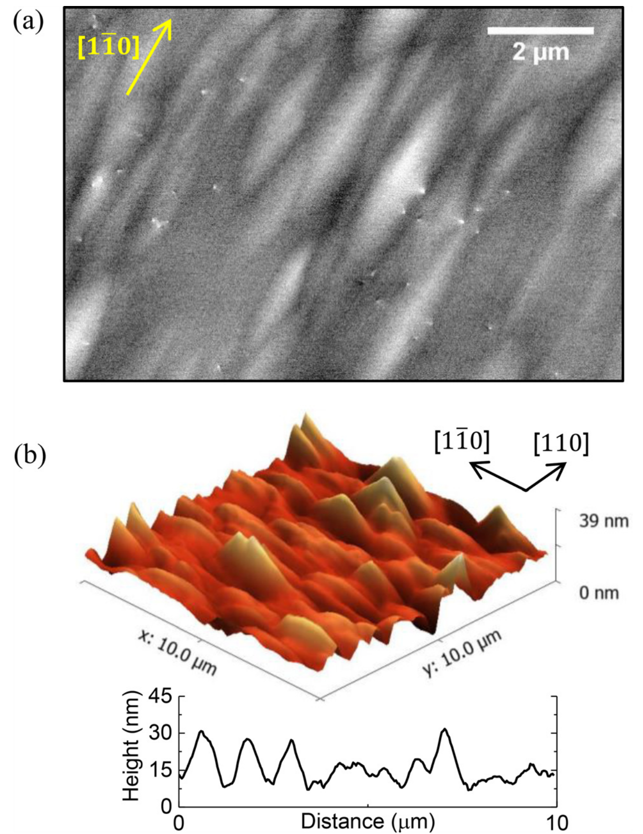

FIG. 3. (a) ECCI and (b) AFM image and line profile along [110] direction from GaAs on GaP/Si sample with application of four cycles of thermal annealing.

overpressure, measured by pyrometer, and held for 5 min. The substrate temperature was then lowered to 320 °C. The lower bound of the TCA was set at ~320 °C because dislocations are essentially immobile around ~450 °C and do not interact each other.[27,28] An ECCI image of Fig. 3(a) reveals a significantly lowered TDD in the sample with TCA, and the calculated TDD is $5.5 \times 10^7\,cm^{-2}$. It is believed that the majority of TDs are removed during the thermal annealing.[4] More specifically, the thermal stress due to the differential thermal expansion coefficients force the TDs to glide during TCA, and two approaching 60° MDs either fuse or annihilate depending on their Burgers vectors.[29,30] Also, note that some of the remaining TDs appear aligned in the [110] direction in Fig. 3(a), indicating a less effective dislocation reduction for β-type dislocations. The application of TCA significantly improved the surface roughness with an RMS roughness of 4.8 nm, as shown in Fig. 3(b).

B. Dislocation filter layers (DFL)

The effects of three different types of dislocation filter layers were studied. These were (a) 10 periods of 10 nm $Al_{0.4}Ga_{0.6}As$ (AlGaAs)/10 nm GaAs strained-layer superlattices,[31] (b) a 200 nm $In_{0.1}Ga_{0.9}As$ (InGaAs) single layer,[32,33] and (c) 10 periods of 10 nm InGaAs/10 nm GaAs.[34] The DFL was inserted after four cycles of TCA. The samples were then capped with a 1.3 μm thick HT-GaAs layer. The growth rates for both the AlGaAs and InGaAs layers were ~1.1 μm/h. The substrate temperature was 600 °C for AlGaAs and 500 °C for InGaAs.

Representative ECCI images from each sample are shown in Figs. 4(a)–4(c). The TDDs are $4.8 \times 10^7\,cm^{-2}$, $9.3 \times 10^6\,cm^{-2}$, and $7.2 \times 10^6\,cm^{-2}$ for samples with the GaAs/AlGaAs strained layer superlattice, InGaAs single intermediate layer, and InGaAs/GaAs strained layer superlattice, respectively. The AlGaAs/GaAs DFL structure is nearly lattice-matched, and it is thought that not many pre-existing TDs bend at the AlGaAs/GaAs interface and experience dislocation fusion/annihilation.[31] However, compared with the sample with TCA only, the samples with the InGaAs single intermediate layer and InGaAs/GaAs strained layer superlattice reduced the TDD by a factor of ~5.2 and ~6.7,

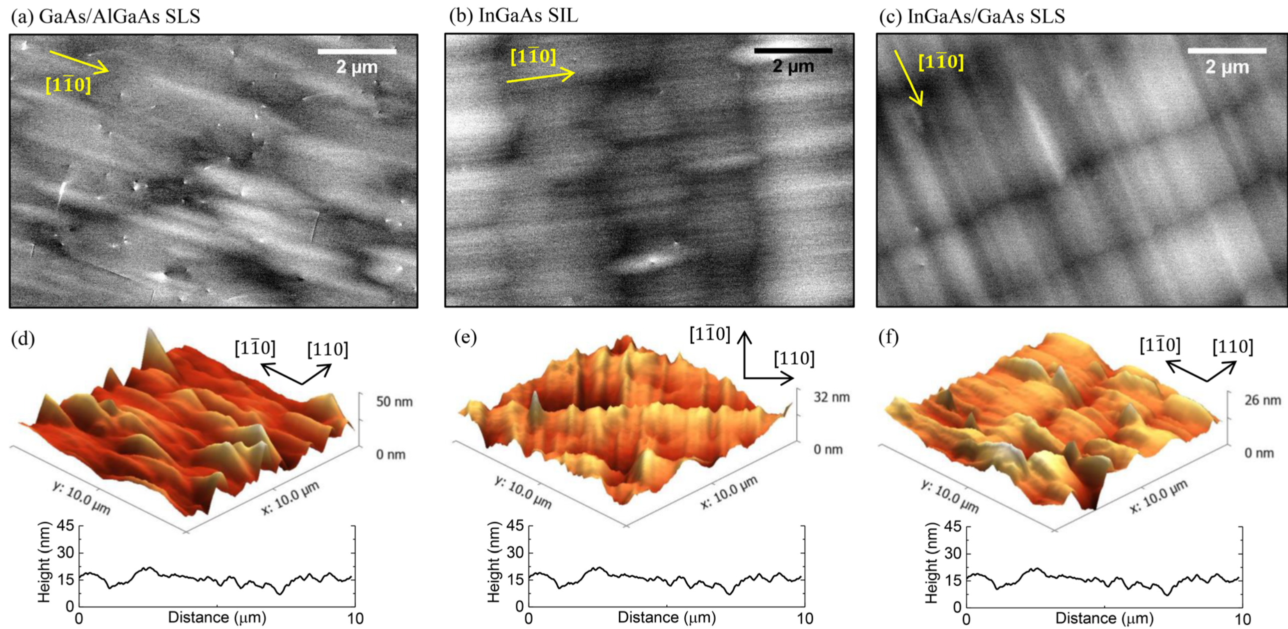

FIG. 4. ECCI and AFM images of GaAs on GaP/Si with [(a) and (d)] GaAs/AlGaAs strained layer superlattice, [(b) and (e)] InGaAs single intermediate layer, and [(c) and (f)] InGaAs/GaAs strained layer superlattice. The AFM line profiles are along [110] direction.

respectively. Previous studies on the effects of an InGaAs single intermediate layer in GaAs buffers grown by MOCVD showed a TDD of $\sim 1.2 \times 10^6\,\text{cm}^{-2}$ from PV-TEM surveys,[32,33] and Okamoto *et al.* also reported a low EPD of $\sim 1.4 \times 10^6\,\text{cm}^{-2}$ from the GaAs buffer layer using InGaAs/GaAs strained layer superlattice.[34] We suspect that the discrepancy in the TD reduction efficiency is likely due to the higher TCA temperatures possible in a MOCVD chamber and the use of (4°–6°) offcut Si substrates. A more detailed discussion is presented in Sec. IV.

Incorporation of the InGaAs layers also considerably improved the surface morphology of the metamorphic GaAs buffers, while the addition of the AlGaAs layers did not have the same effect. The measured RMS roughness for the three samples are 6.7 nm, 3.8 nm, and 2.9 nm for DFL-(a), (b), and (c), respectively. It should be mentioned that GaAs/AlGaAs DFLs actually roughened the GaAs surface compared with the TCA-only sample, while the InGaAs single intermediate layer and InGaAs/GaAs strained layer superlattice decreased the RMS roughness. Cross-hatch patterns along [110] and [1$\bar{1}$0] are clearly observed in Figs. 4(b) and 4(c). Therefore, we inferred that the MDs running at the InGaAs/GaAs interfaces help decrease the GaAs surface roughness. The higher density of cross-hatch along the [1$\bar{1}$0] direction compared with the [110] is attributed to the higher dislocation velocity of the α-dislocations (group-III core) than that of the β dislocations (group-V core) in the InGaAs/GaAs interfaces, commonly reported in growth studies as anisotropic relaxation.[35,36]

C. Growth temperature of LT-GaAs layer

Finding the optimal growth temperature of the initial LT-GaAs layer is important because the majority of the TDs in the final GaAs buffer layer form at the GaAs/GaP interface. The cross-sectional TEM (X-TEM) image shown in Fig. 5(a) shows a high density of MDs formed at the GaAs/GaP Si interface. In contrast, no MDs are observed at the GaP/Si interface because the MD density is lower than the X-TEM detection limit (typically $\sim$1 per μm). We grew the LT-GaAs layers at various growth temperatures ranging from 400 °C to 550 °C, and four cycles of TCA and one set of InGaAs/GaAs DFLs were applied to each sample. Figure 5(b) displays that the TDDs were first decreased from $3.8 \times 10^7\,\text{cm}^{-2}$ to $7.2 \times 10^6\,\text{cm}^{-2}$ as the growth temperature was increased from 400 °C to 500 °C. However, when the growth temperature was increased further to 550 °C, the TDD rose back to $1.3 \times 10^7\,\text{cm}^{-2}$.

It is expected that the size of the initial LT-GaAs islands on the GaP surface would increase with higher growth temperatures (with a lower island density). Up to 500 °C, more edge dislocations without threading segments in the GaAs islands could be formed to relieve the strain as increasing the size of initial GaAs islands. Once the islands coalesce, edge dislocations cannot glide along the interface to further relax the GaAs layer, and the formation of 60° glissile TDs begins to dominate the relaxation mechanism. Increasing the growth temperature of LT-GaAs might also be effective in reducing the initial TDD by increasing dislocation glide velocity. Beyond 500 °C, however, the dislocation nucleation rate, which increases exponentially with temperature,[37] may begin to dominate over the dislocation glide regime in the coalesced LT-GaAs layer. This resulted in the escalated final TDD in the LT-GaAs layer grown at 550 °C.

D. Number of InGaAs/GaAs DFLs

Three samples were grown to investigate the effects of increasing the number of InGaAs/GaAs DFLs on TDDs and surface roughness. One set of DFLs consists of 10 periods of 10 nm InGaAs/10 nm GaAs as described above, and each set of DFLs was separated by a 100 nm thick GaAs layer. The

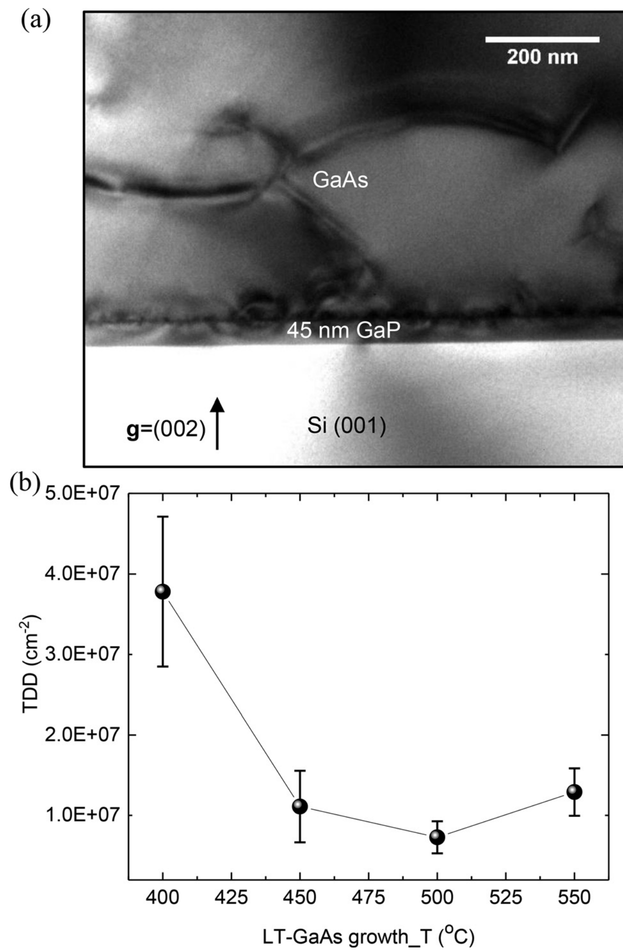

FIG. 5. (a) Cross-sectional bright-field TEM of GaAs on GaP/Si. (b) TDD versus LT-GaAs growth temperatures. The error bar represents the standard deviation. Nearly 3000 μm2 areas were surveyed by ECCI for each sample.

total III-V layer thickness was kept identical for all three samples. Figure 6 shows that the average TDD was increased as the number of sets of DFLs were increased, but the surface roughness continuously decreased. This result is contrary to the earlier work by George *et al.*,[38] where TDDs

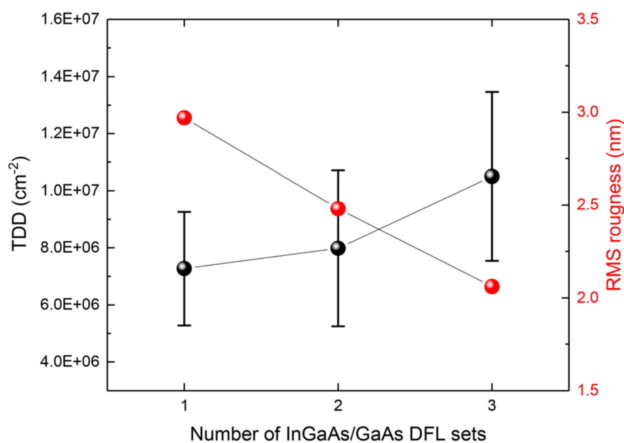

FIG. 6. TDD (black circles) and RMS roughness (red circles) versus number of InGaAs/GaAs DFL sets. The error bar in the TDD data represents the standard deviation, and nearly 3000 μm^2 areas were surveyed by ECCI for each sample. The RMS roughness presented is an average of five different $10 \times 10\ \mu m^2$ AFM scans.

were continuously decreased with more addition of DFLs. We believe that adding more sets of DFLs nucleated more dislocations to relax the upper InGaAs/GaAs DFLs rather than recycling the pre-existing TDs.

E. Room temperature photoluminescence

Four PL structure samples were grown on a GaAs wafer and three different GaAs/GaP/Si virtual substrates with TDDs of $2.8 \times 10^8\ cm^{-2}$, $4.8 \times 10^7\ cm^{-2}$, and $7.2 \times 10^6\ cm^{-2}$ respectively, to assess their optical properties. Figure 7(a) describes the GaAs/AlGaAs PL heterostructure. The GaAs and $Al_{0.4}Ga_{0.6}As$ layers were doped with Si to a target electron concentration of $2 \times 10^{18}\ cm^{-3}$. The samples were excited by a 785 nm laser with a power density of $\sim$6 W/cm^2. Figure 7(b) shows that the PL peak from all GaAs layers grown on GaP/Si show slight red-shifts ($\sim$13 meV) due to the residual tensile strain induced by differential thermal expansion coefficients. The calculated tensile strain from the observed red-shift is $\sim$0.2%, which agrees well with the values from previous reports.[28] It is noted that the integrated PL intensity from the optimized GaAs buffer layer is 7 times larger than the reference sample (TDD $= 2.8 \times 10^8\ cm^{-2}$). Compared with the GaAs layer grown on a native GaAs wafer, the optimized sample shows only $\sim$40% reduction in the PL intensity at room temperature.

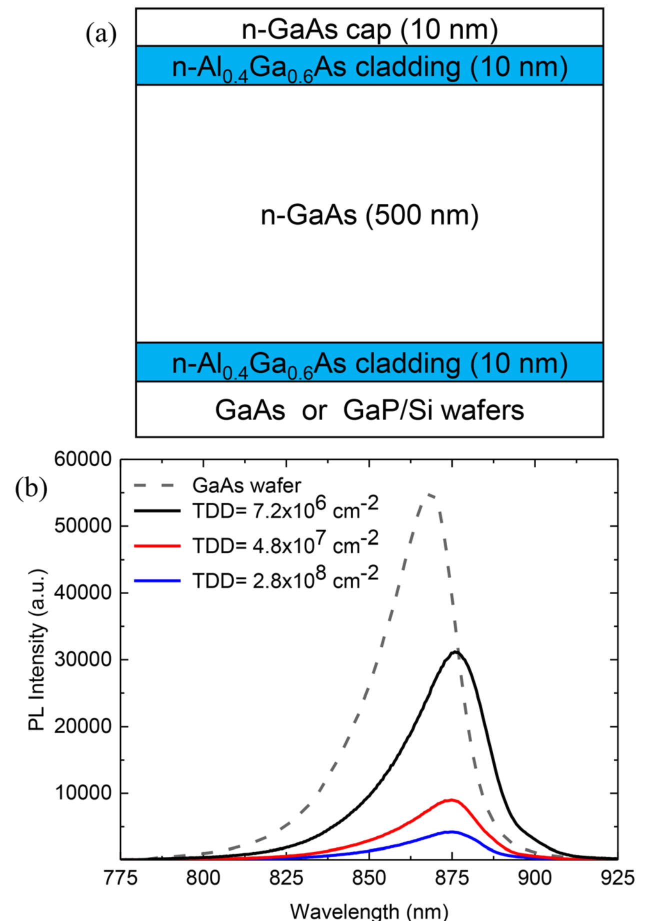

FIG. 7. (a) Schematic of GaAs/AlGaAs PL structure for optical property study. (b) Room temperature PL spectra of GaAs PL samples grown on native GaAs, and three different GaAs/GaP/Si templates.

IV. DISCUSSION

Despite significant improvement, the TDDs in the metamorphic GaAs buffer layers grown on on-axis (001) GaP/Si substrates are still higher than the previously reported best TDD values (1–$2 \times 10^6\,cm^{-2}$) using offcut (4°–6°) Si substrates. We speculated possible explanations for the results. First, the use of offcut Si substrates may encourage the formation of pure edge dislocations in the initial LT-GaAs buffer layers. Fischer *et al*. reported that the step edges on offcut Si substrates can promote the formation of pure edge dislocations over 60° dislocations.[39,40] Those edge dislocations are very effective in relieving strain energy without Burgers vectors in the growth direction, and this may lead to a lower density of TDs in the GaAs buffer layers on offcut Si than on-axis Si.[21] Second, the higher upper bound temperatures (e.g., 850 °C) during TCA available to MOCVD may have improved the efficiency of dislocation reduction by increasing dislocation mobility.[41] In our MBE system, we found that the highest TCA temperature is only ~700 °C without risking severe Ga desorption on the surface. Higher than this temperature, the surface of GaAs buffer layers became very hazy after growth. Third, dissimilar growth mechanisms in the early LT-GaAs growth stage between GaP and Si might also explain in discrepancy in the TDDs. GaAs on a GaP layer grows in a Stranski-Krastanov mode while GaAs on Si grows in a Volmer-Weber growth mode (direct islanding without a wetting layer).[42]

To further reduce TDDs in metamorphic GaAs buffer layers on on-axis (001) Si (GaP/Si), impurity doping in III-V materials could be considered. Once the TDD reaches $\sim 7 \times 10^6\,cm^{-2}$, the average distance between individual TDs is approximately $\sim 10\,\mu m$. For dislocation annihilation, these dislocations have to move much larger distances than when TDDs are in the range of $\sim 1 \times 10^8\,cm^{-2}$. Practically speaking, increasing the number of TCA to boost dislocation movements is not a realistic prospect. Instead, impurity doping such as with Zn could be considered as this is able to increase the dislocation glide velocity in GaAs,[43] especially the β-dislocation which is more than one order of magnitude slower than the α-dislocation in undoped-GaAs.[44] Another approach to reduce TDD is to employ $GaAs_xP_{1-x}$ compositionally step-graded buffers on GaP/Si. Yaung *et al*. demonstrated metamorphic $GaAs_{0.77}P_{0.23}$ layers with TDDs as low as $4 \times 10^6\,cm^{-2}$ on on-axis GaP/Si substrates.[37] Although grading $GaAs_xP_{1-x}$ buffers all the way to pure GaAs may increase the final TDD, yet, a combination of TCA and compositional step-grading scheme remains a promising approach to achieve a TDD of $\sim 1 \times 10^6\,cm^{-2}$.[45]

In conclusion, we have presented the MBE growth of GaAs buffer layers on on-axis (001) GaP/Si substrates. ECCI measurements showed that the TDD in the optimized GaAs layer is $7.2 \times 10^6\,cm^{-2}$, which is a factor of ~40 reduction compared with the unoptimized GaAs layer. The RMS surface roughness of the GaAs buffer layers also decreased from 7.8 nm to 2.9 nm after the optimization procedure. These structural improvements resulted in the optimized GaAs buffer layer on GaP/Si having a 7 times stronger integrated PL intensity than the unoptimized one. We believe that these high quality GaAs buffer layers with low TDDs and smooth surfaces will serve as versatile templates for high performance Si-based optoelectronic devices, including lasers and photodetectors as well as a myriad of photonic integrated circuits made from these devices.

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