A Heterogeneously Integrated III-V/Si Colliding Pulse Mode-locked Laser with On-chip Feedback

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Abstract: We demonstrate a heterogeneously integrated O-band III-V/Si colliding pulse mode-locked laser with tunable on-chip external feedback for pulse stabilization. The 3-dB RF linewidth is 13.8 kHz , a reduction by a factor of 2.9x with the adjustment of external feedback.

OCIS codes: (140.4050) Mode-locked lasers; (140.5960) Semiconductor lasers; (250.5300) Photonic integrated circuits.

1. Introduction

Compact, power-efficient, mass-producible low noise semiconductor passively mode-locked lasers (MLLs) are important because they can generate ultra-stable high frequency pulse trains and coherent frequency combs that can be employed in dense wavelength-division multiplexing (DWDM), high speed optical time-division multiplexing (OTDM), interchip/intrachip clock distribution, arbitrary waveform generation, millimeter wave signal generation, gas sensing, and spectroscopy [1-6]. Low noise passive mode-locking operation is usually obtained by lowering the optical confinement factor Γ to reduce the amount of amplified spontaneous emission (ASE) noise coupled to the oscillating mode, which is believed to be the main noise contributor [2]. An alternative method is to deploy an external feedback cavity to store the coherent photon energy and feed a small portion of light back into the cavity to suppress the ASE noise, which can also help to enhance the mode-locking quality [4-6]. In this paper, we demonstrate a fully integrated colliding pulse semiconductor MLL with tunable on-chip feedback by leveraging CMOS compatible heterogeneous silicon platform that provides low loss SOI waveguides and efficient light generation via bonding high-quality III/V material [7]. The length of the on-chip external cavity is an integer multiple of the laser cavity length, and it comprises of two phase tuners for controlling the optical feedback signal's strength and phase. Compared to its InP counterparts with cleaved facets, this fully integrated low noise heterogeneous MLL has all the components on chip, enabling integration within a more complex photonic integrated circuit.

2. Device design

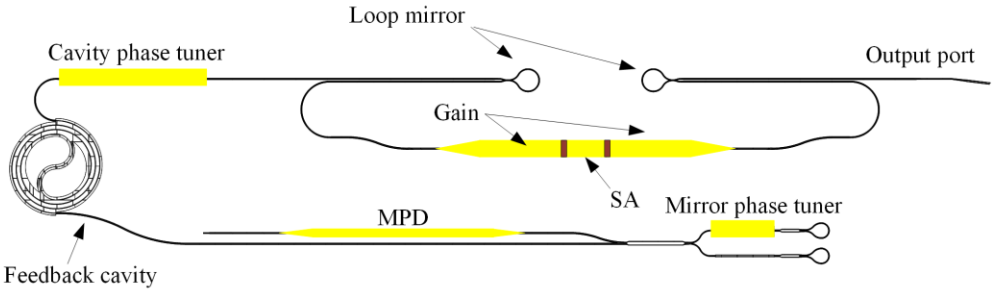

Fig. 1 A schematic diagram of the heterogeneously integrated colliding pulse mode-locked laser with on-chip feedback cavity. SA: saturable absorber, MPD: monitor photodiode.

A schematic diagram of the heterogeneously integrated colliding pulse mode-locked laser with on-chip feedback cavity is shown in Fig. 1. The laser chip was designed by UCSB and fabricated by employing heterogeneous photonic integration process developed under the DARPA EPHI program [8]. The basic laser cavity configuration is a colliding pulse design with cavity length of 3.937 mm, corresponding a fundamental mode-locking frequency of ~ 9.6 GHz, where the saturable absorber (SA) section is positioned in the middle of the cavity, enabling second harmonic operation. The total gain section length is 1200 μm, the SA length is 40 μm with two 15 μm isolation trenches in between the gain and SA section. The gain, SA section and the monitor photodiode (MPD) share the same III/V material and were wafer bonded onto the top of the pattered SOI waveguide. The reflectivities of the

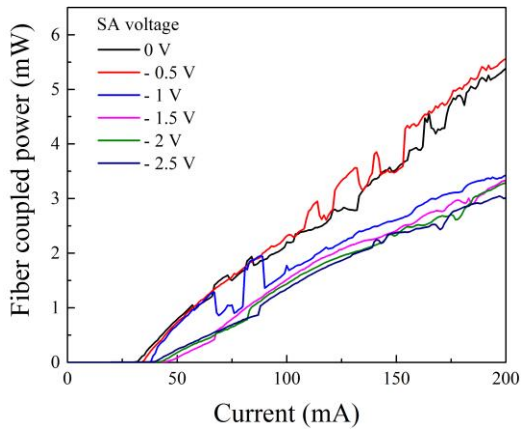

Fig. 2 Light-current curves of the MLL chip with different SA reverse biases. The phase sections are left floating.

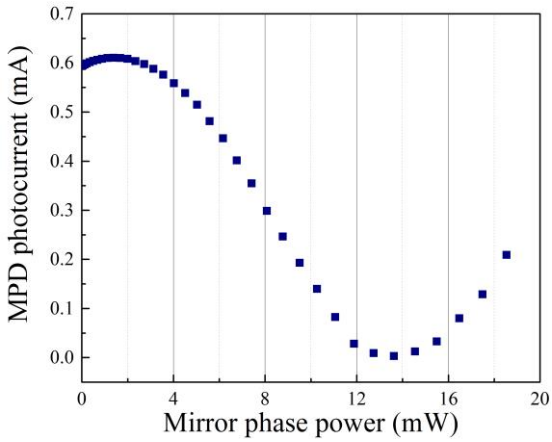

Fig. 3 MPD photocurrent vs mirror phase power (I_{gain} = 92 mA, V_{SA} = - 0.5 V, cavity phase left floating).

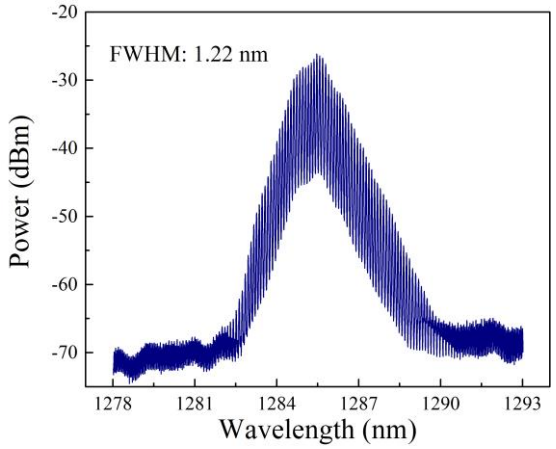

Fig. 4 Optical spectrum of the colliding pulse mode-locked state. The FWHM is 1.22 nm.

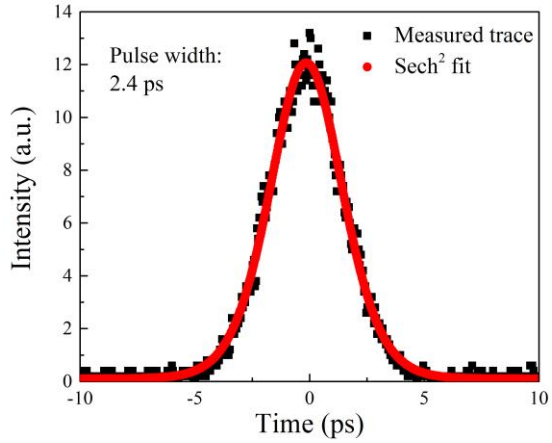

Fig. 5 Autocorrelation trace of the colliding pulse mode-locked state. The pulsewidth is 2.4 ps assuming $sech^2$ shape.

front and back loop mirrors are 15% and 85%, respectively. The output port connecting to the front mirror is 7° angled to minimize unintentional reflections. By introducing an external cavity connected through the back loop mirror, the optical feedback mechanism can be realized on-chip. The total length of the feedback cavity is twice of the fundamental cavity, comprising two phase tuners, a 2 × 2 multimode interferometer (MMI), two 1 × 2 MMIs and a MPD. It is terminated by two 100% reflectivity loop mirrors. By tuning the phase of one of the mirrors, optical feedback strength can be carefully controlled and monitored with the MPD. Combined with the control of the feedback phase, the final mode-locking quality can be improved, leading to low-noise operation. The total chip size is approximately 3.7 mm × 0.7 mm.

3. Device measurements

The MLL chip was mounted on a copper heat sink with a thermoelectric controller setting the stage temperature fixed at 20°. Laser characterization was first started with light-current (L-I) curve testing by sweeping gain section current with different SA reverse bias (phase sections left floating). The output light was collected by a 2-μm lensed single-mode fiber. The threshold current increases from 32 mA to 46 mA with the SA section increase in reverse bias as shown in Fig. 2. The increase in threshold current is due to the increased absorption in the SA section with higher reverse bias. The series resistance is around 2.6 Ω.

The passive colliding pulse mode-locking operation was then obtained by optimizing the gain section current and SA section reverse bias. A wide mode-locking area was obtained in the test condition (I_{gain}: 60 - 160 mA, V_{SA}: -0.2 V - -2.2 V) The optimal settings with phase sections left floating was I_{gain} = 92 mA, V_{SA} = - 0.5 V. We assume that

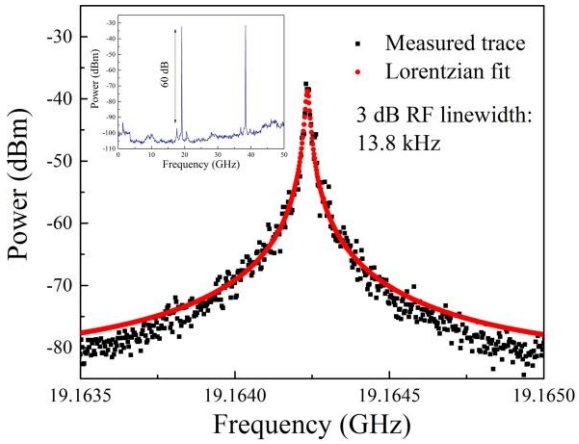

Fig. 6 3-dB RF linewidth of the colliding pulse mode-locked state with on-chip external feedback on (inset: 50 GHz span view with a >60 dB signal to noise floor ratio first harmonic RF signal).

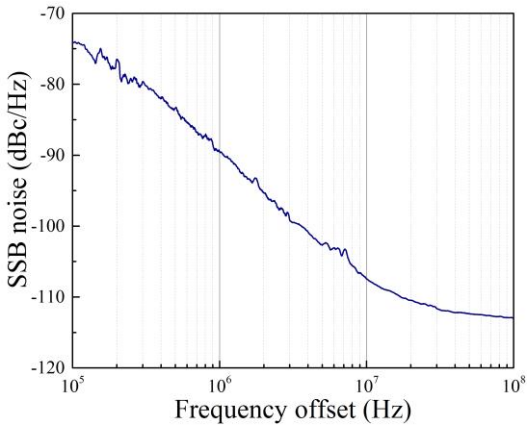

Fig. 7 Single sideband phase noise plot of the colliding pulse mode-locked state with on-chip external feedback on (100 kHz to 100 MHz).

the optical feedback to the laser fundamental cavity, with phase sections left floating, is minimal since nearly all the reflected optical power is captured by the MPD as shown in Fig. 3. The collected output was characterized by splitting and routing the pulse signal to an optical spectrum analyzer for spectral analysis, an autocorrelator for time domain analysis, and an electrical signal analyzer with a fast photodiode for RF frequency measurements, respectively. Fig. 4 and Fig. 5 show the optical spectrum and autocorrelation traces of the passive mode-locked state without the feedback. The full width half maximum value of the spectrum 1.22 nm, leading to a time-bandwidth product of 0.53 when paring with the fitted pulsewidth of 2.4 ps assuming a sech^2 shape pulse. Next the optical feedback was turned on by tuning the mirror phase section power above 2.7 mW, as shown in Fig. 3. The RF linewidth showed clear reduction from 40 kHz down to 13.8 kHz with fine tuning of the cavity phase sections ($P_{\text{mirror phase}}$ = 5.8 mW, $P_{\text{cavity phase}}$ = 3.7 mW). Inset in Fig. 6 shows a 50-GHz span view. The first harmonic RF signal with $>$ 60 dB signal to noise floor ratio indicates good mode-locking quality. Fig.7 presents the single sideband phase noise of the mode locking state. The timing jitter is around 1 ps when integrated from 100 kHz to 100 MHz. These results set up new records for a fully integrated MLL operating in the O-band. More sophisticated tests are on-going using low noise sources for measuring pulse width, mode locking area, output power dependency on feedback intensity and the results will be presented at the conference.

4. Conclusion

We present a fully integrated low noise heterogeneous InGaAsP/Si colliding pulse mode-locked laser with on-chip tunable feedback. By tuning the gain section forward current and saturable absorber (SA) reverse bias as well as the two phase sections power, the colliding pulse mode-locked laser generated 2.4-ps 19-GHz pulse trains with RF linewidth decreased from 40 kHz to 13.8 kHz in the O-band. Low loss silicon waveguides for long external feedback cavity can be integrated within the photonic circuits, leading to a significantly improved mode-locking performance. This design can be further improved with the integration of ultra-low loss silicon nitride waveguides.

Acknowledgements

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